Programmable logic elements using multigate ambipolar transistors

Ashton Snelgrove
Electrical and Computer Engineering
University of Utah
Salt Lake City, Utah, USA
ashton.snelgrove@utah.edu

Pierre-Emmanuel Gaillardon
Electrical and Computer Engineering
University of Utah
Salt Lake City, Utah, USA
pierre-emmanuel.gaillardon@utah.edu

***Abstract*—We propose a general purpose logic element with eight variations, built using multigate ambipolar transistors, sufficiently capable to replace LUTs in FPGAs. We simulate the new logic element using a 10nm silicon-nanowire three-input-gate transistor model, and compare the proposed element to lookup tables and reconfigurable logic elements from the literature implemented using the same technology model. We compare the different elements for delay, power, and number of transistors, specifically accounting for the cost of configuration storage. Compared to an equivalent LUT, the logic element variation with the most available boolean functions uses 90% of the transistors, with a penalty in delay of 102%, and improved dynamic and static power of 97% and 91%, respectively. The smallest variation uses 42% of the transistors, with improved delay of 76%, and improved dynamic and static power of 43% and 43%, respectively.**

***Index Terms*—reconfigurable logic, ambipolar transistor, multigate transistor, TIGFET, FPGA**

I. Introduction

Multigate ambipolar FETs are an emerging transistor technology that exhibit both p-type and n-type behavior. This transistor level reconfigurability has been a major motivation for research into these devices[1], and several reconfigurable logic elements have been described in the literature[2]–[7]. In this work, we propose a reconfigurable logic element based on majority of three (MAJ3) and XOR3 boolean functions, with a set of eight variations with different available boolean functions. These logic elements rely on the universality of a smaller set of functions rather than the complete set of functions available in lookup-tables (LUTs), the logic element commonly used in existing FPGA architectures.

Previous work has compared ambipolar circuits to comparable CMOS implementations, and compared silicon-nanowire three-input-gate FET (SiNW-TIGFET) to FinFET CMOS for logic synthesis and technology mapping [8]. This work instead seeks to explore architectures for FPGAs and other programmable devices that are not realizable using conventional transistors. To this end, we evaluate the performance of the proposed logic elements using a 10nm SiNW-TIGFET SPICE model, and compare with a LUT implementation and reconfigurable logic elements from the literature using the same technology model. A holistic analysis of reconfigurable circuits must also address the non-trivial costs of configuration storage: logic elements were simulated both with and without configuration flip-flops.

For the proposed logic elements, the variation with the most available boolean functions uses 90% of the transistors, with a penalty in delay of 102%, and improved dynamic and static power of 97% and 91%, respectively compared to an equivalent LUT. The smallest variation uses 42% of the transistors, with improved delay of 76%, and improved dynamic and static power of 43% and 43%, respectively.

The rest of the paper is organized as follows. Section II explains the motivation and background for examining new reconfigurable architectures. Section III describes the basic operating behavior of the multigate ambipolar transistor. Section IV covers prior art in reconfigurable ambipolar circuits. Section V presents our proposed logic element. Section VI discusses physical simulation results. Section VII contextualizes results and concludes the paper.

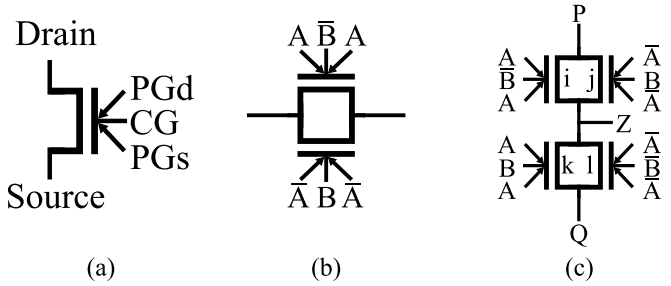
II. Background and Motivation

A. Configuration Storage Costs

For two-function reconfigurable gates the storage required is larger than the gate itself: three transistors vs. six for NAND2/NOR2 (see Figure 2(b) and 2(i)). This pattern continues with LUTs, in which the majority of the total transistors are used for storage. k-LUTs are capable of implementing each of the 2^{2^k} possible boolean functions of k inputs. This comes at the cost of 2^k bits of configuration storage. Not all of these functions are unique: the permutation (P) and negation-permutation-negation (NPN) classes for three-input functions are 220 and 14 distinct functions respectively[9]. The LUT does not provide flexibility in the number of available

This material is based on research sponsored by Air Force Research Lab (AFRL) and Defense Advanced Research Projects Agency (DARPA) under agreement number FA8650-18-2-7849, and the National Science Foundation (NSF) CAREER Award number 1751064.

978-1-6654-9431-1/22/$31.00 ©2022 IEEE



(a) (b) (c)

Fig. 1. (a) Symbol for TIGFET device. (b) Biconditional transmission gate. (c) Reconfigurable XOR block.

functions - changing the number of functions requires either doubling or halving the size.

This creates an opportunity to design logic elements with fewer possible boolean functions, creating a less complete but more compact, power efficient, and faster logic element.

B. Logic Synthesis

AND-inverter graphs (AIG) are a standard representation of logic during logic synthesis and optimization[10]. NAND and NOR are universal gates, so the graph is functionally complete. The XOR function is heavily used in circuits with arithmetic logic, but is costly in an AIG graph. The addition of XOR and MAJ3 gates increases the available functions during synthesis creating the XOR-AND-inverter (XAG), majority-inverter (MIG)[11], and XOR-majority-inverter (XMG) graph representations[12].

The set of functions used in these graphs provide a guide to the functions needed for reconfigurable logic elements. The use of non-traditional FPGA architectures such as ultra-fine-grain logic clusters[4] allows opportunities during logic synthesis for direct use of these graphs without the requirement of mapping to LUTs, so-called one-pass synthesis. [13].

III. Ambipolar transistor behavior

Ambipolar FETs behave as a p-type or an n-type transistor depending on the bias voltage applied to the transistor *polarity gate* terminal. This originates from electrostatic modulation of Schottky barriers at the source and drain terminals[14]. For a three-gate transistor, the gate terminals are the polarity gate at source (PG_s), the control gate (CG), and the polarity gate at drain (PG_d), with function determined by the bias voltage applied to PG_s. The electrical symbol is shown in Figure 1(a). The transistor is on when the three gate terminals are either all V_{ss} (p-type) or all Vdd (n-type). Depending on the gate terminal switched, the transistor exhibits different voltage thresholds (V_t) and leakage current. When PG_d is switched, the transistor has high V_t and lower leakage current. When CG is switched, the transistor has low V_t and higher leakage current. The transistor behavior under various gate terminal values is listed in Table I.

Ambipolar FETs have been demonstrated in carbon nanotubes[7], silicon[14], and other materials [15]. The simulations performed in this work use a TIGFET model from [15], [16], based on TCAD physical simulations of a transistor built with $10nm$ silicon nanowires.

TABLE I
TIGFET behavior for polarity- and control-gate states.

PG_s	CG	PG_d	Type	State	V_t
0	0	0	p-type	on	
0	0	1	p-type	off	high
0	1	0	p-type	off	low
1	1	0	n-type	off	high
1	0	1	n-type	off	low
1	1	1	n-type	on	

IV. Prior Art

A. Polarity Configured Gates

The NAND2/NOR2, AOI21/OAI21, AOI22/OAI22, and XOR2/XNOR2 gates collected in [2] are configurable by controlling the polarity of value P. This can be fixed, set via configuration, or used as an additional input. Schematics of these logic gates are presented in Figure 2. An alternative implementation of XOR2/XNOR2 [5] is presented in 2(f), which does not require complemented inputs and saves one transistor at a delay penalty. MIN3 in 2(h) is notable for being non-polarity configurable due to the symmetric structure of the pull-up and pull-down networks.

B. Logic Elements

Three configurable circuits were proposed in [7] utilizing dynamic logic with a four-phase clock. The first circuit provides eight two-input functions (NAND2, NOR2, AND2, OR2, and the four implications) with three configuration bits. The circuit uses seven transistors. This was used as the basis for an ultra-fine-grain mesh FPGA design [3], [4]. The second circuit proposed provides six two-input functions (NAND2, NOR2, AND2, OR2, XOR2, and XNOR2) with three configuration bits using nine transistors. The final circuit proposed is a three function ALU using two configuration bits, with three inputs and two outputs. The first output implements AND3, OR3, and XOR3, while the second output implements AND2, MAJ3, and $A \wedge B \vee C \wedge \neg(A \wedge B)$.

The circuit proposed in [6] provides six two-input functions (NAND2, NOR2, AND2, OR2, XOR2, XNOR2) with three configuration bits. The circuit uses discrete basic MIN3, XOR3, and MUX2I gates. The schematic is presented in Figure 3(k).

The circuit proposed in [2] provides a six function ALU (NAND2, NOR2, XOR2, XNOR2, MAJ3, XOR3) using three configuration bits. It notably has mix of two- and three-input functions, and two outputs forming a full adder. The schematic is presented in Figure 3(l).

V. Proposed Reconfigurable Logic Cell

The biconditional XNOR transmission gate in Figure 1(b) is active when A and B are not equal. The core transmission block in Figure 1(c) utilizes two transmission gate branches,

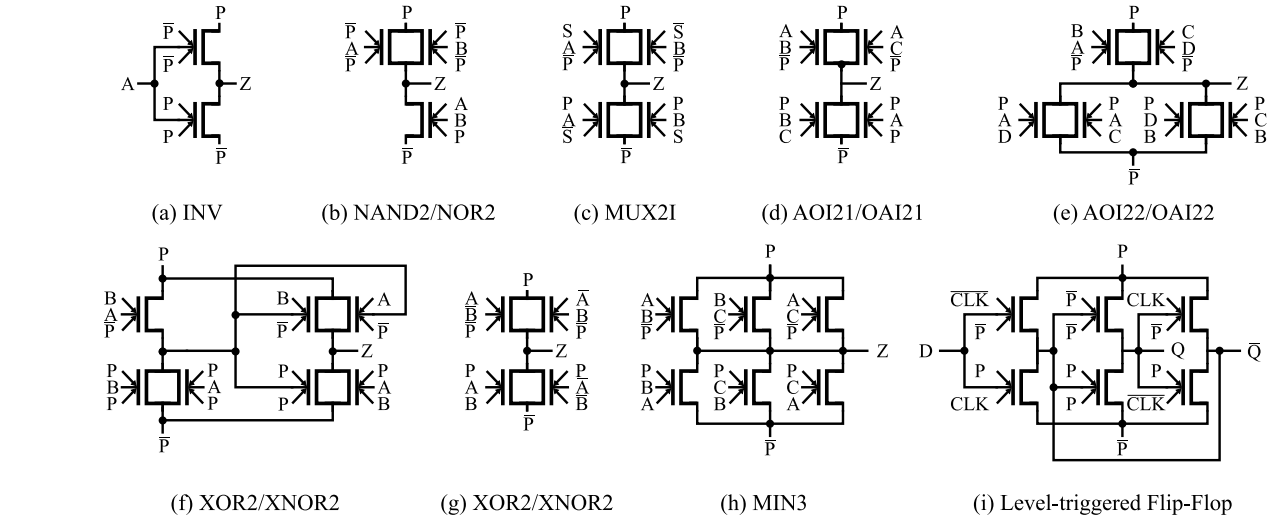


Fig. 2. Basic logic gates in TIGFETs. (a) and (h) are not polarity configurable. All other gates are polarity configurable.

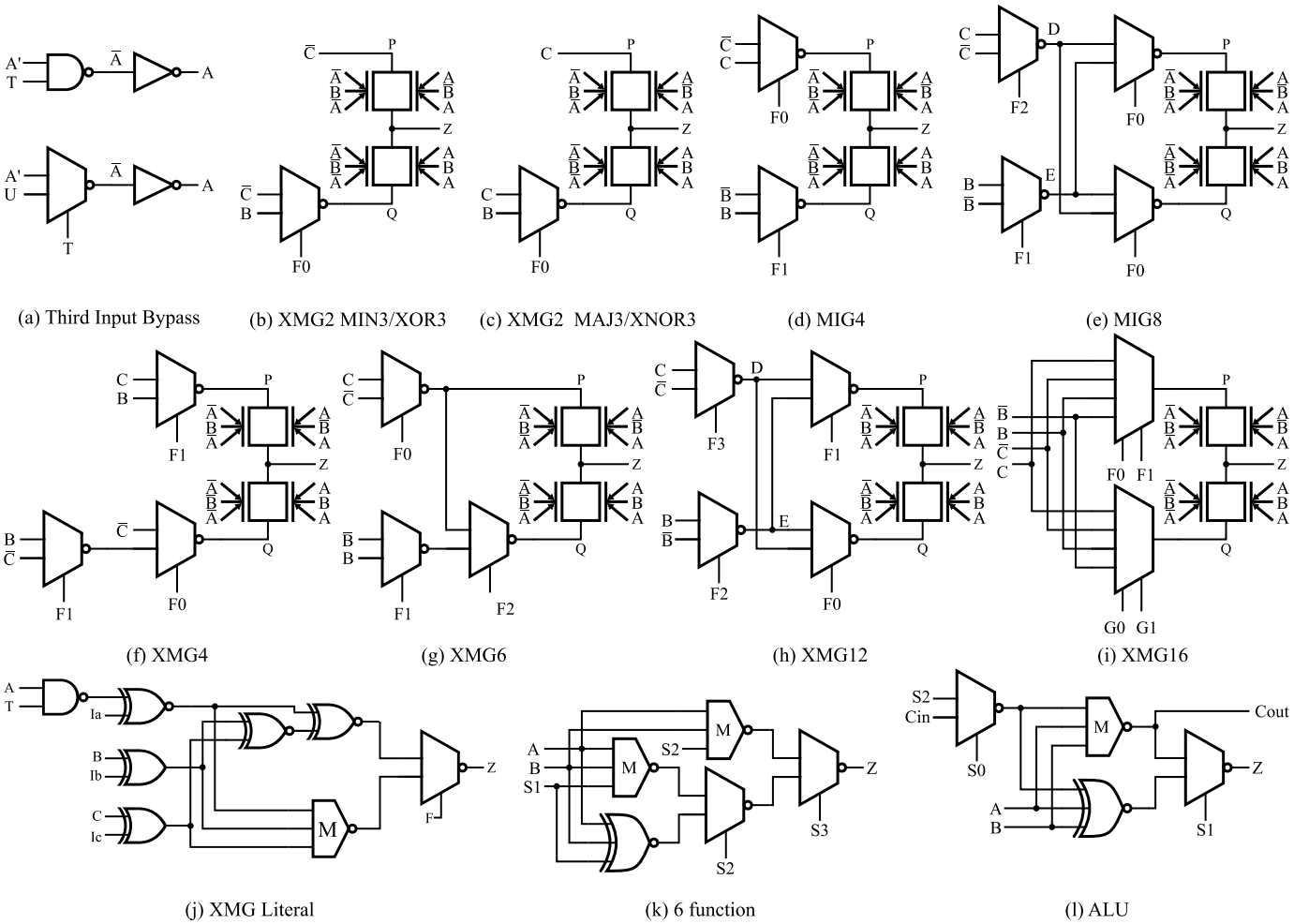


Fig. 3. Circuit variations implementing an XMG cell. (a) contains two options for configurable third input bypass.

TABLE II

LOGIC FUNCTION OF THE TRANSMISSION BLOCK IN FIGURE 1(C) WITH DIFFERENT CONNECTED INPUTS. GATE EXHIBITS MAJ3 WITH INPUT NEGATION, XNOR3, XOR3, IDENTITY, AND NEGATION. GATE EXHIBITS ALL 16 POSSIBLE TWO INPUT BINARY FUNCTIONS WHEN INPUT A IS BIASED TO FALSE (PRIMARY COLUMN) OR TRUE (SECONDARY COLUMN). REMAINING COLUMNS LIST THE AVAILABLE CONFIGURATIONS OF THE CIRCUITS IN FIGURE 3.

P	Q	Function	Primary	Secondary	XMG2	XMG2	XMG4	MIG4	MIG8	XMG6	XMG12	XMG16
C	B	$MAJ3(A,B,C)$	$B \wedge C$	$B \vee C$	0			11	111	000	1110	1101
B	C	$MAJ3(\neg A,B,C)$	$B \vee C$	$B \wedge C$					110		0001	0111
$\neg C$	$\neg B$	$MAJ3(\neg A,\neg B,\neg C)$	$\neg(B \wedge C)$	$\neg(B \vee C)$		0		00	001	011	0010	1000
$\neg B$	$\neg C$	$MAJ3(A,\neg B,\neg C)$	$\neg(B \vee C)$	$\neg(B \wedge C)$			00		000		1101	0010
$\neg C$	B	$MAJ3(A,B,\neg C)$	$B \not\Longrightarrow C$	$C \Longrightarrow B$			10	01	011	001	1010	1001
B	$\neg C$	$MAJ3(\neg A,B,\neg C)$	$C \Longrightarrow B$	$B \not\Longrightarrow C$					010		0101	0110
C	$\neg B$	$MAJ3(\neg A,\neg B,C)$	$B \Longrightarrow C$	$C \not\Longrightarrow B$				10	101	010	0110	1100
$\neg B$	C	$MAJ3(A,\neg B,C)$	$C \not\Longrightarrow B$	$B \Longrightarrow C$			01		100		1001	0011
$\neg C$	C	$XOR3(A,B,C)$	$B \oplus C$	$\neg(B \oplus C)$		1	11			1x1	x011	1011
C	$\neg C$	$XNOR3(A,B,C)$	$\neg(B \oplus C)$	$B \oplus C$	1					1x0	x111	1110
$\neg B$	B	A	F	T							1x00	0001
B	$\neg B$	$\neg A$	T	F							0x00	0100
B	B	B	B	B								0101
$\neg B$	$\neg B$	$\neg B$	$\neg B$	$\neg B$								0000
C	C	C	C	C								1111
$\neg C$	$\neg C$	$\neg C$	$\neg C$	$\neg C$								1010
Available functions with configurable bypass					6	6	12	12	16	18	24	32
Schematic figure					3(c)	3(b)	3(f)	3(d)	3(e)	3(g)	3(h)	3(i)

one XOR and the other XNOR. It has been previously demonstrated that the block can implement XOR3 when $P = \neg C$ & $Q = C$[17] and MAJ3 when $P = C$ & $Q = B$[13].

The pass transistor circuit yields a distinct function for all 16 possible combinations of C and B and their negations, as listed in Table II (A can be substituted for B). Depending on the input assigned to P and Q the circuit implements the identity and negation function for all three inputs, the MAJ3 function of all inputs and their possible negations, and the XNOR3 and XOR3 functions. When one input is biased, the circuit implements all possible two input functions.

The proposed logic element operates by configuring the connections to P and Q. The circuit variation with all possible combinations is presented in Figure 3(i). Seven additional variations with fewer available functions are presented in 3(b) to 3(h). The available functions for each of the circuit variations are listed in Table II. Functions were chosen to cover critical functions, to reduce redundancy, and to maximize number of available inversions of inputs and outputs. Elements are named XMG if both XOR3 and MAJ3 are used, and MIG if no XOR3 is used; a numeric suffix is given with the number of available three-input functions.

Pass transistor inputs are driven by the output of a non-pass transistor gate, minimizing voltage drop. Additionally, the need for complementary inputs to each element allows sharing of inverters between fanouts, reducing transistor count [18].

During logic synthesis, MIG and XMG will represent two-input functions by biasing one of the inputs to the MAJ3 or XOR3 gate. Adding additional configuration to the behavior of the third input A in the logic element mitigates mismatch between two- and three-input logic and increases the possible number of functions.

Input A can be directly connected to a flip-flop, creating a two input gate configurable between primary and secondary function, increasing total size by four transistors. A can be connected to a NAND2 gate, and biased to false with configuration bit T to bypass the third input to select only the primary two-input function, increasing the size by nine transistors. A can also be connected to a MUX2, with an additional configuration bit U selecting between primary and secondary when bypassed, increasing the size by sixteen transistors. Schematics for third input bypass are presented in Figure 3(a),

VI. PHYSICAL SIMULATION RESULTS

A. Configuration Storage and Lookup Tables

A basic level triggered D flip-flop was designed using six transistors, presented in Figure 2(i). If polarity P is changed, the flip-flop changes from positive to negative level triggered. This flip-flop is used for all simulations.

Basic lookup tables were constructed using trees of the MUX2I from Figure 2(c). Each additional input adds a layer of MUXs, for a total of $2^k - 1$ MUX2I and k inverters. No output inverters were added, so k-LUTs with even number of inputs are inverting while those with odd number of inputs are non-inverting.

B. Simulation setup

Physical simulation was done using Synopsys HSpice. The logic element output was connected to an inverter, which was not included in the measurements, to accurately model a fanout

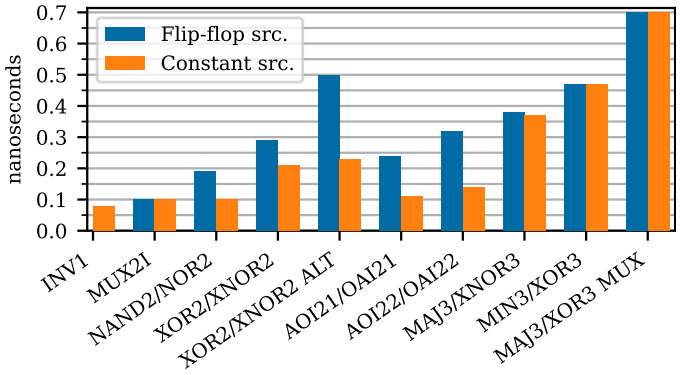


Fig. 4. Worst case delay for basic configurable gates with different configuration source.

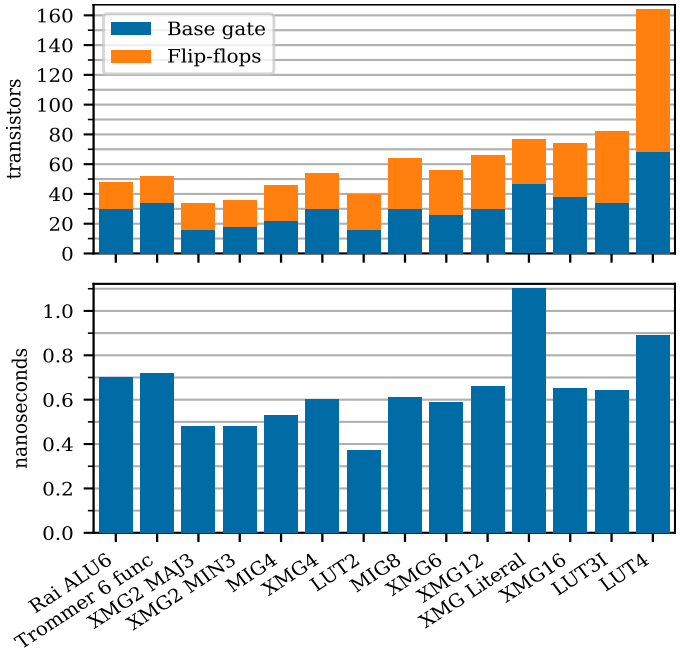


Fig. 5. (a) Size in transistors for reconfigurable logic elements. (b) Worst case delay in nanoseconds for reconfigurable logic elements. Logic elements are in order of increasing functionality.

to another device. The element was first tested with configuration bits connected to a constant source to characterize independent of storage. The element was then tested with configuration bits connected to flip-flops to characterize in a complete environment with storage. Transient timing was measured from 50% input rise to 50% output rise for all possible input transitions. Circuit size is measured in number of transistors, including from flip-flops. Testing for this work was limited to static logic, so the circuits from [7] were not evaluated. Simulation results are presented in Table III and IV.

C. Polarity Configurable Gates

The polarity configurable gates all have approximately double the delay between configuration set at constant voltage and when driven by flip-flops, as seen in Figure 4. The XOR2/XNOR2 in 2(g) demonstrates the least variation. The non-polarity configured gates have no difference in delay. This demonstrates that driving source/drain from configuration has a significant delay cost. The flip-flop causes a consistent increase in static power, on average $7.2e^{-}11$. No other difference in power is observed.

D. Logic elements

An XMG logic element using non-configurable logic gates was tested. A MUX2I is used to switch between MIN3 and XNOR3 gates, with inputs invertable using XOR2 gates. The schematic is presented in Figure 3(j). The elements from [2] in Figure 3(l) and [6] in Figure 3(k) are also tested. All three perform worse in power and delay compared to LUT3I. They did however use fewer transistors.

The results presented in Table IV, in Figure 5(a), and the rest of this section are for elements with bypass-configurable third input. For XMG16 3(i), adding the bypass-configurable circuit incurs a penalty of 16 transistors, an increase in dynamic and static power by 118% and 125%, respectively, and no change in delay over the base circuit.

All proposed logic element variants required fewer transistors than the LUT3I, as shown in Figure 5(a). Size correlates strongly with the number of functions, due to increase in storage cost per configuration bit as well as additional complexity in the base gate. LUTs are dominated by the cost of storage, 59% for LUT3I.

Size has a strong correlation with power. The proposed element performs better in dynamic and static power compared to LUT3I in all variations. The LUT networks perform well in dynamic power relative to their size, due to their larger proportion of storage. However for the same reason their static power consumption is higher.

Worst case delay through each circuit is consistent with the sum of gate delays along the critical path, as shown in Figure 5(b). Delay in XMG2-MAJ3 3(c) and XMG2-MIN3 3(b) was bounded by the bypass circuit, with base performance equivalent to LUT2. Delay does vary depending on the configured function - in the case of XMG16 3(i) the worst performing functions were the identity and inversion of B, 5% higher delay than the next worst non-identity function. Restricting the use of these functions during synthesis is a possible option to enable better performance.

VII. Conclusion

The eight variations of our circuit demonstrated here represent a set of possible choices for logic elements in future reconfigurable devices. The power, size, and delay of these circuits exceed the performance of a comparable three-input LUT. They range in functionality from two to sixteen three-input functions, with options for input bypass-configuration increasing the number of possible functions to thirty-two three- and two-input functions.

When designing an FPGA using the proposed circuit, the choice of which variation to use is a complex question. Future work is required for the determination of an effective balance between performance and functionality, and evaluating the relationship between architecture and logic synthesis.

TABLE III

SIMULATION RESULTS FOR BASIC LOGIC GATES. SIZE IS IN NUMBER OF TRANSISTORS, POWER IN PICOWATTS, AND WORST DELAY IN NANOSECONDS

Gate	Figure	Transistors		Dynamic Power pW		Static Power pW		Worst Delay ns	
		base	total	flip-flop	constant	flip-flop	constant	flip-flop	constant
INV1	2(a)	2	-	-	84	-	37	-	0.08
MUX2I	2(c)	4	10	143	72	111	37	0.10	0.10
NAND2/NOR2	2(b)	3	9	129	62	102	28	0.19	0.10
XOR2/XNOR2	2(g)	8	14	286	215	186	112	0.29	0.21
XOR2/XNOR2 ALT	2(f)	7	13	247	176	148	75	0.50	0.23
AOI21/OAI21	2(d)	4	10	129	62	102	28	0.24	0.11
AOI22/OAI22	2(e)	6	12	139	73	107	33	0.32	0.14
MAJ3/XNOR3	3(c)	12	18	278	205	208	135	0.38	0.37
MIN3/XOR3	3(b)	14	20	385	312	269	195	0.47	0.47
MAJ3/XOR3 + MUX		26	32	710	636	410	337	0.70	0.70

TABLE IV

SIMULATION RESULTS FOR RECONFIGURABLE LOGIC ELEMENTS. XMG AND MIG ELEMENT VARIATIONS USE A THIRD INPUT CONFIGURABLE BYPASS.

Gate	Figure	Funcs.	Config	Transistors			Dynamic Power pW		Static Power pW		Worst Delay ns	
			bits	base	store	total	flip-flop	constant	flip-flop	constant	flip-flop	constant
Rai ALU6	3(l)	6	3	30	18	48	859	673	560	374	0.70	0.70
Trommer 6 Fun.	3(k)	6	3	34	18	52	887	703	502	316	0.72	0.72
XMG2 MAJ3/XNOR3	3(c)	6	3	16	18	34	433	247	358	172	0.48	0.48
XMG2 MIN3/XOR3	3(b)	6	3	18	18	36	536	350	418	232	0.48	0.48
MIG4	3(d)	12	4	22	24	46	622	380	496	254	0.53	0.52
XMG4	3(f)	12	4	30	24	54	839	597	686	444	0.60	0.60
LUT2		16	4	16	24	40	537	242	426	131	0.37	0.37
MIG8	3(e)	16	5	30	34	64	878	468	696	310	0.61	0.63
XMG6	3(g)	18	5	26	30	56	771	473	605	307	0.59	0.59
XMG Literal	3(j)	20	5	47	30	77	1364	1067	931	633	1.10	1.09
XMG12	3(h)	24	6	30	36	66	847	495	668	314	0.66	0.66
XMG16	3(i)	32	6	38	36	74	976	625	758	404	0.65	0.64
LUT3I		256	8	34	48	82	1007	421	833	243	0.64	0.63
LUT4		2^{16}	16	68	96	164	1832	653	1573	395	0.89	0.89
LUT5I		2^{32}	32	134	192	326	3595	1239	3122	766	1.33	1.32
LUT6		2^{64}	64	264	384	648	6800	2091	6029	1321	1.89	1.89

REFERENCES

[1] S. Rai, S. Srinivasa, *et al.*, "Emerging reconfigurable nanotechnologies: Can they support future electronics?" In *Proceedings of the International Conference on Computer-Aided Design*, 2018.

[2] S. Rai, J. Trommer, *et al.*, "Designing efficient circuits based on runtime-reconfigurable field-effect transistors," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 27, no. 3, pp. 560–572, 2019.

[3] P.-E. Gaillardon, X. Tang, *et al.*, "A novel FPGA architecture based on ultrafine grain reconfigurable logic cells," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 23, no. 10, pp. 2187–2197, 2015.

[4] P.-E. Gaillardon, F. Clermidy, *et al.*, "Matrix nanodevice-based logic architectures and associated functional mapping method," *ACM Journal on Emerging Technologies in Computing Systems*, vol. 7, no. 1, pp. 1–23, 2011.

[5] M. Raitza, A. Kumar, *et al.*, "Exploiting transistor-level reconfiguration to optimize combinational circuits," in *Design, Automation Test in Europe Conference Exhibition (DATE), 2017*, 2017, pp. 338–343.

[6] J. Trommer, A. Heinzig, *et al.*, "Reconfigurable nanowire transistors with multiple independent gates for efficient and programmable combinational circuits," in *Proceedings of the 2016 Conference on Design, Automation & Test in Europe*, 2016, pp. 169–174.

[7] I. O'Connor, J. Liu, *et al.*, "CNTFET modeling and reconfigurable logic-circuit design," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 54, no. 11, pp. 2365–2379, 2007.

[8] R. Gauchi, A. Snelgrove, and P.-E. Gaillardon, "An open-source three-independent-gate FET standard cell library for mixed logic synthesis," ISCAS, 2022.

[9] C. R. Baugh, C. S. Chandersekaran, *et al.*, "Optimal networks of nor-or gates for functions of three variables," *IEEE Transactions on Computers*, vol. C-21, no. 2, pp. 153–160, 1972.

[10] A. Mishchenko and R. Brayton, "Scalable logic synthesis using a simple circuit structure," in *Proc. IWLS*, vol. 6, 2006, pp. 15–22.

[11] L. Amarú, P. Gaillardon, and G. D. Micheli, "Majority-inverter graph: A new paradigm for logic optimization," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 35, no. 5, pp. 806–819, 2016.

[12] Z. Chu, M. Soeken, *et al.*, "Structural rewriting in XOR-majority graphs," in *Proceedings of the 24th Asia and South Pacific Design Automation Conference*, 2019, pp. 663–668.

[13] L. Amarú, P.-E. Gaillardon, and G. De Micheli, "Biconditional BDD: A novel canonical BDD for logic synthesis targeting XOR-rich circuits," in *2013 Design, Automation Test in Europe Conference Exhibition (DATE)*, 2012, pp. 1014–1017.

[14] M. De Marchi, D. Sacchetto, *et al.*, "Polarity control in double-gate, gate-all-around vertically stacked silicon nanowire FETs," in *2012 International Electron Devices Meeting*, San Francisco, CA, USA, 2012, pp. 8.4.1–8.4.4.

[15] P. Cadareanu and P. E. Gaillardon, "A TCAD simulation study of three-independent-gate field-effect transistors at the 10-nm node," *IEEE Transactions on Electron Devices*, vol. 68, no. 8, pp. 4129–4135, 2021.

[16] P. Cadareanu, J. Romero-Gonzalez, and P.-E. Gaillardon, "Parasitic capacitance analysis of three-independent-gate field-effect transistors," *IEEE Journal of the Electron Devices Society*, vol. 9, pp. 400–408, 2021.

[17] A. Zukoski, X. Yang, and K. Mohanram, "Universal logic modules based on double-gate carbon nanotube transistors," in *Proceedings of the 48th Design Automation Conference*, 2011, pp. 884–889.

[18] X. Hu, A. S. Abraham, *et al.*, "Hybrid pass transistor logic with ambipolar transistors," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 68, no. 1, pp. 301–310, 2021.