An Open-source Three-Independent-Gate FET Standard Cell Library for Mixed Logic Synthesis

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***Abstract*—*Three-Independent-Gate FET* (TIGFET) technology is one of the most promising candidates to succeed CMOS and FinFET technologies due to its low off-current, compact surface area, reconfigurable logic, and CMOS compatibility. In this paper, we present an open-source standard cell library based on silicon nano-wire TIGFETs, which enables efficient implementation of novel XOR-and-majority-based circuit designs. We also discuss logic synthesis methods tailored to take advantage of TIGFET capabilities to allow their potential to be realized at the system level. By combining the 10 nm TIGFET technology with a mixed logic synthesis tool, the PicoRV core design shows a 2.3× lower area and a 5.7× lower energy consumption, compared to an equivalent low-power 12 nm FinFET implementation.**

***Index Terms*—Three-Independent-Gate FET, FinFET, XOR-Majority Graph, Logic Synthesis, Standard Cell.**

I. Introduction

For the past 50 years, the scaling of technology nodes has led to higher transistor density along with lower latency and power. However, this trend is slowing down due to physical limitations [1], primarily driven by leakage power and reaching the minimum threshold voltage, resulting in the end of Dennard's law and what is known as the "power wall" [2]. To overcome this limitation, new technologies are being explored. One promising technology is *Reconfigurable Field-Effect Transistors* (RFETs), which have the ability to alternate between n- and p-type after fabrication. Compared to CMOS and FinFET technology, the channel is replaced by silicon nanowires (SiNW) or similar gate-all-around topologies [3]. This structure gives several advantages, including low power consumption and reduced surface area. Of particular interest are the opportunities for novel circuits implemented using the reconfiguration of these transistors. One type of RFET, the *Three-Independent-Gate Field-Effect Transistor* (TIGFET) has demonstrated functionality at the transistor level to enable highly efficient 3-to-1 XOR and Majority (MAJ) logic gate structures [4], [5]. These gates are of particular interest for arithmetic circuits, as they implement the sum and carry operation respectively [4].

The adoption of reconfigurable logic requires *Electronic Design Automation* (EDA) synthesis tools to also adopt new techniques to fully exploit the new capabilities. Current EDA synthesis research has focused on the *And-Inverter-Graph* (AIG), which represents logic as a directed acyclic graph using only AND gates and inverter connections [6]. While the AIG is functionally complete, the addition of MAJ3 and XOR gates increases the capability of natively representing the full range of circuits. Recent works [7] [8] [9] aim at exploring different strategies based on *Majority-Inverter Graph* (MIG), *XOR-AND-Inverter Graph* (XAG), and *XOR-Majority-Inverter Graph* (XMG) schemes. The use of these strategies directly supports the capabilities of TIGFET technology [10].

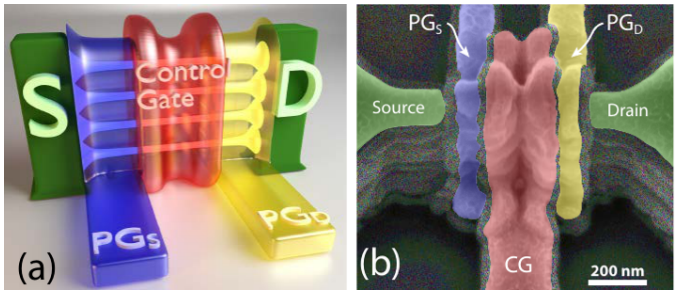

Fig. 1. **(a)** Conceptual sketch of a vertically-stacked nanowire TIGFET. **(b)** *Scanning Electron Microscope* (SEM) image of the fabricated device [12].

In this paper, we propose for the first time an open-source standard cell library using the 10 nm TIGFET technology node, featuring a full set of logic gates characterized for multiple stacked nanowires [11]. Using mixed logic synthesis software enabling the new XMG strategy, we show at circuit-level the advantage that only TIGFET structure functionality offer for XOR and MAJ functions. We evaluate the *Power, Performance and Area* (PPA) trade-offs of TIGFET technology compared to a 12 nm FinFET low-power technology, using standard combinational and sequential benchmarks, as well as a production RISC-V core.

The remainder of this paper is organized as follows: Section II introduces the unique TIGFET technology features, Section III details the standard cell integration methodology, Section IV discusses the mixed logic synthesis strategies, Section V presents results from synthesizing a set of benchmark circuits, and finally, Section VI concludes the paper.

II. TIGFET Devices

TIGFETs are made up of vertically stacked *Silicon Nanowires* (SiNW) surrounded by gate oxide acting as a semiconducting channel, metallic source/drain contacts and three independent gate electrodes: the *Polarity Gate at Source* (PG_S), the *Polarity Gate at Drain* (PG_D) and the *Control Gate* (CG), as presented in Fig. 1. The CG controls the potential barrier in the channel the same way as the gate of a conventional MOSFET and turns the device on or off. However, the

metal-semiconductor-metal structure forms Schottky barriers at the source and drain junctions, which PG_S, PG_D gates are capable to modulate these Schottky barriers [3]. Hence, these gates determining which carriers will enter the channel and control the current flow, enabling the device reconfigurability in terms of: (1) polarity, to switch between n-type or p-type dominance in the channel, and (2) threshold voltage, to achieve extremely low leakage current thanks to the Schottky barrier cut-off [13]. *Gate-All-Around* (GAA) structures in SiNW transistors give the ideal shape for effective electrostatic control and a favorable rise in I_{ON}/I_{OFF} [14]. These devices have been successfully fabricated for various geometry, with a single silicon nanowire [15], [16] and multiple stacked silicon nanowires [3].

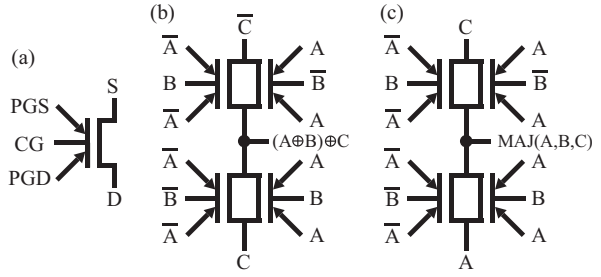

Fig. 2. (a) Symbol representation of a TIGFET device, (b) a three-input TIGFET XOR gate, and (c) a three-input TIGFET MAJ gate.

By changing the carrier dominance in the channel, a single TIGFET can reproduce a series of two transistors (where PG_S-PG_D and CG are control gates) providing the ability to implement compact logic gates. This device-level configurability gives the most benefit to: a 3-to-1 XOR gate (XOR3) and a Majority gate (MAJ3), only using four TIGFETs [13], [16], [17], as illustrated in Fig. 2. Moreover, this technology is capable of implementing a variety of compact logic gates, such as combinational logic cells (INV, NAND, NOR, XOR, XNOR) [18], sequential flip-flops (FF) [19], and 2-to-1 low-power multiplexer (MUX) [20]. Compact *AND-OR-INVERT* (AOI) gates can be achieved: a 2-1 AOI gate is implemented with four TIGFETs [21], and a 2-2 AOI gate with six TIGFETs [22]. TIGFETs have also been demonstrated as a high performance cells for resistive memory [23], in security systems for logic locking [24], and for arithmetic ripple-carry adder [5].

III. TIGFET Standard Cell Characterization

To evaluate TIGFET and FinFET technologies using commercial or open-source synthesis tools, we follow a *Design to Technology Co-Optimization* (DTCO) methodology [25], as proposed in Fig. 3. It aims to reduce the cost and time-to-market in the development of advanced technologies to circuit level by integrating premature physical model of transistors into standard cell structures, thus compatible with a conventional digital design flow. This methodology is split into three parts: (1) the modeling of the TIGFET device considering its physical dimensions, (2) the extraction of the wiring's

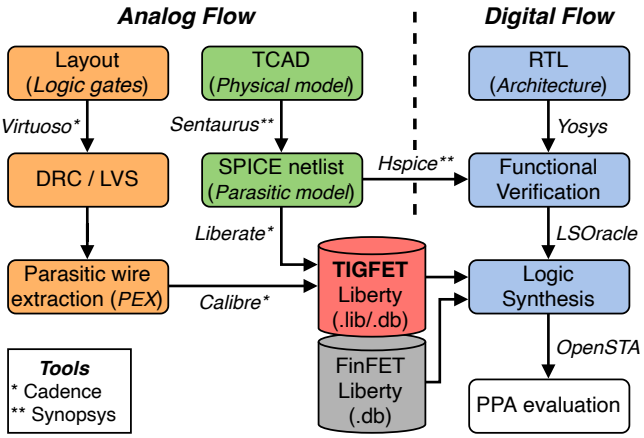

Fig. 3. Proposed mixed-design synthesis flow to evaluate 10 nm TIGFET and 12 nm FinFET technology nodes. TIGFET standard cells are characterized and mapped in a Liberty (.lib) database for analog-digital compatibility.

parasitics and area for each standard cell, (3) the evaluation of circuit performance according to their *Register-Transfer Level* (RTL) description, using AIG and XMG synthesis strategies.

A. Intrinsic Transistor Models

The TIGFET physics model is calibrated with *Technology Computer-Aided Design* (TCAD) Synopsys *Sentaurus* simulations [13], which provides ID-VGS curves stored in look-up tables (LUTs) at the operation voltage of VDD=0.7 V, while the transient behavior depending on the device geometry are extracted from multi-physic simulations [26]. To enable circuit-level simulations, these model are written in Verilog-A and SPICE netlists, for intrinsic electrical properties and parasitic capacitance models, respectively.

B. Standard Cell Layout Optimizations

We implement the layouts of combinational (AND, AOI, INV, MAJ, MUX, NAND, NOR, OAI, OR, XNOR, XOR) and sequential (DFF) standard cells using Cadence *Virtuoso*,

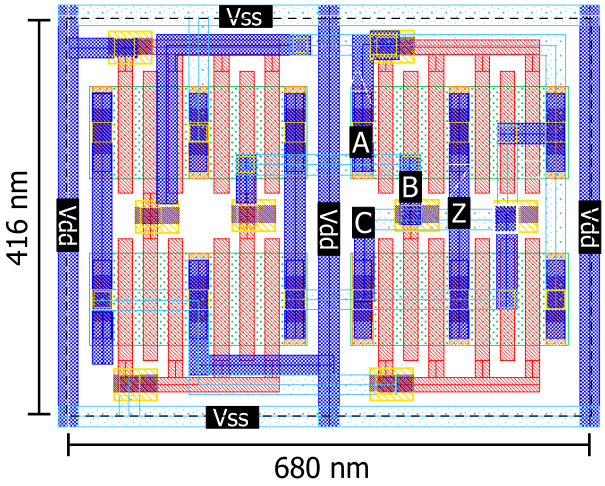

Fig. 4. Layout of the 10 nm TIGFET MAJ3 cell with 12 stacked nanowires.

as shown is Fig. 4. All layouts ensure correct cell spacing according to the *Design Rule Check* (DRC) and *Layout Versus Schematic* (LVS) rules defined by the 10 nm TIGFET predictive *Process Design Kit* (PDK) [5], and metal wire spacing of the *Back-End Of Line* (BEOL) according to the DRC of the *FreePDK15nm* [27]. Hence, metal layer parasitics are extracted (PEX) for each cell using Cadence *Calibre*, in order to increase the transient behavior reliability. Another advantage of the TIGFET layout is its symmetric logic cells that enable layout regularity. This in turn facilitates the design of an efficient regular layout tile, which we use to create circuit layout using a *Sea-of-Tiles* (SoT) design methodology [28]. This regularity provides the ability to optimize area, which translates into energy savings.

C. Logic Synthesis Integration

To ensure seamless integration with commercial and open-source synthesis tools, all proposed logic gates are characterized using Cadence *Liberate*, which generate the standard cell library in a *Liberty* (.lib) format, freely available in [11]. Benchmark circuits are synthesized and technology mapped using open-source *Yosys* [29] and *LSOracle* [30] tools. Finally, the PPA are evaluated for various number of nano-wires using static analysis in *OpenSTA*, as discussed in Sec. V.

IV. XOR-Majority Graph Strategy

The most well known representation for logic synthesis is the *AND-Inverter Graph* (AIG), which are *Directed Acyclical Graphs* (DAG) where each node represents the AND2 function, and edges represent fan-in and fan-out connections, which may be inverted. While an AIG is capable of representing any possible logical circuit, not all structures are easily represented. Of particular concern is the XOR gate, which can be represented by a minimum of four NAND gates. XOR typically represent the largest simple gate a technology node must implement, and are expensive in CMOS: in the GF12 technology the minimum voltage XOR2 gate has 3.5× the area and 6.6× the worst case leakage power compared to the minimum voltage inverter.

Beyond simple gates, a complete full adder can be represented by a minimum of nine NAND gates. The additional of more complex gates greatly simplifies the implementation. The XOR3 or parity function $A \oplus B \oplus C$ implements the sum function in a full adder, and the majority-of-three (MAJ3) function $(A \wedge B) \vee (B \wedge C) \vee (A \wedge C)$ implements the carry operation [4]. The addition of these gates forms the *Majority-Inverter Graph* (MIG), *XOR-AND-Inverter Graph* (XAG), and *XOR-Majority-Inverter Graph* (XMG). In addition to native representation, these DAGs also allow additional optimization techniques [7]. XAGs have been used to reduce the multiplicative complexity for security applications [31].

V. Benchmark Results

We evaluated the PPA of the 10 nm TIGFET technology node using a set of standard benchmark circuits. Results for the TIGFET node were compared with the *GlobalFoundries* (GF) 12 nm FinFET technology node. Benchmarks used were from the ISCAS'85 and EPFL'15 benchmarks [32], as well as PicoRV32 [33], a small RISC-V core. Benchmarks in the suites with less than 100 nodes were not considered to ensure sufficient complexity. Benchmarks with more than 25,000 nodes were also not considered due to runtimes.

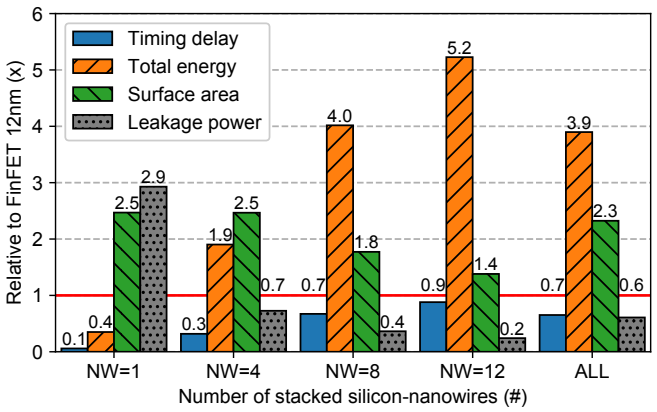

Fig. 5. Performance gains of the PicoRV32 circuit, synthesized with 10 nm TIGFET technology node for various stacked silicon-nanowires, normalized in comparison to a 12 nm FinFET implementation (using only AIG strategy).

A. Effect of the number of nanowires

The maximum number of vertically stacked nanowires is limited to four, in order to maintain an acceptable form factor of the pillars (Source/Drain pillars in Fig. 1). Thus, NW=1 and NW=4 cells are made up of one stack of nanowires, while NW=8 and NW=12 cells are implemented with two and three stacks respectively. Performance trade-offs of the TIGFET technology with regards to number of nanowires are demonstrated in the results for the PicoRV32 circuit, as shown in Fig. 5. In the final case (ALL), the synthesis tools use combinations of all four variations. Values are normalized to the FinFET technology, where values superior to 1 correspond to better performance for TIGFETs.

Leakage power and surface area increase as the number of nanowires increases, with a corresponding decrease in critical path delay. The leakage current and critical path delay show proportional relationships to the number of nanowires used. While surface area increases with the number of nanowires, the sea-of-tile structures still allow a significantly smaller cell surface dimensions compared to FinFET technology. TIGFET showed improved area performance for all nanowire configurations tested, with an average gain of 2.3× more compact design than FinFET technology.

For a single nanowire cell (NW=1), the leakage power achieves a gain of 2.9× compared to FinFET, thanks to the cutoff provided by the two Schottky barriers of the silicon nanowire [3]. This comes at the cost of a significant degraded critical path delay performance. To improve the delay and energy performance, the cells must exploit a higher number of nanowires. Increasing the number of nanowires to 12 improves the static energy performance up to 5.2× improvement, at a

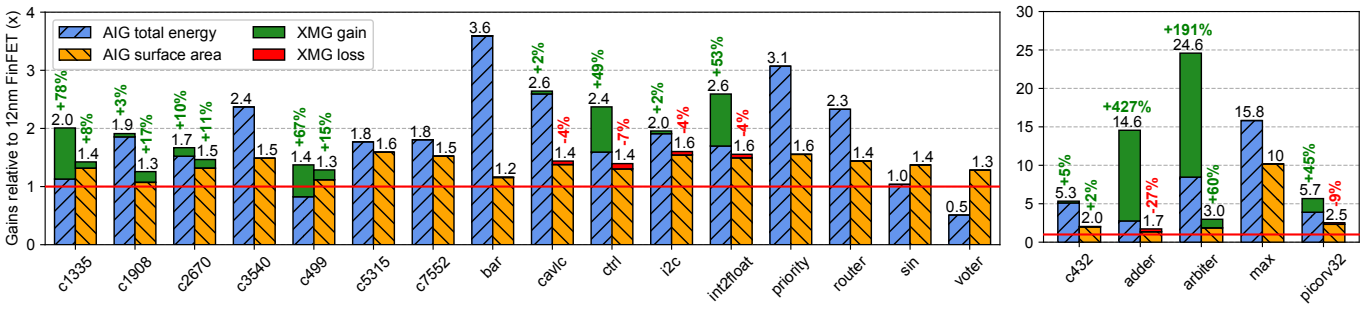

Fig. 6. (a) Total energy and surface area gains of 10 nm TIGFET synthesized circuits compared to the 12 nm FinFET implementations, using AIG or XMG strategy. Each value superior to 1 as better energy-efficiency than FinFET. (b) Addition results with significant improvements, shown on a larger scale.

cost of a critical path delay of 0.9×, compared to the FinFET (NW=12). Leakage current does increase significantly with additional nanowires, with worse results than FinFET for all cases above 1 nanowire.

Technology nodes offer multiple options for standard cells of a given gate function, with trade-offs between time, area, static, and dynamic energy consumption. When synthesized with a combination of all four sets of cells, we demonstrate an energy gain of 3.9× and a surface area gain of 2.3×, with only a 0.7× loss in critical path delay compared to FinFET (ALL). The library with the combined set of cells will be used in all following benchmarks.

B. Benefits of the AIG and XMG strategies

Of the 21 circuits evaluated, the TIGFET technology demonstrates improved energy performance in 19 circuits, improved surface area performance in all cases as shown in Fig. 6. The XMG optimizations are capable of significant improvements in energy, as demonstrated in the *adder* and *arbiter* circuits from the EPFL suite. The best results for energy gain where significantly enhanced with XMG synthesis with LSOracle in the case of The EPFL benchmarks. The circuits make heavy use of AOI and OAI gates in the case of TIGFETs. *Arbiter* yields significant delay reduction by eliminating a large number of buffers and inverters. *Adder* shows a large reduction in pre-tech-mapping depth, from 255 to 12, with a corresponding improvement in post-tech-mapping delay.

Comparing the performance of FinFET and TIGFET technologies using the AIG synthesis with ABC, on average the TIGFET technology node improves power by 2.81×, area by 1.51×, with a penalty in delay of 0.97×, as shown in table I. Thus, we evaluate the additional effects in performance that occur when using the LSOracle mixed synthesis tool. For the FinFET technology, synthesizing with LSOracle does cause some area and power penalty on average. Despite this penalty, on average it improves in power by 2.82×, area by 1.53 ×, with a penalty in delay of 0.87×. This is slightly improved in power and area over the use of ABC and the TIGFET technology, but with a larger penalty in delay.

TABLE I
AVERAGE IMPROVEMENT OVER FINFET OPTIMIZED WITH ABC.

	FinFET			TIGFET		
	Power	Area	Delay	Power	Area	Delay
ABC	1.0	1.0	1.0	2.81	1.51	0.97
LSOracle	0.88	0.92	1.00	2.82	1.53	0.87

VI. CONCLUSION

In this paper, we presented an open-source standard cell library using the 10 nm TIGFET technology node [11], offering seamless integration into digital synthesis flows. By combining TIGFET technology with a mixed synthesis strategy (AIG and XMG), targeting XOR and MAJ logic gate optimizations, the PicoRV32 core achieves a speed gain of 5.7× for a compact area of 2.3×, compared to an equivalent 12 nm FinFET implementation. This technology provides optimized logic gates that enable low-power circuit design. Due to the stacked silicon nanowire structure and the tradeoffs available between different numbers of nanowires, this provides opportunities for device selection during synthesis for improved PPA. For the PicoRV32 core, we demonstrated improved PPA by using a mix of devices of different numbers of nanowires, achieving high speed while preserving a small area. Finally, when evaluating the technological trade-offs of the proposed library to the low-power 12 nm FinFET library using standard synthesis techniques, the benchmarks show an average improvement of 2.8× in power, 1.51×, with an average penalty of 0.97× in delay. Although the application of an XMG synthesis strategy did not achieve the best results for all design circuits tested, it shows promising results, yielding the best gain of 24.6× for energy for the *arbiter* benchmark. Future work will seek to address and improve the capabilities of EDA tools to leverage the TIGFET technology.

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REFERENCES

[1] A. Razavieh, P. Zeitzoff, D. E. Brown, G. Karve, and E. J. Nowak, "Scaling challenges of FinFET architecture below 40nm contacted gate pitch," in *Device Research Conference (DRC)*, 2017.

[2] R. H. Dennard, F. H. Gaensslen, H. Yu, V. L. Rideout, E. Bassous, and A. R. LeBlanc, "Design of ion-implanted MOSFET's with very small physical dimensions," *IEEE Journal of Solid-State Circuits (JSSC)*, 1974.

[3] J. Zhang, M. De Marchi, D. Sacchetto, P.-E. Gaillardon, Y. Leblebici, and G. De Micheli, "Polarity-controllable silicon nanowire transistors with dual threshold voltages," *IEEE Transactions on Electron Devices (TED)*, 2014.

[4] J. Romero-González and P.-E. Gaillardon, "An Efficient Adder Architecture with Three- Independent-Gate Field-Effect Transistors," in *IEEE International Conference on Rebooting Computing (ICRC)*, 2018.

[5] G. Gore, P. Cadareanu, E. Giacomin, and P.-E. Gaillardon, "A Predictive Process Design Kit for Three-Independent-Gate Field-Effect Transistors," in *IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC)*, 2019.

[6] A. Mishchenko and R. Brayton, "Scalable logic synthesis using a simple circuit structure," *Proc. IWLS*, 2006.

[7] L. Amarú, P.-E. Gaillardon, and G. De Micheli, "Majority-inverter graph: A new paradigm for logic optimization," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, 2016.

[8] Z. Chu, M. Soeken, Y. Xia, L. Wang, and G. De Micheli, "Structural rewriting in XOR-majority graphs," in *ACM Asia and South Pacific Design Automation Conference ASP-DAC*, 2019.

[9] X. Ma and Y. Xia, "Power optimization based on dual-logic using and-xor-inverter graph," in *2017 IEEE 12th International Conference on ASIC (ASICON)*, 2017, pp. 351–354.

[10] P.-E. Gaillardon, L. G. Amaru, and G. De Micheli, "Unlocking controllable-polarity transistors opportunities by exclusive-OR and majority logic synthesis," in *IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*, 2014.

[11] Laboratory for Nano-Integrated Systems, "Open-source 10-nm TIGFET standard cell library." [Online]. Available: https://github.com/lnis-uofu/TIGFET-10nm-SCLIB

[12] P.-E. Gaillardon, R. Magni, L. Amarú, M. Hasan, R. Walker, B. S. Rodriguez, J.-F. Christmann, and E. Beigné, "Three-independent-gate transistors: Opportunities in digital, analog and rf applications," in *2016 17th Latin-American Test Symposium (LATS)*, 2016.

[13] P. Cadareanu and P.-E. Gaillardon, "A TCAD Simulation Study of Three-Independent-Gate Field-Effect Transistors at the 10-nm Node," *IEEE Transactions on Electron Devices*, 2021.

[14] A. Heinzig, S. Slesazeck, F. Kreupl, T. Mikolajick, and W. M. Weber, "Reconfigurable silicon nanowire transistors," *Nano Letters*, vol. 12, no. 1, p. 119—124, 2012.

[15] M. De Marchi, D. Sacchetto, S. Frache, J. Zhang, P.-E. Gaillardon, Y. Leblebici, and G. De Micheli, "Polarity control in double-gate, gate-all-around vertically stacked silicon nanowire FETs," *IEEE IEDM Tech. Dig.*, 2012.

[16] J. Zhang, M. De Marchi, P.-E. Gaillardon, and G. De Micheli, "A Schottky-barrier silicon FinFET with 6.0 mv/dec Subthreshold Slope over 5 decades of current," in *IEEE International Electron Devices Meeting (IEDM)*, 2014.

[17] T. Mikolajick, A. Heinzig, J. Trommer, T. Baldauf, and W. M. Weber, "The RFET—a reconfigurable nanowire transistor and its application to novel electronic circuits and systems," *Semiconductor Science and Technology*, 2017.

[18] J. Zhang, X. Tang, P.-E. Gaillardon, and G. De Micheli, "Configurable Circuits Featuring Dual-Threshold-Voltage Design With Three-Independent-Gate Silicon Nanowire FETs," *IEEE Transactions on Circuits and Systems I: Regular Papers*, 2014.

[19] D. Vana, P.-E. Gaillardon, and A. Teman, "C^2TIG: Dynamic C^2MOS Design Based on Three-Independent-Gate Field-Effect Transistors," *IEEE Transactions on Nanotechnology*, 2020.

[20] E. Giacomin, J. R. Gonzalez, and P.-E. Gaillardon, "Low-power multiplexer designs using three-independent-gate field effect transistors," in *2017 IEEE/ACM International Symposium on Nanoscale Architectures (NANOARCH)*, 2017, pp. 33–38.

[21] J. Trommer, A. Heinzig, T. Baldauf, S. Slesazeck, T. Mikolajick, and W. M. Weber, "Functionality-enhanced logic gate design enabled by symmetrical reconfigurable silicon nanowire transistors," *IEEE Transactions on Nanotechnology*, 2015.

[22] S. Rai, J. Trommer, M. Raitza, T. Mikolajick, W. M. Weber, and A. Kumar, "Designing efficient circuits based on runtime-reconfigurable field-effect transistors," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, 2019-03.

[23] A. Levisse, P.-E. Gaillardon, B. Giraud, I. O'Connor, J.-P. Noel, M. Moreau, and J.-M. Portal, "Resistive switching memory architecture based on polarity controllable selectors," *IEEE Transactions on Nanotechnology*, vol. 18, pp. 183–194, 2019.

[24] S. Rai, S. Patnaik, A. Rupani, J. Knechtel, O. Sinanoglu, and A. Kumar, "Security promises and vulnerabilities in emerging reconfigurable nanotechnology-based circuits," *IEEE Transactions on Emerging Topics in Computing*, 2020.

[25] G. Yeric, B. Cline, S. Sinha, D. Pietromonaco, V. Chandra, and R. Aitken, "The past present and future of design-technology co-optimization," in *Proceedings of the IEEE 2013 Custom Integrated Circuits Conference*, 2013, pp. 1–8.

[26] P. Cadareanu, J. Romero-Gonzalez, and P.-E. Gaillardon, "Parasitic Capacitance Analysis of Three-Independent-Gate Field-Effect Transistors," *IEEE Journal of the Electron Devices Society*, 2021.

[27] K. Bhanushali and W. R. Davis, "Freepdk15: An open-source predictive process design kit for 15nm finfet technology," in *ACM Symposium on International Symposium on Physical Design*, 2015.

[28] S. Bobba and G. De Micheli, "Layout technique for double-gate silicon nanowire fets with an efficient sea-of-tiles architecture," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, 2015.

[29] C. Wolf, "Yosys open synthesis suite." [Online]. Available: https://github.com/YosysHQ/yosys

[30] Laboratory for Nano-Integrated Systems, "LSOracle." [Online]. Available: https://github.com/lnis-uofu/LSOracle

[31] E. Testa, M. Soeken, L. Amarù, and G. De Micheli, "Reducing the multiplicative complexity in logic networks for cryptography and security applications," in *ACM Design Automation Conference (DAC)*, 2019.

[32] L. Amarù, P.-E. Gaillardon, and G. De Micheli, "The EPFL combinational benchmark suite," *International Workshop on Logic & Synthesis (IWLS)*, 2015.

[33] C. Wolf, "Picorv32 - a size-optimized risc-v cpu." [Online]. Available: https://github.com/cliffordwolf/picorv32