An Energy-Efficient Three-Independent-Gate FET Cell Library for Low-Power Edge Computing

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***Abstract*—With the increasing demand for compute-intensive applications for IoT devices, new technologies that enable a power reduction at the device-level are needed to improve energy savings at the system-level. Unfortunately, the scaling of standard CMOS technologies is not as fast as the scaling of computing performance, which leads to the so-called "power wall". The *Three-Independent-Gate Field-Effect Transistor* (TIGFET) is a promising technology that enhances the device functionality to create more compact logic gates and provide silicon-nanowire structures that meet the requirements of low leakage power systems. However, the evaluation of complex designs is currently limited to the intrinsic model of the transistor and does not consider the parasitic effects of cell layouts. In this paper, we propose a standard cell library for 10-nm silicon-nanowire TIGFET devices, including combinational and sequential gates, to evaluate a production RISC-V core targeting low energy consumption budget. After synthesis, the core achieves 4× lower energy consumption up to a frequency of 340 MHz compared to an equivalent low-power 12-nm FinFET technology node.**

***Index Terms*—Three-Independent-Gate FET, Standard Cell, Layout, Low-Power, Edge Computing.**

I. Introduction

Modern applications for *Internet of Things* (IoT) systems are becoming increasingly demanding in data traffic and computing workloads [1]. To reduce the energy consumption of the overall system, edge computing brings computing and data storage closer to the data sources. Such solutions have a limited energy budget to process compute-intensive tasks. At the same time, the incremental shrinkage of *Complementary Metal-Oxide-Semiconductor* (CMOS) transistors leads to an exponential increase in leakage currents, which limits the overall performance and its energy efficiency, also known as the "power wall" [2]. To address the edge computing challenges and further scaling devices, novel technology such as *Reconfigurable Field-Effect Transistors* (RFETs) provide enhanced functionalities to create more compact logic cells rather than only reducing the material dimensions.

For instance, the *Three-Independent-Gate Field-Effect Transistor* (TIGFET) provides two additional gates, called *Polarity Gates* (PGs), to configure the channel device between *n*-type and *p*-type depending on the PGs voltage biases [3]. This dynamic reconfiguration extends the logic behaviors of a single transistor, resulting in less surface area for complex cells, such as 3-to-1 XOR and Majority gates [4], [5]. Moreover, the channel is replaced by a *Silicon-Nanowire* (SiNW) providing lower leakage power consumption compared to standard CMOS technologies [6]. However, dimensional scaling for advanced technology nodes below 20 nm introduces additional parasitic effects and impacts circuit performance [7]. For SiNW-based devices, the parasitic contributions increase up to twice compared to CMOS due to the smaller capacitance between the gates and the channel [8], [9]. Since these studies focus on the intrinsic parasitics of the transistor, it is necessary to consider wire parasitics of the gate when gate-to-gate connections increase the input and output load capacitance.

In this paper, we propose a TIGFET-based standard cell library [10], that considers all parasitic effects from the intrinsic transistor model up to the gate-level wiring. This library provides a set of combinational and sequential logic gates allowing users to compare digital circuits to emerging and existing state-of-the-art technologies using the same digital design flow. In addition, this study provides a qualitative comparison to position the TIGFET devices among low-power technologies designed to meet the demands of edge computing applications. Thus, complex TIGFET gates provide a surface area gain up to 71% and an energy reduction of 92% compared to the *Global Foundries* (GF) 12 nm FinFET technology node. Comparing these technologies for a production RISC-V core, constrained to the same clock frequency up to 340 MHz, the energy saving of the TIGFET is 4× better.

The remainder of this paper is organized as follows: Section II introduces the TIGFET technology devices, Section III details the proposed standard cell design flow, Section IV presents gate-level analysis and synthesis results for low-power circuits, and finally, Section V concludes the paper.

II. Related Work

RFETs offer an alternative option to continue shrinking the size of transistors with novel materials, while reducing the number of devices in the circuit thanks to their reprogrammable operations. With their additional control gates, the polarity of a single RFET can be changed to dynamically switch from *p*-type to *n*-type, or even replicate a series of transistors, thus implementing more compact logic gates compared to CMOS devices. New 3D materials and geometries have been developed to reduce the leakage current and improve the electrostatic control of the channel using 2D *Fin Field-Effect Transistor* (FinFET) or 3D *Gate-All-Around* (GAA) structures [11]. Recent works have demonstrated low leakage current with different materials and geometries, including silicon-fins [12], single SiNW [3], [13], multiple stacked SiNWs [14], [15] and *Germanium-Nanowires* (GeNW) [16].

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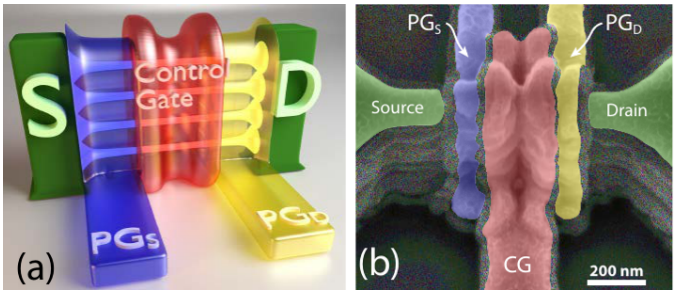

Fig. 1. (a) Conceptual sketch of a vertically-stacked SiNW TIGFET. (b) *Scanning Electron Microscopy* (SEM) image of the fabricated device [6]

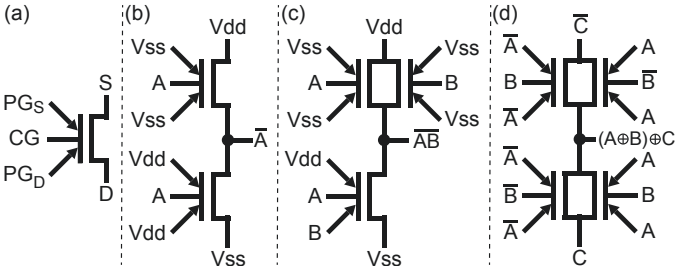

Fig. 2. (a) Symbol representation of a TIGFET device, (b) a 1-input inverter (INV) gate, (c) a 2-input NAND gate, and (d) a 3-input XOR gate.

A. TIGFET Devices

One type of RFET, the TIGFET, is a promising candidate due to its ability to implement complex logic cells using its three independent gate structure [5], [17]–[19]. As presented in Fig. 1, the TIGFET is composed of vertically stacked SiNWs surrounded by a gate oxide acting as a semiconducting channel, metallic source/drain contacts, and three gate electrodes: *Polarity Gate at Source* (PG_S), the *Polarity Gate at Drain* (PG_D), and the *Control Gate* (CG). The CG controls the potential barrier in the channel the same way as the gate of a conventional MOSFET. At the source and drain junctions, the metal-semiconductor-metal structure creates Schottky barriers, which the PG_S and PG_D gates are able to modulate [6]. Thus, these gates control the current flow to dynamically configure the device in terms of: (i) polarity, to switch between n-type or p-type dominance in the channel, and (ii) threshold voltage, to achieve ultra-low leakage current resulting from to the Schottky barrier cut-off [9]. In addition, multiple stacked SiNWs supply higher drive current to reduce propagation delays and improve device performance at the cost of higher static power. TIGFET devices with six stacked SiNWs have shown a 1.8× reduction in delays for half the leakage power on different circuits compared to CMOS technology [15].

B. TIGFET Operations and Logic Gates

The TIGFET device dimensions are technically larger than a CMOS transistor, but they are smaller when the TIGFET replaces a series of two transistors, an advantage of its reconfigurability. As shown is the Fig. 2(b), a 1-input TIGFET inverter requires the same amount of transistors as its CMOS counterpart, but a 2-input NAND gate (Fig. 2(c)) saves one transistor by replicating two transistors in its lower part. This reconfigurability feature is more advantageous for complex gates, whereas a 3-input CMOS XOR requires 20 transistors, a TIGFET implementation requires only 10 transistors, including all complementary states, as illustrated in Fig. 2(d). In the literature, other circuit opportunities have been demonstrated when implementing combinational logic gates, such as INV1, NAND2, NOR2, XOR2, XOR3, AOI21, MAJ3 gates [4], [17], 2-to-1 multiplexer [18], sequential logic gates, such as flip-flop (DFFQ1) and latch (LATQ1) [19], and a 1-bit full adder [5]. Since these works do not address trade-offs of multiple stacked SiNWs and gate-level parasitics, this work proposes a TIGFET standard cell library for accurate circuit evaluations.

III. TIGFET Standard Cell Design Flow

As shown in Fig. 3, the proposed design flow methodology is organized into five main steps: (1) design of the cell layout, (2) *Design Rule Check* (DRC), (3) *Layout Versus Schematic* (LVS), (4) *Parasitic Extraction* (PEX), and (5) Liberty file generation. A similar methodology has been proposed in [20], so this work focuses on the physical design optimization of compact TIGFET logic gates through two main optimization loops. The first loop Ⓐ aims at minimizing the cell area while considering the cost of parasitics, thanks to the advanced structures *Sea-of-Tiles* (SoT) [15], [21], [22] which ensure a compact area for SiNW-based logic gates and to the support of the TIGFET DRC, as established in [5]. The second loop Ⓑ ensures the correct implementation of each cell by matching the pin function between layout and the schematics through the LVS step. Then, all parasitics from the wire resistance and capacitance and the TIGFET device itself are extracted in the PEX step to generate a cell description in SPICE format. Finally, these files are provided to the Cadence Liberate for characterizing all cells in terms of delays, static and dynamic powers to generate a Liberty file format, a standard used by conventional *Electronic Design Automation* (EDA) tools.

A. Physical Layout

Cells are created by placing TIGFETs and adding contacts to connect the devices. Next, connections between devices are made using metal layers, and finally, *Vdd* and *Vss* rails apply voltage biases to the devices. The remaining internal cell connections are derived from the device operation.

1) Device Placements and Contacts: TIGFETs are placed using a SoT design structure with equivalent source and drain terminals overlapping to avoid unnecessary wiring between the terminals. The SoT design organizes devices to have equivalent CGs opposing and inline, and connects them using the gate layer. This work adapts SoTs to reflect the TIGFET layouts used in this study by aligning PGs instead of the CGs. Fig. 4 shows the layout of the low and high fan-out devices used to create the cells. Low and high fan-out cells have the same width and only the height changes to accommodate the two additional SiNW stacks in the high fan-out cell. Then, source and drain contacts and gate contacts are placed to connect devices with metal wires.

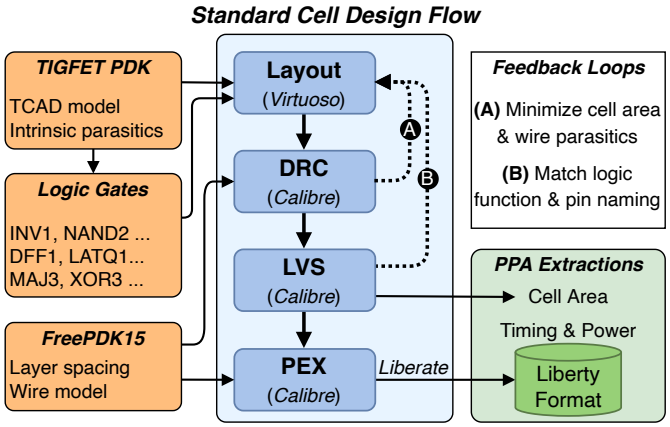

Fig. 3. Design flow and methodology to evaluate TIGFET cell *Performance, Power and Area* (PPA) using Cadence (*Virtuoso*, *Liberate*) and Mentor Graphics (*Calibre*) EDA tools.

2) Metal Connections: Metal connections are made between source and drain and gate contacts to connect the devices, and to minimize the area of the cell. The metal layer M1 is used until it is no longer possible without overlapping with itself. Similarly, the metal layer M3 is used when connections with the metal layer M2 are not feasible. None of the cells in the library require more than three metal layers. Metal connections are checked in the DRC step to confirm layouts are compliant with PDK rules that ensure a realistic chip fabrication with acceptable parasitic effects.

3) Power Rail Considerations: *Vdd* and *Vss* rails are added to the cell. The rails supply voltages to the source, drain, CGs, and PGs to configure the device type. Rails also allow for a single *Vdd* and *Vss* pin in the layout, as required by the tool to run the LVS, and create a more accurate cell layout when generating the parasitic model. The rails reflect the parasites of the cell involved in a current drop, which makes them necessary when evaluating TIGFETs at the circuit level where many rails are used throughout the circuit.

Due to the additional PGs, it is not possible to place the rails exclusively above and below the cell, so the rails are placed around the cell, as shown in Fig. 5. Furthermore, rails are not placed around the entire cell but only where devices require *Vdd* and *Vss* connections to minimize the usage and parasitic effects of the rails. As shown in Fig. 5, the complete layout of the INV1 is a simple cell and does not require any metal layers to connect devices. However, the NAND2 uses M1 and M2, and the XOR3 uses all three metal layers. The XOR3 is one of the most complex cells in the library and shows that G4 and G2 SoT layouts provide compact design at the expense of additional wiring.

B. Design Rule Check (DRC)

Cells have to satisfy the DRC to ensure minimal parasitic effects between TIGFET devices and wires being placed too close in the physical layout. The DRC for the devices and contacts is adapted from the proposed TIGFET PDK [5] to

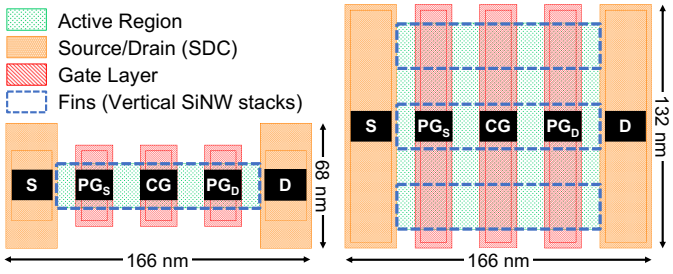

Fig. 4. Layouts of low (left) and high (right) fan-out TIGFET devices. The high fan-out device is made of 3 fins to support a total of 12 stacked SiNWs.

reflect the updated device layouts. Additional rules are added from FreePDK15 [23] to consider constraints for metal layers M1, M2, and M3. The DRC verification is performed by the Calibre nmDRC tool, which is integrated into Virtuoso. Layouts are fixed by iterations until all constraints are satisfied, as described in loop Ⓐ of Fig. 3.

C. Layout Versus Schematic (LVS)

Cells need to pass the LVS to verify connections between source, drain, and gate contacts are the same as described in the schematic. The LVS also verifies that the pin names in the layout match the names used in the simulations that evaluate and characterize the cell. To perform the LVS, the Calibre nmLVS tool extracts the netlist representation from the schematic and the layout of the cell and compares both netlists. Similar to the DRC step, cells are fixed by iteration until passing the LVS, as described in loop Ⓑ of Fig. 3.

D. Parasitic Extraction (PEX)

Once a cell passes the LVS, the parasitic model of the cell can be extracted from the layout. A set of PEX rules derived from FreePDK15 [23] defines the material properties, such as the conductivity and sheet resistance, of each layer. These properties and the cell layout determine the parasitic effects of contacts and wiring in the cell, while the TCAD model and the Verilog-AMS parasitic description of the TIGFET describe the intrinsic parasitics of the device [8], [9]. The Calibre PEX tool uses the PEX rules and cell layout to perform the extraction of capacitances and resistances of the cell to produce a PEX SPICE file. Thus, this SPICE model includes the parasitic effects of contacts, wiring and intrinsic parasitics of the device, resulting in a more accurate model of the TIGFET cells.

E. Cell Characterization

Since SPICE simulations are slow due to a continuous time measurement of all parasitics, Cadence's Liberate tool is used to characterize the cells to create a discrete representation for faster simulations. The generated file is a Liberty-based format compatible with all commercial and open-source EDA tools [10]. As a result, this design flow methodology enables large TIGFET-based circuits to be evaluated and compared to other technologies implemented with equivalent timing constraints for accurate evaluation of the TIGFET technology.

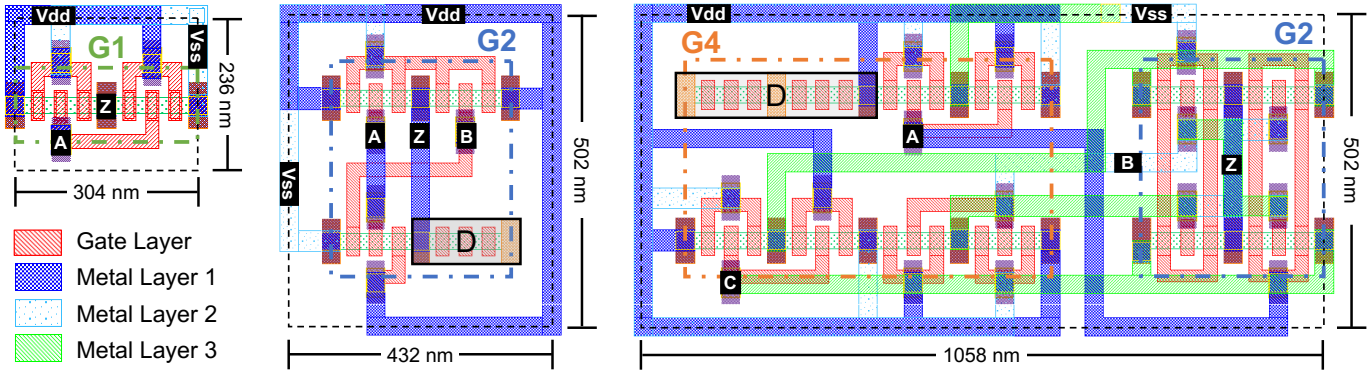

Fig. 5. Physical cell layouts of a 1-input inverter, 2-input NAND, and 3-input XOR gates (from left to right) using low fan-out TIGFET devices. These gates are using sea-of-tile layouts (G1, G2, and G4 zones) [22] ensuring more compact designs. The D areas correspond to the dummy cells.

IV. Experimental Results

Following the proposed design flow in Section III, 17 gates are implemented using the 10 nm TIGFET PDK [5], for three different fin structures. In these experimental results, the low *Fan-Out* (FO) cells refer to a single SiNW and the high FO cells refer to 12 stacked SiNWs distributed on three fins, as discussed earlier. As shown in Table I, gates are categorized in three classes according to layout gate complexities.

TABLE I
Logic gates available in the standard cell library.

Simple Gates			Complex Gates		Sequential Gates
INV1	BUF1	MUX2	AOI21	OAI21	DFFQ1
AND2	OR2	XOR2	XOR3	XNOR3	LATQ1
NAND2	NOR2	XNOR2	MIN3	MAJ3	

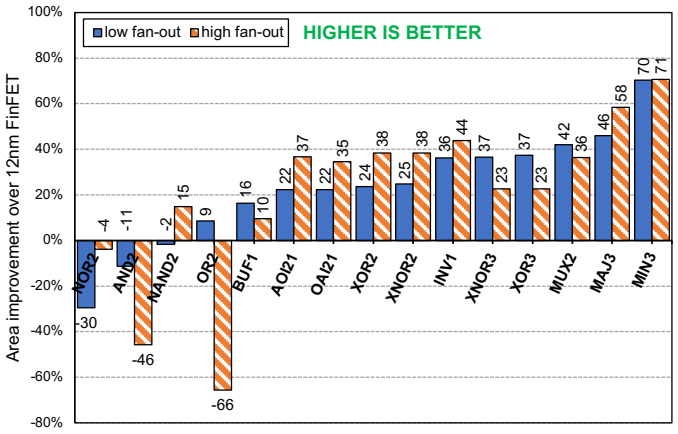

Fig. 6. Gate surface area compared to 12 nm FinFET for low/high fan-outs.

A. Evaluation Methodologies

First, the *Performance, Power, and Area* (PPA) of individual logic gates are evaluated through SPICE simulations using their respective PEX netlists. These results are compared to industry standard cells from the GF 12 nm FinFET technology node using a FO factor of X1 and X2 for low and high FO cells respectively. Since 3-input majority (MAJ3) and minority (MIN3) gates are missing from the FinFET library, three NAND2 and one NAND3 gates are assembled to implement the majority logic function, whereas three NAND2 and one AND3 gates are used for the minority logic function. Their total surface area result is the sum of the constituent gates.

Second, the generated Liberty library format compatible with EDA tools is used to synthesize complete circuits, thus reducing the simulation time. The PicoRV32 [24] core design is synthesized with the *Synopsys* DesignCompiler tool for 12 nm FinFET and 10 nm TIGFET technology nodes. This digital flow translates the behavior of the circuit using all logic gates with 1, 4, 8, and 12 stacked SiNWs while minimizing the overall power consumption at a given clock frequency.

B. Gate Area Dimensions

The area dimensions of each TIGFET logic gates are compared to the FinFET technology, as shown in Fig. 6. The low FO TIGFET gates require less area than the FinFET except for the AND2, NAND2, and NOR2. The simple gates require relatively few transistors and mainly benefit from technology shrinking. However, complex gates also benefit from the unique reconfigurability of the TIGFET devices to achieve more compact design, such as the MAJ3 and MIN3 gates that save up to 46% and 70% area respectively.

The high FO TIGFET gates follow a similar trend where the complex gates have greater area-savings than simple gates, and the TIGFET requires less area than the FinFET except for NOR2, AND2, and OR2. The BUF1 and NAND2 area improvements are less than 20% of the same FinFET gate. Identical to the low FO gates, more complex high FO gates have greater area improvements meaning an area-saving trade-off also exists for high FO gates. The high FO MIN3 and MAJ3 improve the most, similar to the low FO gates. The MIN3 and MAJ3 cells require 71% and 58% less area than FinFET, respectively.

The area trade-off shows TIGFETs require less area for complex gates when reconfigurability can optimize a circuit design. Simple gates, such as INV1, are already compact gates and have minimal wiring, meaning that gates cannot be optimized with reconfigurability. The area improvement in simple gates comes from the technology used in the TIGFET

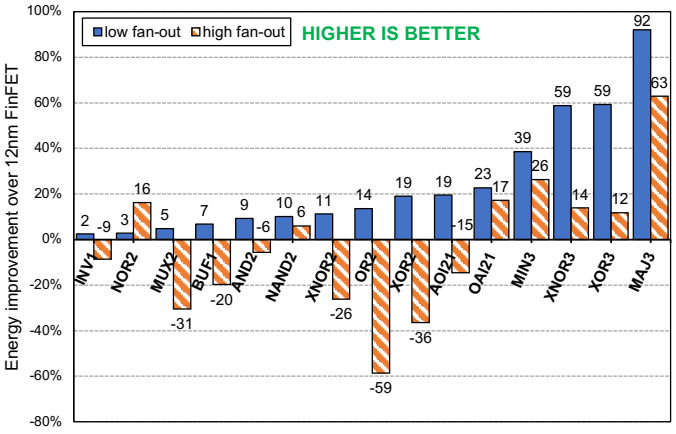

Fig. 7. Gate energy consumption compared to 12 nm FinFET for low/high fan-outs (FOs). Output loads are set at 40 fF (low-FO) and 80 fF (high-FO).

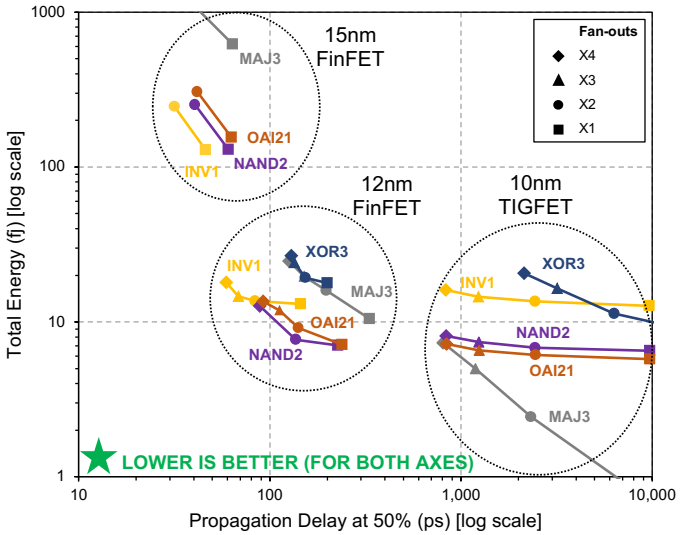

Fig. 8. Timing delay and energy trade-off of sub-20 nm technology nodes for a set of gates and fan-outs with the same capacitance load of 50 fF.

and not from the device properties. However, complex gates can benefit from reconfigurability more than the technology node, and we observe a sizable area reduction compared to FinFET technology.

C. Gate Energy Consumption

As shown in Fig. 7, each TIGFET gate energy consumption is compared with FinFET according to low and high FO gates. For a fair energy comparison between these technologies, the gates drive an output load capacitance of 40 fF and 80 fF for the low and high FO, respectively.

The low FO gates require less energy than the FinFET implementation in all cases. The SiNW material set has a low leakage power making dynamic energy the dominant factor of the gate power consumption. Similar to the TIGFET area, complex gates achieve better performance due to their reduced transistor numbers, a result of the device reconfigurability. The MAJ3 gate achieves an energy reduction of 93% compared to FinFET. Simple gates, such as INV1 and AND2, have relatively little improvement at 2% and 9%, respectively. The simple gates do not benefit from reconfigurability, and their dynamic energy consumption is similar to FinFET, so the overall relative dynamic energy consumption is not better than FinFET. Gates that benefit from reconfigurability can be implemented using fewer transistors than FinFETs, so the relative dynamic energy consumption is lower. Thus, the relative total energy consumption is lower for complex gates that benefit from reconfigurability.

The high FO gates require more energy than FinFETs for most of the gates. Seven gates require less energy than FinFETs, and only two show an improvement greater than 20%. The high FO TIGFETs consume more energy than FinFETs due to their additional SiNWs, which increase their leakage power and have a higher impact on total energy consumption than the low FO gates. Complex gates still benefit from reconfigurability and a lower relative dynamic energy consumption, but the leakage power from the high FO device becomes dominant and reduces the benefits of reconfigurability.

D. Technology Trade-off between Delay and Energy

The trade-off between delay and total energy for INV1, OAI21, XOR3, and MAJ3 gates for different FO factors, is shown is Fig. 8. Delay is dependent on the output capacitance and the number of SiNWs in the device. FO-X4 devices can provide more current which reduces the time for an input signal to propagate through the circuit. The TIGFET has approximately 10× the delay of 12 nm FinFET. The overall worse delay for the TIGFET can be attributed to its material set and geometry. Schottky barriers at each PG create additional barriers for carriers and result in a slower device [9]. While the TIGFET gates are slower, the total energy consumption is less compared to 12 nm FinFET and 15 nm FinFET [23]. The TIGFET being slower but consuming less energy highlights the trade-off between performance and energy consumption. This analysis places the TIGFET technology as an ideal candidate for low-power applications where reduced performance is acceptable due to high energy constraints.

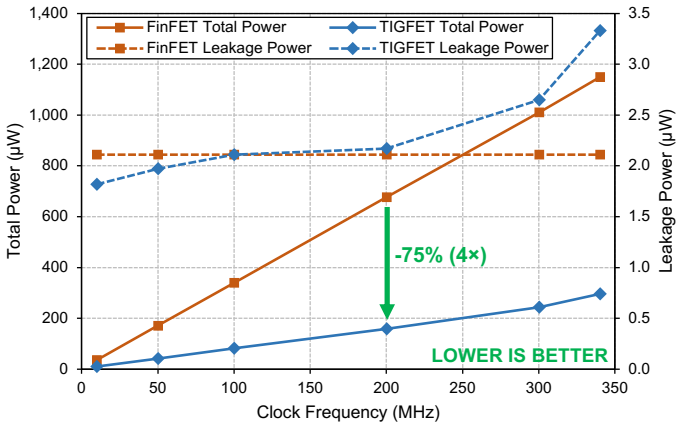

Fig. 9. Total power (left axis) and leakage power (right axis) results of 12 nm FinFET and 10 nm TIGFET after synthesis of the PicoRV32 [24] constrained for various operating clock frequencies.

E. Synthesis Results under Timing Constraints

To assess the benefits of TIGFET technology at the system-level, a production RISC-V core is synthesized under strict design constraints to meet the demands of low-power edge computing applications. As presented in the Fig. 9, average total power and leakage power are extracted with Synopsys PrimeTime Power tool when the PicoRV32 [24] core is running a simple user application for a given clock frequency. As expected, the 10 nm TIGFET achieves an average energy consumption reduction of 4× over the 12 nm FinFET on the clock frequency range from 10 MHz to 340 MHz. For a 100 MHz clock frequency, both TIGFET and FinFET circuits consume a leakage power of 2.1 μW, but the TIGFET outperforms the FinFET implementation with a total energy consumption of 81.3μW. However, beyond the frequency of 340 MHz, the synthesis of the TIGFET circuit fails to meet the setup timing due to slow gate propagation delays. This effect can also be observed in the static power consumption, which becomes 58% higher at 340 MHz compared to FinFET, due to the increased use of 12 stacked SiNW gates to meet the constraints.

V. Conclusion

In this paper, we introduced an open-source standard cell library [10] using the 10 nm TIGFET technology node, considering all wiring parasitic effects up to the gate-level implementation to enable the design of low-power circuits for edge computing applications. Simple, complex, and sequential gates were designed using the proposed design flow methodology while integrating the 10 nm TIGFET PDK and all previous work on TIGFET-based cells. Thanks to the unique TIGFET device-level reconfigurability, most logic gates offer up to 71% area reduction over advanced FinFET technology node for low and high fan-out structures. However, because the silicon-nanowire channel achieves a low leakage power consumption due to its Schottky barrier, the current is not high enough to achieve the same timing performance as FinFET technologies. Nevertheless, the total power consumption of a production RISC-V core is 4× better than its FinFET implementation at a clock frequency up to 340 MHz, thus satisfying the performance requirements for edge computing applications.

Acknowledgements

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References

[1] W. Yu, F. Liang, X. He, W. G. Hatcher, C. Lu, J. Lin, and X. Yang, "A Survey on the Edge Computing for the Internet of Things," *IEEE Access*, 2018.

[2] R. H. Dennard, F. H. Gaensslen, H. Yu, V. L. Rideout, E. Bassous, and A. R. LeBlanc, "Design of ion-implanted MOSFET's with very small physical dimensions," *IEEE Journal of Solid-State Circuits (JSSC)*, 1974.

[3] M. De Marchi, D. Sacchetto, S. Frache, J. Zhang, P.-E. Gaillardon, Y. Leblebici, and G. De Micheli, "Polarity control in double-gate, gate-all-around vertically stacked silicon nanowire FETs," *IEEE IEDM Tech. Dig.*, 2012.

[4] J. Romero-González and P.-E. Gaillardon, "An Efficient Adder Architecture with Three- Independent-Gate Field-Effect Transistors," in *IEEE International Conference on Rebooting Computing (ICRC)*, 2018.

[5] G. Gore, P. Cadareanu, E. Giacomin, and P.-E. Gaillardon, "A Predictive Process Design Kit for Three-Independent-Gate Field-Effect Transistors," in *IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC)*, 2019.

[6] J. Zhang, M. De Marchi, D. Sacchetto, P.-E. Gaillardon, Y. Leblebici, and G. De Micheli, "Polarity-controllable silicon nanowire transistors with dual threshold voltages," *IEEE Transactions on Electron Devices (TED)*, 2014.

[7] J. Zou, Q. Xu, J. Luo, R. Wang, R. Huang, and Y. Wang, "Predictive 3-D Modeling of Parasitic Gate Capacitance in Gate-all-Around Cylindrical Silicon Nanowire MOSFETs," *IEEE Transactions on Electron Devices*, 2011.

[8] P. Cadareanu, J. Romero-Gonzalez, and P.-E. Gaillardon, "Parasitic Capacitance Analysis of Three-Independent-Gate Field-Effect Transistors," *IEEE Journal of the Electron Devices Society*, 2021.

[9] P. Cadareanu and P.-E. Gaillardon, "A TCAD Simulation Study of Three-Independent-Gate Field-Effect Transistors at the 10-nm Node," *IEEE Transactions on Electron Devices*, 2021.

[10] Laboratory for Nano-Integrated Systems (LNIS), "Open-source 10-nm TIGFET standard cell library." [Online]. Available: https://github.com/lnis-uofu/TIGFET-10nm-SCLIB

[11] Y. Cui, Z. Zhong, D. Wang, W. U. Wang, and C. M. Lieber, "High Performance Silicon Nanowire Field Effect Transistors," *Nano Letters*, 2003.

[12] G. V. Resta, Y. Balaji, D. Lin, I. P. Radu, F. Catthoor, P.-E. Gaillardon, and G. De Micheli, "Doping-Free Complementary Logic Gates Enabled by Two-Dimensional Polarity-Controllable Transistors," *ACS Nano*, 2018.

[13] A. Heinzig, S. Slesazeck, F. Kreupl, T. Mikolajick, and W. M. Weber, "Reconfigurable silicon nanowire transistors," *Nano Letters*, 2012.

[14] J. Zhang, M. De Marchi, P.-E. Gaillardon, and G. De Micheli, "A Schottky-barrier silicon FinFET with 6.0 mv/dec Subthreshold Slope over 5 decades of current," in *IEEE International Electron Devices Meeting (IEDM)*, 2014.

[15] S. Bobba, P.-E. Gaillardon, J. Zhang, M. De Marchi, D. Sacchetto, Y. Leblebici, and G. De Micheli, "Process/design co-optimization of regular logic tiles for double-gate silicon nanowire transistors," in *IEEE/ACM International Symposium on Nanoscale Architectures (NANOARCH)*, 2012.

[16] J. Trommer *et al.*, "Enabling energy efficiency and polarity control in germanium nanowire transistos by individually gated nanojunctions," *ACS NANO*, 2017.

[17] J. Zhang, X. Tang, P.-E. Gaillardon, and G. De Micheli, "Configurable Circuits Featuring Dual-Threshold-Voltage Design With Three-Independent-Gate Silicon Nanowire FETs," *IEEE Transactions on Circuits and Systems I: Regular Papers*, 2014.

[18] E. Giacomin, J. R. Gonzalez, and P.-E. Gaillardon, "Low-power multiplexer designs using three-independent-gate field effect transistors," in *IEEE/ACM International Symposium on Nanoscale Architectures (NANOARCH)*, 2017.

[19] D. Vana, P.-E. Gaillardon, and A. Teman, "C^2TIG: Dynamic C^2MOS Design Based on Three-Independent-Gate Field-Effect Transistors," *IEEE Transactions on Nanotechnology*, 2020.

[20] R. Gauchi, A. Snelgrove, and P.-E. Gaillardon, "An open-source three-independent-gate fet standard cell library for mixed logic synthesis," in *IEEE International Symposium of Circuits and Systems (ISCAS)*, 2022.

[21] S. Bobba, M. De Marchi, Y. Leblebici, and G. De Micheli, "Physical synthesis onto a Sea-of-Tiles with double-gate silicon nanowire transistors," in *ACM Design Automation Conference (DAC)*, 2012.

[22] S. Bobba and G. De Micheli, "Layout technique for double-gate silicon nanowire fets with an efficient sea-of-tiles architecture," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, 2015.

[23] K. Bhanushali and W. R. Davis, "Freepdk15: An open-source predictive process design kit for 15nm finfet technology," in *ACM International Symposium on Physical Design (ISPD)*, 2015.

[24] C. Wolf, "Picorv32 - a size-optimized risc-v cpu." [Online]. Available: https://github.com/cliffordwolf/picorv32