2022 21st IEEE Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems (iTherm) | 978-1-6654-8503-6/22/$31.00 ©2022 IEEE | DOI: 10.1109/iTherm54085.2022.9899595

# Device-level Transient Cooling of β-$Ga_2O_3$ MOSFETs

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***Abstract* — β-phase gallium oxide (β-$Ga_2O_3$) has garnered considerable attention due to its large critical electric field strength and the availability of low cost/high quality melt-grown substrates, both of which are advantages over silicon carbide (SiC) and gallium nitride (GaN) in terms of the development radio frequency (RF) and power switching devices. However, because of the low thermal conductivity of β-$Ga_2O_3$, thermal management strategies at the device-level are required to accomplish the targeted high power operation. Recent package- and system-level thermal management studies have shown that design solutions based on steady-state operation could lead to ineffective cooling performance under transient thermal loading conditions, and result in an overdesigned cooling system. For these reasons, we performed a comparative study of the thermal dynamics of β-$Ga_2O_3$ and GaN based transistor devices, which sheds light on the design of device-level transient cooling solutions for β-$Ga_2O_3$ metal-oxide-semiconductor field-effect transistors (MOSFETs). Results show that replacing the host β-$Ga_2O_3$ substrate with a high thermal conductivity material, similar to device-level thermal management solutions established for GaN devices, is effective in terms of heat extraction from the device active region under direct current (DC) operating conditions, but not under high frequency power dissipating conditions beyond the ~$10^2$ kHz range. In order to cool lateral β-$Ga_2O_3$ MOSFETs under transient pulse-powered conditions, additional topside heat extraction via a high thermal conductivity passivation overlayer is necessary.**

***Keywords—Gallium oxide (β-$Ga_2O_3$), MOSFET, Raman spectroscopy, self-heating, transient thermal management, thermal modeling***

## I. Introduction

β-phase gallium oxide (β-$Ga_2O_3$) is an ultra-wide bandgap (UWBG) semiconductor that offers outstanding electronic properties and potentially low manufacturing cost, that are both necessary to develop next-generation high power electronic devices. The large bandgap energy (~4.8 eV) translates into a high breakdown electric field (~8 MV/cm), leading to a high Baliga's figure of merit (BFOM) and Johnson's figure of merit (JFOM), that render the material ideal for high-voltage/power switching devices as shown in Table 1 [1]–[4]. For example, recent reports have demonstrated the development of depletion mode lateral metal-oxide-semiconductor field-effect transistors (MOSFETs), with a high critical field strength (3.8 MV/cm) [5], high current density (600 mA/mm) [6], and high breakdown voltage (2.32 kV) [7]. However, β-$Ga_2O_3$ possesses a poor thermal conductivity as compared to other wide band gap semiconductors (e.g., GaN and SiC), as shown in Table 1. Therefore, β-$Ga_2O_3$ devices suffer from device self-heating under nominal operating conditions [8]–[12]. Also, the low anisotropic thermal conductivity of β-$Ga_2O_3$ (9 – 26 W/m-K at room temperature) [13] leads to excessively high operational channel temperatures that compromise the device performance and reliability. Therefore, the design of thermal management solutions with highest cooling performance is critical for the commercialization of β-$Ga_2O_3$ device technologies.

Table 1. Electronic and thermal properties of semiconductors used to construct radio frequency (RF) and power switching devices [14]–[16].

| Material Property | Si | 4H-SiC | GaN | β-$Ga_2O_3$ |
|---|---|---|---|---|
| Bandgap (eV) | 1.1 | 3.25 | 3.4 | 4.6-4.9 |
| Breakdown field (MV/cm) | 0.3 | 3 | 3.3 | 8 |
| Normalized BFOM | 1 | 320 | 860 | 1100 - 3250 |
| Normalized JFOM | 1 | 8.2 | 22.9 | 37.5 |
| Density ($g/m^3$) | 2.33 | 3.21 | 6.15 | 6.44 |
| Specific heat (J/kg-K) | 710 | 670 | 490 | 490 |
| Thermal diffusivity ($m^2/s$) | 9.1e-5 | 2.3e-4 | 4.3e-5 | 4.1e-6 |
| Thermal conductivity at 300 K (W/m-K) | 135 | 490 | 130 | 26 [010]<br>13 [001]<br>9 [100] |

Package- and system-level thermal management solutions, that are designed based on steady-state operation, were shown to be often ineffective for applications that operate under transient thermal loading, and could result in overdesigned cooling systems [17]. Since the practical operation of RF and

power electronic devices involve pulsed power dissipation, it is necessary to consider the device transient thermal dynamics when designing device-level cooling solutions. In this study, we investigated the effectiveness of different device-level cooling schemes applied to a β-$Ga_2O_3$ MOSFET under transient operating conditions. The device thermal time constant ($\tau$) [18]–[20] (the rise time for a device to reach ~63% of its steady-state temperature in response to a power step input) [21] is inversely proportional to the thermal diffusivity ($\alpha$), i.e., $\tau \propto 1/\alpha = \rho c_p/\kappa$, where $\rho$ is the density, $c_p$ is the specific heat at constant pressure, and $\kappa$ is the thermal conductivity. Since the thermal conductivity of β-$Ga_2O_3$ is an order of magnitude lower than those for GaN and SiC, the thermal diffusivity is an order of magnitude lower as well (Table 1). This renders β-$Ga_2O_3$ transistors to possess a significantly longer thermal time constant than those for GaN and SiC devices. Because of this relatively long thermal time constant, the heat diffusion length in β-$Ga_2O_3$ is limited under short transient thermal loading; therefore, device-level thermal management solutions established for GaN devices [22] may not be applicable to β-$Ga_2O_3$ devices, especially under high frequency operating conditions that involve switching power losses. This study builds upon our recent reports on the growth of polycrystalline diamond on β-$Ga_2O_3$ [23] and the fabrication of β-$Ga_2O_3$ composite substrates [24]. As a follow-up study, this work highlights key considerations for the design of transient cooling solutions for high power β-$Ga_2O_3$ electronic devices using transient thermal modeling.

## II. Device Description

The steady-state and transient self-heating behavior of the β-$Ga_2O_3$ MOSFET was compared to experimental results for a GaN-on-Si high electron mobility transistor (HEMT) acquired from our previous work [25], [26]. Fig. 1 (a) shows the cross-sectional schematic of a single channel β-$Ga_2O_3$ MOSFET tested in this work. A Si-doped β-$Ga_2O_3$ channel layer was grown on a Fe-doped (010)-oriented β-$Ga_2O_3$ commercial substrate using metal organic vapor phase epitaxy (MOVPE). The channel length is 2.5 µm, where the gate length is 0.5 µm and the gate–drain length is 2 µm. The gate width is 100 µm. More fabrication details, including the gate metal stack and ion-implant conditions/activation can be found in [25]. A GaN HEMT was grown on a Si substrate, which consisted of a 10 nm in situ $SiN_x$ passivation layer, a 4 nm GaN cap layer, a 24 nm AlGaN barrier layer, a 514 nm GaN layer, and a 4.4 µm GaN buffer layer. The GaN HEMT has a gate length of 2 µm, a gate width of 100 µm, a gate-to-source spacing of 2 µm, and a gate-to-drain spacing of 15 µm. More details of this device can be found in [27].

Based on the experimental data acquired from our previous thermal characterization studies on the homoepitaxial β-$Ga_2O_3$ MOSFET (Fig. 1 (a): option 1) [16], [25], [28], a transient device thermal model was created. This model was then extended to study a hypothetical β-$Ga_2O_3$ device fabricated on a β-$Ga_2O_3$/diamond composite substrate (Fig. 1 (b): option 2) and another device structure that also employs a polycrystalline diamond passivation layer grown on top of the β-$Ga_2O_3$ channel (Fig. 1 (c): option 3). The β-$Ga_2O_3$/diamond composite wafer is assumed to be constructed by bonding a 6.5 µm-thick β-$Ga_2O_3$ layer thinned from the host substrate (similar to our previous work [14]) onto a polycrystalline diamond substrate with a thickness of 350 µm. For these simulated device structures, the device geometries (gate-to-source distance, gate length, gate-to-drain distance) were kept identical to the homoepitaxial MOSFET.

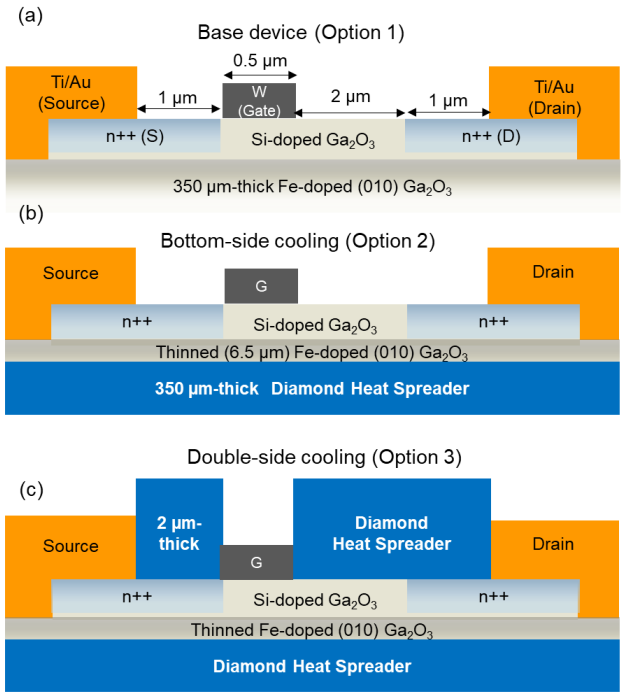


Fig. 1 (a) Option 1: Schematic of a homoepitaxial β-$Ga_2O_3$ MOSFET. (b) Option 2: A simulated device structure with the host substrate replaced by a β-$Ga_2O_3$/diamond composite wafer. (c) Option 3: A simulated device that further augments the device architecture in (b) by depositing a polycrystalline diamond heat spreader over the β-$Ga_2O_3$ channel layer.

## III. Experimental and Modeling Details

To experimentally quantify the transient temperature rise of the channel of the homoepitaxial β-$Ga_2O_3$ MOSFET (option 1), micro-Raman spectroscopy measurements were performed using a Horiba LabRAM HR Evolution spectrometer with a 532 nm excitation source [26]. Measurements were performed in a 180° backscattering configuration with a long working distance 50 × objective (NA = 0.45). Nanoparticle-assisted Raman thermometry was used to probe the surface temperature of the β-$Ga_2O_3$ MOSFET using anatase titanium dioxide ($TiO_2$) nanoparticles (99.98% purity) deposited on the device surface [29]. The spatial resolution is dictated by the size of sub-micrometer nanoparticles serving as surface temperature transducers. The experimental setup used for transient Raman thermometry experiments is illustrated in Fig. 2 (a). This setup adopts a lock-in modulation scheme, in which the electrical and laser pulse trains are synchronized while the Raman signal accumulates over many periods. Using this experimental setup, a temporal resolution of 15 ns was achieved and used in this study. Fig. 2 (b) shows the synchronized pulsing scheme that allows to control the electrical pulse width ($\tau_{on}$) of the applied drain-source voltage ($V_{DS}$) and the laser pulse width ($\tau_{laser}$) that produces a Raman signal, which is collected by the detector of

the Raman system. The time delay ($\tau_{delay}$) between the electrical and laser pulses is controlled by a digital delay generator to measure the full transient temperature rise of the device in response to a square electrical pulse with a 10% duty cycle. Thermoreflectance thermal imaging was performed on the gate electrode of a GaN-on-Si HEMT using a Microsanj NT-210B system equipped with a 1626 × 1236 charge coupled device (CCD) camera. Experiments were carried out with a 20 × objective (NA =0.35) with 530 nm LED [26]. Temperature rise was measured at 1.6 W/mm under 10 kHz pulsed (10% duty cycle) conditions [26].

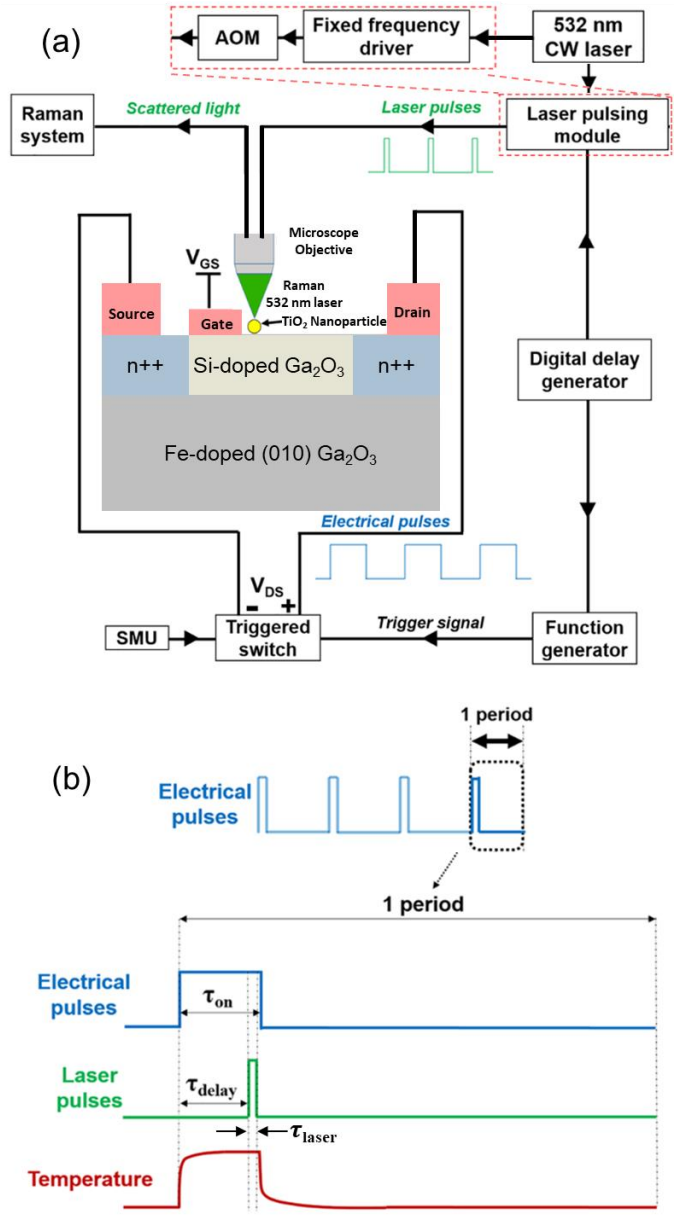


Fig. 2 (a) Experimental setup used for transient Raman Thermometry. (b) The synchronized pulsing scheme used to capture the transient thermal response of the β-$Ga_2O_3$ MOSFET.

In order to validate the trends observed in the experiments and to further understand the device transient thermal dynamics, a 3D transient device thermal model was constructed (using COMSOL Multiphysics). The β-$Ga_2O_3$ MOSFET and GaN HEMT were operated under a fully open channel condition [16], [28], [30], [31] by keeping the gate voltage at 4 V. Under such bias condition, the Joule-heating profile across the device channel could be approximated as a uniform heat flux that is applied between source and drain [32]. In the device model, the temperature dependence (~$1/T^{1.3}$ dependence) as well as the anisotropy of the thermal conductivity of β-$Ga_2O_3$ were accounted for as shown in Table 1 [33]. Also, a temperature dependent specific heat was used in the model [34]. A temperature boundary condition ($T_{bottom}$ = 25°C) was applied to the bottom of the device substrate, and a convective boundary condition (h = 5 W/$m^2$-K, $T_{inf}$ = 25°C) was applied elsewhere. The thermal conductivity of the polycrystalline diamond substrate (part of the composite wafer in Fig. 1 (b)) was 1940 W/m-k at room temperature [35]. For the diamond passivation layer (in Fig. 1 (c)), a directionally averaged thickness dependent thermal conductivity of high quality/large grain polycrystalline diamond (0-0.25 μm: 110 W/m-K, 0.25-1 μm: 240 W/m-K, 0.25-1 μm: 660 W/m-K) and a recently published thermal boundary conductance value at the β-$Ga_2O_3$/diamond interface (179 MW/$m^2$-K) were used in the device thermal model [23], [24], [36]. The transient thermal model for the GaN HEMT was constructed in a similar manner. A GaN/Si interfacial thermal boundary conductance of 10 MW/$m^2$-K was used in the GaN HEMT thermal model [27]. In Fig. 3, simulated channel surface temperatures are compared with the experimental data obtained from nanoparticle-assisted Raman thermometry showing excellent agreement.

## IV. Results and Discussion

Fig. 3 (a) shows the transient temperature rise of both the homoepitaxial β-$Ga_2O_3$ MOSFET and the GaN-on-Si HEMT under 1 W/mm and 1.6 W/mm power dissipation levels, respectively. Under steady-state, the β-$Ga_2O_3$ MOSFET exhibits a 2.7 × higher temperature rise than the GaN HEMT despite the β-$Ga_2O_3$ MOSFET is operating under a ~38% lower power density. The corresponding device-to-package thermal resistances of the β-$Ga_2O_3$ MOSFET and the GaN HEMT are 65 °C-mm/W and 15 °C-mm/W, respectively. To interrogate and compare the device transient dynamics, Fig. 3 (a) is replotted as Fig. 3 (b), where the channel temperature rise of both devices are normalized with respect to their steady-state temperature rise. Obviously, as shown in Fig. 3 (b), the GaN device exhibits a shorter thermal time constant than the homoepitaxial β-$Ga_2O_3$ MOSFET, which means its channel temperature reaches the steady-state value much faster than the β-$Ga_2O_3$ device.

To estimate the channel temperature rise in the four device architectures under a realistic power dissipation level, device simulation was performed at a power dissipation level of 4 W/mm, and results are plotted in Fig. 4. Today's GaN devices typically operate under 5–6 W/mm to ensure that the operating temperature does not exceed the safe allowable range for reliable operation [22]. Without any cooling solution applied, the steady-state channel temperature rise of the homoepitaxial β-$Ga_2O_3$ MOSFET (option 1) is 278°C (i.e., the channel temperature is 303°C while the base temperature is 25°C), which exceeds typical operational safety limits (e.g., 175°C for GaN and 125°C

for Si devices) [20], [37]. Because of the low thermal conductivity of β-$Ga_2O_3$, replacing the β-$Ga_2O_3$ substrate with diamond (option 2) reduces the steady-state channel temperature rise by 65% (dropping from 278°C to 97.5°C). However, the red and purple lines (simulation results for the homoepitaxial β-$Ga_2O_3$ MOSFET and the MOSFET fabricated on a β-$Ga_2O_3$/diamond composite wafer) in Fig. 4 show that, for high frequency power switching applications operating beyond the ~$10^2$ kHz range (elapsed time < ~$10^{-5}$ s), employing a composite substrate (i.e., bottom-side cooling) does not improve the transient thermal response (i.e., self-heating) of the device. The channel temperature rise for both device structures are identical up to ~$2\times10^{-6}$ s, which corresponds to transient thermal loading under ~500 kHz. Therefore, solely relying on a bottom-side cooling strategy (i.e., employing a composite substrate similar to the case of GaN-on-diamond devices [22]) is insufficient for the thermal management of pulse-powered β-$Ga_2O_3$ MOSFETs.

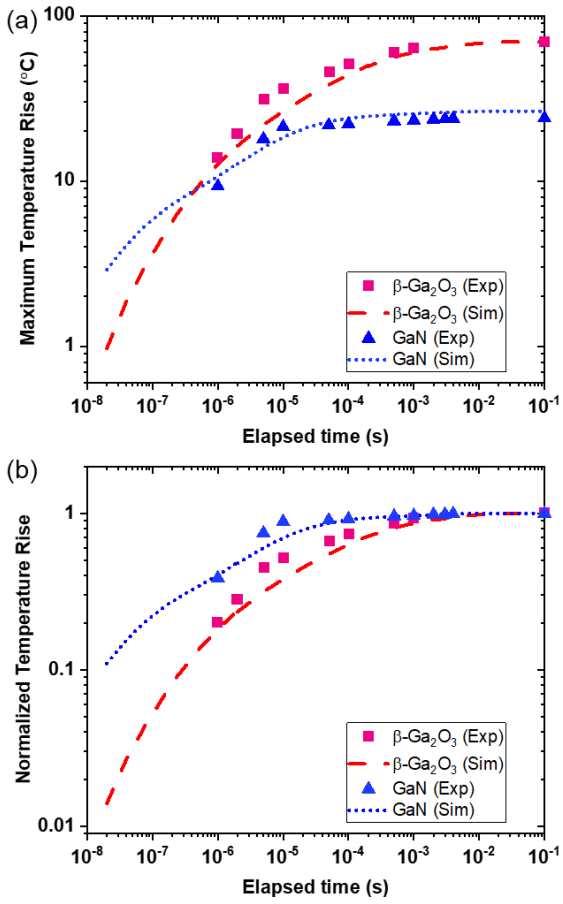


Fig. 3 (a) Experimental data obtained from nanoparticle-assisted Raman thermometry and thermoreflectance imaging along with simulated results for the β-$Ga_2O_3$ MOSFET and GaN-on-Si HEMT that were operated under 1 W/mm and 1.6 W/mm power dissipation levels, respectively. (b) Normalized temperature rise of the β-$Ga_2O_3$ MOSFET and GaN-on-Si HEMT with respect to their steady-state temperature rise. The steady-state temperature rise of the β-$Ga_2O_3$ MOSFET is 65°C for a power dissipation level of 1 W/mm. The steady state temperature rise of the GaN-on-Si HEMT is 24°C for a power dissipation level of 1.6 W/mm.

Fig. 4 shows the transient thermal response of a β-$Ga_2O_3$ MOSFET augmented by not only the β-$Ga_2O_3$/diamond composite wafer, but also a 2 μm-thick polycrystalline diamond passivation layer over the device channel (i.e., option 3), as shown in Fig. 1. The steady-state temperature rise of this double-side cooled device is 19.7°C under 4 W/mm, which is even lower than that for the GaN-on-Si HEMT, 105.5°C. Also, the addition of a top-side heat spreader (i.e., diamond passivation) effectively reduces the temperature rise during short transient conditions (e.g., elapsed time < ~$10^{-5}$ s). The diamond passivation layer with a moderately high thermal conductivity effectively reduces the device temperature not only under steady-state conditions, but also under the high frequency operating regime, since it is located in proximity (i.e., less than several tens of nanometers) to the β-$Ga_2O_3$ device active region, where Joule heating occurs. Therefore, device-level thermal management of β-$Ga_2O_3$ MOSFETs requires the combined use of a composite wafer and a top-side heat spreader, in order to cope with thermal loading that occurs during both direct current (DC; steady-state) and pulsed (transient) operating conditions.

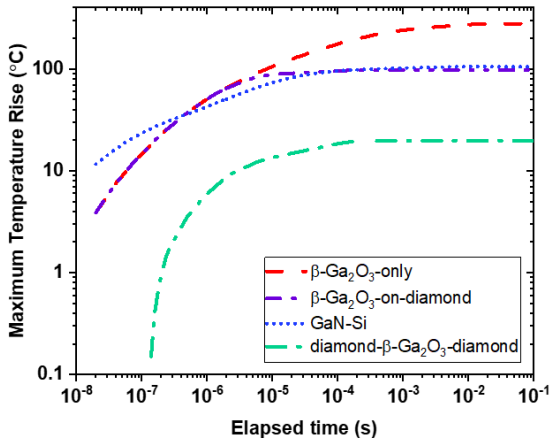


Fig. 4 The transient channel temperature rise under a power density of 4 W/mm for a homoepitaxial β-$Ga_2O_3$ MOSFET (option 1: β-$Ga_2O_3$-only), a β-$Ga_2O_3$ MOSFET fabricated on the composite substrate (option 2: β-$Ga_2O_3$-on-diamond), a β-$Ga_2O_3$-on-diamond MOSFET further augmented by diamond passivation (option 3: diamond-β-$Ga_2O_3$-diamond), and a GaN-on-Si HEMT.

## V. Conclusion

In this study, we compared the transient self-heating behavior of a homoepitaxial β-$Ga_2O_3$ MOSFET and a GaN-on-Si HEMT using nanoparticle-assisted Raman thermometry and thermoreflectance thermal imaging. The effectiveness of bottom-side and double-side cooling schemes using a polycrystalline diamond substrate and a diamond passivation layer were studied via transient thermal modeling. Because of the low thermal diffusivity of β-$Ga_2O_3$, the use of a β-$Ga_2O_3$ composite substrate (bottom-side cooling) must be augmented by a diamond passivation layer (top-side cooling) to effectively cool the device active region under both steady-state and transient operating conditions. Without no proper cooling applied, the steady-state device-to-package thermal resistance

of a homoepitaxial β-$Ga_2O_3$ MOSFET is 2.6 times higher than that for a GaN-on-Si HEMT. Replacing the substrate with polycrystalline diamond (under a 6.5 μm-thick β-$Ga_2O_3$ layer) could reduce the steady-state temperature rise by 65% compared to that for a homoepitaxial β-$Ga_2O_3$ MOSFET. However, for high frequency power switching applications beyond the ~$10^2$ kHz range, bottom-side cooling (integration with a high thermal conductivity substrate) does not improve the transient thermal response of the device. Adding a diamond passivation over layer diamond not only suppresses the steady-state temperature rise, but also drastically reduces the transient temperature rise under high frequency operating conditions.

## ACKNOWLEDGMENT

This work was supported by the National Science Foundation under Grant No. CBET-1934482 (Program Director: Ying Sun).

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