Thermally-Aware Layout Design of β-Ga_2O_3 Lateral MOSFETs

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***Abstract*— β-phase gallium oxide (β-Ga_2O_3) is drawing significant attention in the power electronics field due to its remarkable critical electric field strength [greater than gallium nitride (GaN) and silicon carbide (SiC)] and the availability of high-quality melt-grown substrates providing the opportunity for low-cost manufacturing. However, because of the low thermal conductivity of β-Ga_2O_3, thermal management strategies at the device-level are required to achieve the targeted high-power capabilities. In this work, the effects of the anisotropic thermal conductivity of β-Ga_2O_3 and the geometrical design of the metal electrodes/interconnects on the device self-heating were investigated. For a power density (P_{dis}) of 1 W/mm at $V_{GS} = 4$ V (i.e., a fully open channel condition), when the channel width is along a direction perpendicular to ($\bar{2}01$), the channel temperature decreases by 10% as compared to a case aligning the channel length along the direction close to [100]. Also, by decreasing the width of the interconnect between the drain electrode and the metal bond pad (serving as a heat pathway) from 100 to 10 μm (90% reduction), the channel temperature increased by ~8% for $P_{dis} = 1$ W/mm. Last, for devices with identical heat generation profiles, increasing the distance between the gate and drain contact from 1 to 10 μm, results in a 35% increase in the channel temperature rise. This work highlights the importance of thermally aware device layout design for lateral β-Ga_2O_3 transistors, in terms of maximizing both the electrical and thermal performance.**

***Index Terms*— Electro-thermal modeling, gallium oxide, MOSFET, nanoparticle-assisted Raman thermometry, self-heating, thermal characterization.**

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I. Introduction

β-PHASE gallium oxide (β-Ga_2O_3) is an ultrawide bandgap (UWBG) semiconductor that gives promise to the development of next-generation power electronic devices. The bandgap energy of β-Ga_2O_3 (4.6–4.9 eV [1]–[3]) is larger than that of wide bandgap (WBG) materials silicon carbide (SiC) and gallium nitride (GaN). This UWBG material is expected to tolerate high breakdown fields of 6–8 MV/cm, which translates to an outstanding Baliga's figure of merit (BFOM; ~10× higher than 4H-SiC vertical devices) and lateral figure of merit (LFOM; ~3.6× higher than GaN lateral devices) [4]–[7]. In addition, β-Ga_2O_3 exhibits excellent thermal and chemical stability. These favorable attributes of β-Ga_2O_3 give promise to the production of low-loss power switching devices with large breakdown voltage and potentially allow for high-temperature and deep space operation [8], [9]. In addition, high-quality and low-cost melt-grown β-Ga_2O_3 substrates provide opportunities to fabricate low-cost transistors with high-performance, addressing concerns related to the manufacturing cost of SiC and GaN devices [10]. However, a major drawback of β-Ga_2O_3 is its poor thermal conductivity, which results in devices with unacceptably high junction-to-package thermal resistance [11]–[16]. Experimental studies show that the thermal conductivity of β-Ga_2O_3 is highly anisotropic, where values along different crystallographic directions fall in the range of 11–26 W/m · K at room temperature [17]. This range of thermal conductivities is an order of magnitude lower than those for SiC and GaN.

Recently, several experimental and computational studies have reported self-heating mitigation strategies for β-Ga_2O_3 transistors. The effectiveness of bottom-side cooling methods (substrate engineering and microchannel cooling) and top-side cooling methods (air-jet impingement cooling and flip-chip hetero-integration) has been demonstrated [12]. In addition, the transfer of thin β-Ga_2O_3 membranes onto a high thermal conductivity diamond substrate has also been demonstrated [18], [19]. An improvement of both electrical and thermal performance by replacing the 200-μm-thick β-Ga_2O_3 substrate with a 50-μm-thick Cu substrate has been proposed [20]. It should be noted that these pioneering studies have focused on thermal management strategies that rely upon engineering solutions that add upon or alter the homoepitaxial configuration of β-Ga_2O_3 transistors.

In contrast, this work investigates how the device layout design of a homoepitaxial β-Ga_2O_3 MOSFET itself could be optimized to enhance the device's thermal performance. To be more specific, many device engineers are currently building their Ga_2O_3 devices based on device mask layouts they have been using for previous device development (e.g., GaN transistors), because guidelines for such thermally aware devices design is lacking in the open literature. The impact of two design parameters was studied by modeling and experiments: 1) orientation of the channel width and 2) geometrical design of the metallization structures. To investigate the effect of the in-plane anisotropy of the thermal conductivity of (010)-oriented β-Ga_2O_3 substrates, MOSFETs with various channel orientations (rotated by 0°/30°/60°/90°) were fabricated and characterized. Electro-thermal device simulation was performed to quantify the orientation-dependence of the device self-heating behavior, isolated from effects from the metallization structure arrangement. After this, to exclusively study the cooling effect arising from the metallization layout, electrically identical (identical heat source profile under a given bias condition) but thermally different (different gate–drain contact spacing) devices were fabricated and tested via nanoparticle Raman thermometry and infrared (IR) thermography.

II. Device Preparation

Fig. 1(a) shows the device's cross-sectional schematic. A 65-nm thick Si-doped β-Ga_2O_3 channel layer was grown on a 680-μm thick Fe-doped (010)-oriented β-Ga_2O_3 substrate using metal-organic vapor phase epitaxy (MOVPE). The device fabrication process started with depositing 200 nm of SiO_2 by plasma-enhanced chemical vapor deposition (PECVD) which acted as the gate dielectric as well as an implant cap.

A tungsten (W) refractory metal layer was sputtered and patterned with a chromium (Cr) hard mask to define a 2.5-μm W/Cr gate electrode using an SF_6 reactive ion etch (RIE) chemistry. A refractory metal gate is crucial to the self-aligned process because an Au-based gate metal stack would not survive at the required implant activation temperature of greater than 900 °C. Si-implant regions were then patterned with the source-side of the W/Cr gate ($L_G = 0.5$ μm, $W_G = 100$ μm) exposed to eliminate the gate–source region ($L_{GS} = 0$ μm), while the gate–drain distance (e.g., $L_{GD} = 2$ μm) remained. A shallow Si-implant profile was designed with 10- and 35-keV energies with a total dose of 1×10^{15} ions cm^{-2} to achieve a target doping concentration of 1×10^{20} cm^{-3}. The Si-implant was activated at 900 °C for 120 s using rapid thermal annealing (RTA) in N_2 ambient. Ohmic contacts over the implanted regions were achieved with a Ti/Al/Ni/Au evaporated metal stack followed by a 470 °C RTA process for 1 min in an N_2 ambient, after removing the implant cap via RIE. Electrical isolation was achieved using inductively coupled plasma/reactive ion etching. The Ti/Au gate and interconnect metals were added for device characterization. From transmission line measurements of the implanted material, the average sheet resistance across the sample was 1.9 kΩ/sq. From Hall measurements using a Van der Pauw structure consisting of the nonimplanted epitaxial material, the sheet resistance of the channel was 11.3 kΩ/sq. The average contact resistance across the sample was

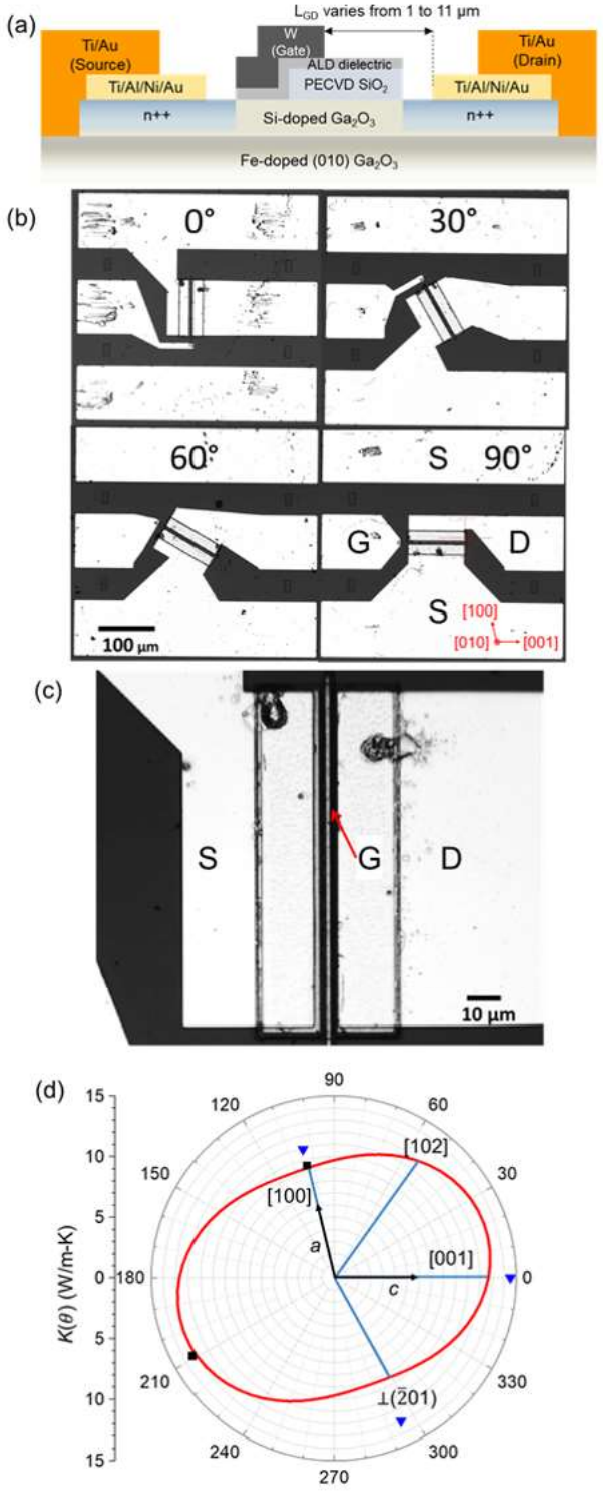

Fig. 1. (a) Schematic cross-section of the β-Ga_2O_3 MOSFET. (b) Charge-coupled device (CCD) image of four different rotational MOSFETs with different in-plane orientations. The top-left device is denoted as a 0° device. (Similarly, top-right device: 30° device, bottom-left: 60° device, and bottom-right: 90° device.) (c) Enlarged CCD image of 0° device showing the gate, source, and drain electrodes. (d) Directional dependence of the in-plane thermal conductivity of a (010) β-Ga_2O_3 substrate at room temperature. The red curve and square data points are from Jiang *et al.* [22], and the triangles are from Guo *et al.* [17].

1.2 $\Omega \cdot$ mm. More fabrication details, including the gate metal, implant conditions, and implant activation can be found in [21]. For the orientation dependence study, the gate and the interconnect metal were rotated by 30°/60°/90°. To be more specific, the channel width of the baseline device [heretofore to be called as a 0° device; Fig. 1(c)] was oriented along a direction close to [100]. Three additional devices were fabricated with the gate metal rotated counterclockwise by 30°, as shown in Fig. 1(b). Fig. 1(d) depicts that the highest in-plane thermal conductivity is along a direction between [102] and [001], which is close to the direction perpendicular to $\perp(\bar{2}01)$ direction. The lowest in-plane thermal conductivity is close to the [100] direction [22]. To study the cooling effect by metal contact arrangement, "electrically identical but thermally different" devices were fabricated. Specifically, the length of the Si-implant region was kept at 2.5 μm for all devices (i.e., identical effective channel length for electron transport), while the distance between the gate and drain metal contacts was varied from 1 to 11 μm.

III. Experiments and Simulation

To compare the surface temperature of the fabricated devices, IR thermography and nanoparticle-assisted Raman thermometry were utilized. A Quantum Focus Instruments (QFI) medium wavelength IR (MWIR) InfraScope with a 15× objective was used to perform qualitative thermal imaging [23]. To perform quantitative temperature measurements of gate, drain, and source metal electrodes, anatase (TiO_2) nanoparticles (99.98% purity) were deposited on the devices and micro-Raman thermometry was performed using a Horiba LabRAM HR Evolution spectrometer. This method allows probing the surface temperature of both metal electrodes and the semiconductor channel without complications associated with thermo-elastic stress effects, depth averaging, and the slow thermal transient response of β-Ga_2O_3 devices [12], [24]–[27].

3-D coupled electro-thermal modeling was performed to evaluate the orientation-dependent self-heating effect, isolated from other effects such as different levels of heat dissipation caused by the dissimilar metal electrode arrangement of fabricated devices [refer to Fig. 1(b)]. Briefly, electro-thermal modeling was done by coupling a 2-D electrical model (Synopsys Sentaurus TCAD software) with a 3-D finite element thermal model (COMSOL Multiphysics) with a detailed solid geometry that represents that of a real device, i.e., the 0° device in Fig. 1(c). This coupled modeling process is outlined in detail in our previous publications [13], [28], [29].

Then, to exclusively study the effect of device orientation on the self-heating, simulation was performed with no metallization structures on the device surface. This is because the four devices fabricated to study the orientation-dependent self-heating employed interconnects with different geometry [Fig. 1(b)], where the heat extraction occurs through the bond wires. Such geometrical differences made it difficult to quantify the orientation-dependent self-heating behavior isolated from geometrical effects through experiments. After this, the effect of interconnecting geometry on the heat dissipation was studied by simulating varying widths of the interconnect [W_{hp} = 10–100 μm as shown in Fig. 4(c)], acting as a heat pathway toward the bond pad, and monitoring the change in the channel temperature rise. Finally, to study the cooling effectiveness exclusively arising from the location of the drain metal contact with respect to the gate edge, nanoparticle-assisted Raman thermometry was performed on the "electrically identical but thermally different" devices with varying gate–drain distances (L_{GS}) of 1, 6, and 11 μm.

IV. Results and Discussion

DC I–V curves were generated for all devices at room temperature. Fig. 2(a) shows the measured and simulated I–V characteristics of the baseline (0°) device. The channel temperature of the devices with different channel orientations was measured under fully open channel conditions (gate–source voltage, V_{GS} = 4 V) as shown in Fig. 2(b) and (c). Fig. 2(c) shows the identical I–V characteristics of the four devices with different orientations under fully open channel conditions. The orientation-dependent difference in the current and ON-resistance among these devices is negligible. These bias conditions were used to minimize alteration of the heat generation profile arising from different voltage bias conditions required to operate the devices at an identical power level [30]. Fig. 2(d) and (e) show how bias conditions can affect the Joule heating profile for an identical P_{dis}. Under a fully open channel condition (V_{GS} = 4 V, V_{DS} = 6.5 V), a relatively uniform heat generation profile forms between source to drain, whereas localized Joule heating occurs near the gate under partially open (or pinched-off) channel conditions (V_{GS} = −4 V, V_{DS} = 14 V).

Fig. 3(a) shows the temperature rise at the gate metallization of the four devices illustrated in Fig. 1(b), measured by nanoparticle-assisted Raman thermometry for two different power dissipation levels: 0.75 and 1 W/mm. Also shown are the modeling results of the gate surface temperature where the nanoparticles were located. IR thermography images are included as insets to qualitatively visualize the orientation-dependent self-heating effect. The 0° and 30° devices exhibited lower channel temperatures among the four devices. The IR images also confirm these results. It should be noted that all of the device models used to derive results in Fig. 3(a) employed the geometry of the metallization structures for the 0° device. For this reason, there are discrepancies between the experimental and simulation results for the 30°, 60°, and 90° devices. In other words, the geometrical effect of the top metal structures on the device self-heating behavior was not isolated from the orientation-dependent effects.

Fig. 3(b) shows the simulated channel temperature rise as a function of different channel orientations. The simulation only accounts for the orientation dependence because other variables such as metallization structures are excluded from the device model. The 30° device exhibits the lowest channel temperature rise among all the possible channel orientations. This is because the thermal conductivity along the channel length is the highest [this direction is close to the direction perpendicular to $\perp(\bar{2}01)$ direction as shown in Fig. 1(b) and (d)] while the thermal conductivity along the channel width is the

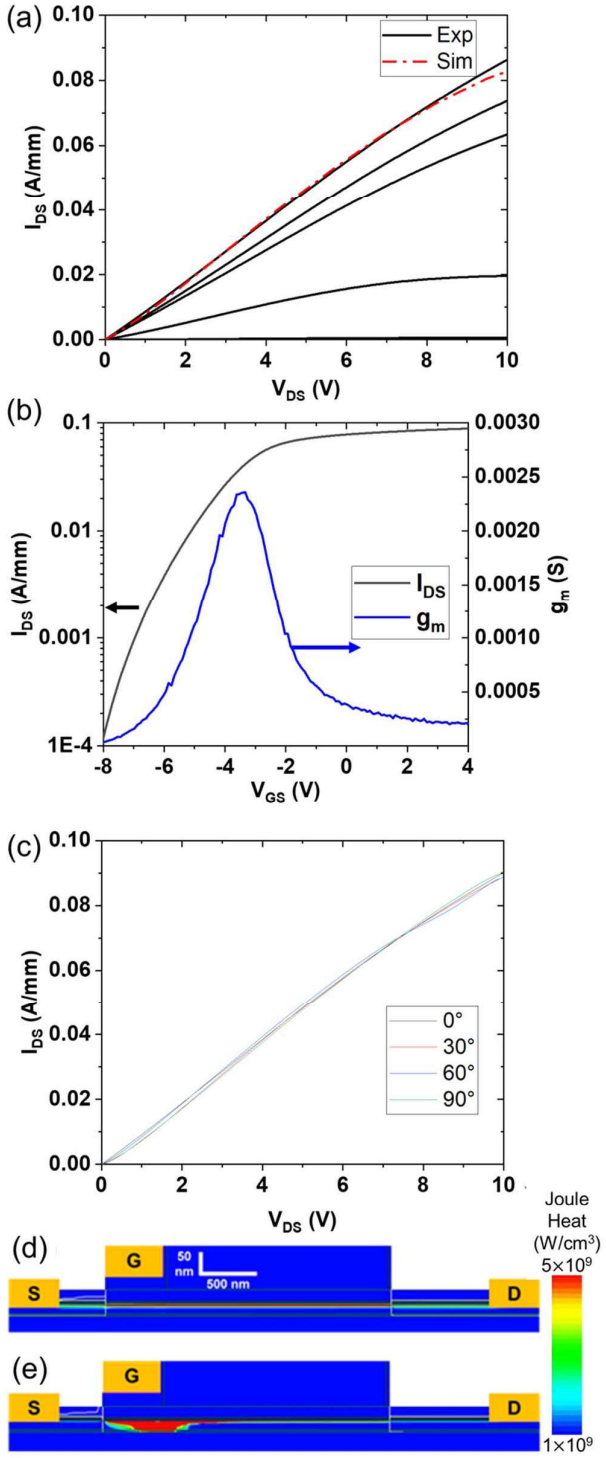

Fig. 2. (a) I–V characteristics of the baseline (0°) β-Ga_2O_3 MOSFET for V_{GS} increasing from −8 to 4 V by 3 V steps. The simulated I–V curve for $V_{GS} = 4$ V is also shown. (b) Transfer characteristics of the baseline MOSFET at $V_{DS} = 10$ V. (c) I_{DS}–V_{DS} curves at $V_{GS} = 4$ V (fully open channel conditions) of the four devices with different orientations (0°, 30°, 60°, and 90°). (d) Simulated Joule heating profile of the "fully open" channel condition ($V_{GS} = 4$ V) showing a relatively uniform heating profile throughout the entire channel. (e) Simulated Joule heating profile of the "partially open" channel condition ($V_{GS} = -4$ V) showing concentrated heating under the gate.

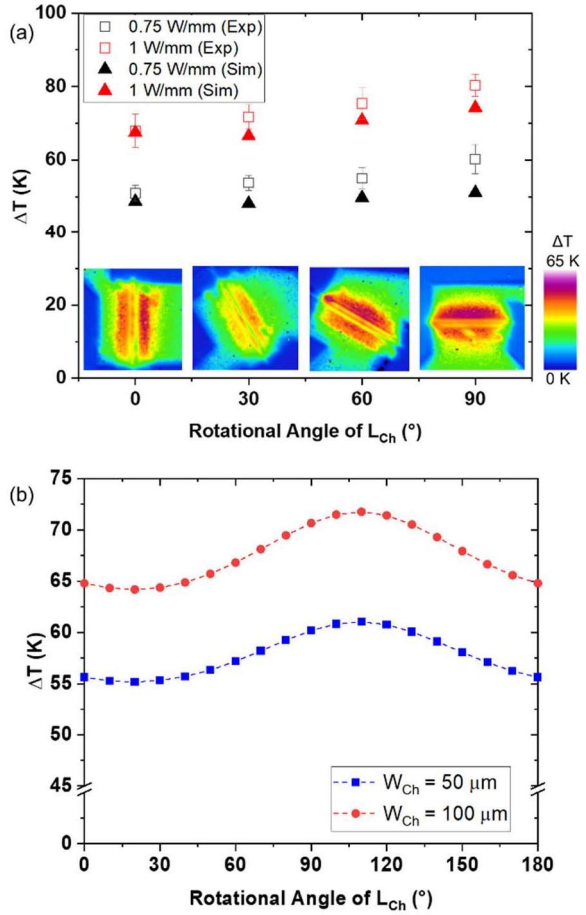

Fig. 3. (a) Gate temperatures of MOSFETs with different orientations obtained by simulation and experiments. Results for two different power dissipation levels ($P_{dis} = 0.75$, 1 W/mm at $V_{GS} = 4$ V) are shown. Also, IR images of the four MOSFETs are displayed ($P_{dis} = 0.75$ W/mm). (b) Simulated MOSFET channel temperatures as a function of channel orientation for $P_{dis} = 1$ W/mm at $V_{GS} = 4$ V. This model does not include surface metallization structures to exclusively quantify the orientation-dependence of the device self-heating. Modeling was performed for two different channel widths (W_{ch}) of 50 and 100 μm.

lowest (this direction is close to [100]). In other words, the channel width direction is less effective in terms of spreading the heat generated within the channel than the direction along the channel length. In contrast, a 110° device is subject to an opposite condition, resulting in the highest temperature rise among all orientations. In this case, the thermal conductivity along the channel length, which is close to the direction, is the lowest. It was found that the channel orientation itself can result in a ~10% difference in the channel temperature rise for $P_{dis} = 1$ W/mm at $V_{GS} = 4$ V for MOSFETs fabricated on (010)-oriented β-Ga_2O_3 substrates.

A previous report suggests a targeted power density of 10 W/mm for Ga_2O_3 MOSFETs, which is twice the operational power density of GaN power amplifiers [31]–[33]. However, this study [12] also states that the operating junction temperature should be kept below 200 °C, which is based on studies on legacy GaN RF applications [31]–[33]. Using the calibrated electro-thermal device model and assuming a base temperature condition of 25 °C, the 110° device (with the lowest in-plane thermal conductivity along the channel length direction) is able to operate up to a power density of ~2.1 W/mm at a channel temperature below 200 °C. On the

other hand, a 30° device (with the highest cross-plane thermal conductivity along the channel length direction) can operate up to ~2.4 W/mm. This equates to a ~14% increase in the power density by implementing the thermally aware design. Augmenting the optimized device layout (30° device) with device- and package-level thermal management solutions will allow achieving maximum power densities, while keeping the channel temperature below the safe operating limit.

In addition, devices with two different channel widths (50 and 100 μm) were studied via modeling to understand whether the self-heating of narrow channel devices or wide channel MOSFETs would be more influenced by the anisotropic thermal conductivity of β-Ga_2O_3. As plotted in Fig. 3(b), when the device width decreases from 100 to 50 μm (for a power dissipation level of 0.75 W/mm), the differences between minimum and maximum temperature decreases by ~10%, meaning a weaker anisotropic effect.

The discrepancy between the mean values of the experimental data and the modeling results in Fig. 3(a) indicates that the metal structure geometry may affect the device's self-heating behavior. To quantify this effect, simulation was performed where the width (W_{hp}) of the interconnect between the drain electrode and the metal bond pad (where heat is extracted through the needle probes or wire bonds; in this work, we used needle probes to operate the devices) was varied from 10 to 100 μm, as shown in Fig. 4(a). While the area of the heat extraction region (bond pad) was kept invariant, the width of the heat pathway (interconnect), W_{hp}, was varied to mimic the different shapes of the metallization structures for the devices with different channel orientations [Fig. 1(b)]. As shown in Fig. 4(b), when W_{hp} decreases to 10% of the original width, the channel temperature rise increases by ~8%. Therefore, the geometry of the metallization structures near the device active region plays an important role in dissipating heat away from the channel region. The relatively large difference between the thermal conductivities of the metal layers and the β-Ga_2O_3 is responsible for the observed geometrical effect of the metallization structures on the device self-heating. In contrast, this effect is negligible for upright-configured devices based on SiC and GaN, because of the relatively high thermal conductivity of the semiconductor base materials.

Another important aspect related to the device layout that may impact the device thermal performance is the gate–drain distance, which is typically controlled to achieve a targeted device breakdown voltage. For this reason, "electrically identical but thermally different" devices were fabricated and investigated. Fig. 5(a) shows the pulsed electrical output characteristics of the three devices with different gate–drain electrode distances (L_{GD} = 1, 6, 11 μm) under three V_{GS} conditions, demonstrating the electrically identical behavior, which is expected due to the low resistance of the n^{++} region. In other words, despite the metal electrode distances being different, the effective electron channel lengths are identical, which results in identical electrical output characteristics. Accordingly, for identical bias conditions, the three devices will exhibit an identical heat generation profile. This is shown in Fig. 5(c) as line plots of the integrated heat flux within the channel region. Therefore, the sole effect

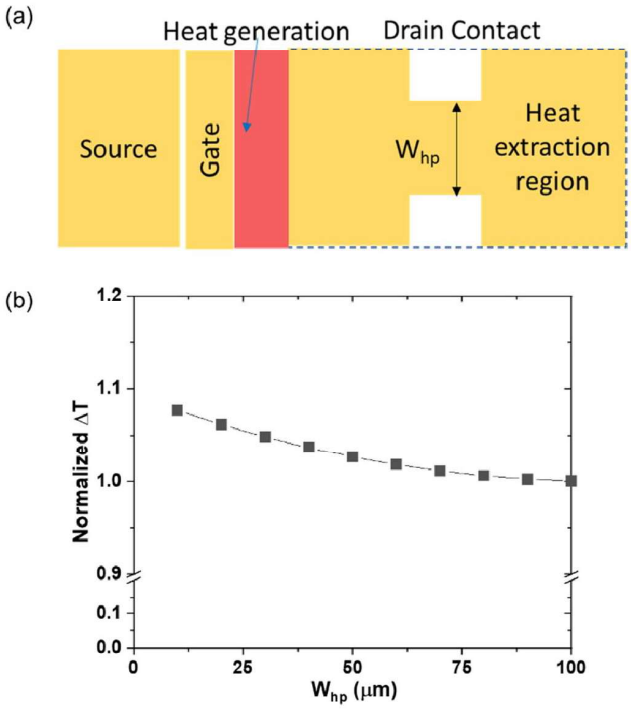

Fig. 4. (a) Schematic of the drain metal contact: to consider the differences in the metal contact shape, the width of the heat path of the metal contact (i.e., interconnect), W_{hp} varies while the area of heat extraction region is fixed. (b) Temperature rise with reduced W_{hp} is normalized with respect to the 0° model (W_{hp} = 100 μm) results. It should be noted that W_{hp} is 10 μm for the 90° MOSFET.

of the distance between the heat source (located near the drain side corner of the gate [28], [30]) and the drain metal electrode on the device self-heating behavior can be evaluated. Utilizing nanoparticle-assisted Raman thermometry, the temperatures of the source, gate, and drain electrodes were measured under a fully open channel condition (V_{GS} = 4 V, dissipated power = 0.8 W/mm), as plotted in Fig. 5(b). Since nanoparticle deposition (i.e., positioning individual particles) is not a fully controllable process, it was not possible to measure temperatures at the center of the device channels. Instead, temperatures at the drain side corner of the gate were measured using the nanoparticle-assisted Raman thermometry method. Although all three transistors were operating with identical heat generation profiles, the temperatures of the gate metal electrode show a large discrepancy. For the device with L_{GD} = 1 μm, the temperature rise of the gate electrode is the lowest since the drain electrode, which is acting as a heat sink, is closest to the heat source. Accordingly, a larger temperature rise at the drain electrode is observed, as compared to other devices with longer L_{GD}. When the drain metal electrode is further shifted by 10-μm away from the gate electrode (L_{GD} = 11 μm), a ~35% increase in the gate temperature rise occurs. For the case of L_{GD} = 6 μm, the gate temperature rise increases by about 15%, as compared to the case of L_{GD} = 1 μm. The temperature rise of the drain electrode of the MOSFET with L_{GD} = 1 μm is ~10% higher than that for the device with L_{GD} = 6-μm MOSFET and ~20% higher than that of the MOSFET with L_{GD} = 11 μm. There

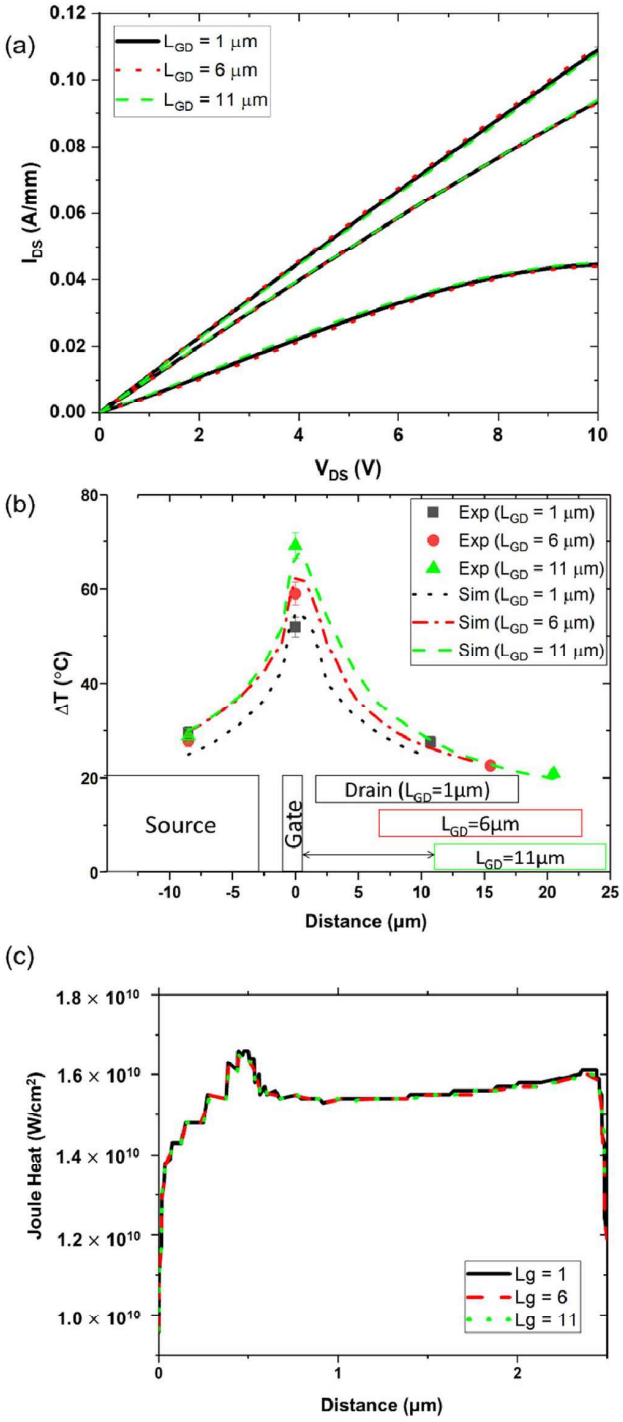

Fig. 5. (a) Pulsed *I–V* curves for $V_{GS} = -2$, 1, 4 V, for the three "electrically identical" devices with different L_{GD}. (b) Temperatures of the source–gate–drain electrodes along the centerline of the devices operating under $P_{dis} = 0.8$ W/mm at $V_{GS} = 4$ V. The length of the drain and the source electrodes are 16 μm and nanoparticles were measured near the center of the electrodes. (c) Heat flux profiles for the three gate–drain spacings at a power density of 0.75 W/mm. The two endpoints in the *x*-axis correspond to both ends of the channel region. In other words, the low resistance n^{++} regions outside the channel terminate at both ends.

is a minor difference in the source electrode temperature among the three device structures. These results demonstrate the tradeoff between increasing the device breakdown voltage and improving the device thermal performance by adjusting L_{GD} for homoepitaxial lateral transistors based on β-Ga_2O_3.

V. Conclusion

Previous studies have focused on the design of active and passive cooling solutions that add upon or alter the homoepitaxial configuration of β-Ga_2O_3 transistors. In contrast, this work has focused on how to optimize the device layout to mitigate self-heating, prior to implementing such engineering solutions. It was found that the channel orientation, the distance between the gate and drain metal electrodes, and the geometry of the interconnects that link the metal electrodes and the bond pads can play a significant role in the dissipation of heat away from the device active region. These effects are pronounced in β-Ga_2O_3 devices as compared to GaN and SiC electronics, due to the relatively low and anisotropic thermal conductivity of the base material. It was found that aligning the gate/channel length along the orientation with the highest thermal conductivity is favorable for lateral devices built on (010)-oriented β-Ga_2O_3 substrates. While a longer gate–drain distance is favorable in terms of increasing the device breakdown voltage, this is achieved at the price of sacrificing the device's thermal performance. From a thermal standpoint, it is also recommended to use wide metal interconnects between the device metal electrodes and bond pads to enhance heat extraction by the bond wires. This work demonstrates that device engineers working in the emerging field of the β-Ga_2O_3 device technology should implement device layout codesign practices that account for both electrical and thermal effects.

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