

2–8 GHz Interference Detector With 1.1 μ s Response

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Abstract—This letter reports the first wideband method that: 1) detects both the power and frequency of an arbitrary interferer within a two-octave bandwidth and 2) subsequently deactivates the interferer through a frequency-tunable narrowband bandstop filter (BSF). The entire process can be completed within approximately 1 μ s. The success of the proposed detection method relies on creating frequency- and power-dependent standing wave patterns of the incoming signal. It is worth emphasizing that all frequencies and power levels are simultaneously mapped to the system's detection scheme without requiring time-consuming spectrum- and/or power-searching steps. After presenting the fundamental concept and the basic design steps, we demonstrate a proof-of-concept system that can detect interfering signals with unknown and arbitrary frequencies in the 2–8 GHz band and powers in the -5 to $+15$ dBm range. The proposed system is implemented with low-cost off-the-shelf components. The measured interferer deactivation response time is 1.1 μ s for all signals within the system specifications.

Index Terms—Frequency-selective limiters, interference detection, wideband receivers.

I. INTRODUCTION

STRONG interferers are one of the major hurdles in wideband communications. High-power blockers can saturate receivers and possibly damage front-end devices. This is frequently addressed by employing broadband high-power active limiters (e.g., GaN limiters). This often leads to additional power consumption [1]. Moreover, while this approach reduces the potential of electrical/thermal breakdowns, it cannot recover an interferer-blocked communication channel. This limitation also applies to receivers protected by passive broadband limiters [2], [3]. Alternatively, frequency-selective limiters can discerningly suppress incoming high-power interferers, while maintaining the fidelity of the desirable communication channels [4], [5]. Such approaches, however, often exhibit the drawback of requiring prior knowledge of the blocker's frequency. In addition, the inherently limited bandwidth of frequency-selective limiters, along with slow-response times, further limit their application space.

The wideband detection method presented in this letter is capable of determining both the incoming power and

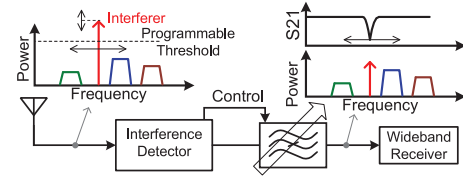


Fig. 1. Presented detection method can rapidly detect and deactivate an interferer of unknown frequency and power. The detection data are used to tune a BSF to suppress this interferer if its power exceeds an adjustable threshold level.

frequency of an arbitrary interferer within a microsecond. This information can be used to tune a bandstop filter (BSF) to suppress the interferer. The devised concept is shown in Fig. 1. The detection method relies on creating and sensing an input-spectrum-generated standing wave pattern in an open stub. This pattern is generated by weakly coupling the input signal(s) to the open stub. Voltage peak detectors are used to sense the standing wave pattern. We validate this scheme by a proof-of-concept system that can detect interferers in the 2–8 GHz band, with a power level of -5 to $+15$ dBm. The system is made with low-cost off-the-shelf components. In addition, a tunable BSF is used to demonstrate interference suppression. The system of detector and filter is capable of suppressing an interferer within 1.1 μ s, with a programmable power threshold.

II. DETECTION CONCEPT

To detect the presence of an interferer in the band of interest, a weak coupling of the input signal is used. While reactive coupling is typically preferred due to its low loss, a resistor R_C is used here because of its frequency-independent response, which is critical for multi-octave bandwidths. This is shown in Fig. 2(a). The value of the resistor is chosen such that it is practically innocuous to the insertion loss or the reflection level. The coupled signal is then amplified to ensure it is at a detectable level. The amplifier gain can be controlled to target a range of detectable power. The output of the amplifier then drives an open circuit stub, which creates a standing wave pattern that reveals the power and the frequency of the highest power signal (assuming other signals have much lower power).

Two voltage peak detectors are placed on the open circuit stub to quantify the standing wave pattern. The first is at the open end of the stub (V_0). Since this voltage is directly proportional to the interferer power (regardless of the frequency), a lookup table is created such that the reading of V_0 can be translated to power. Fig. 2(b) shows how the voltage across the stub is a function of the power of the interferer.

The second peak detector is placed at $\lambda/4$ from the open end, where λ is the guided wavelength of the maximum

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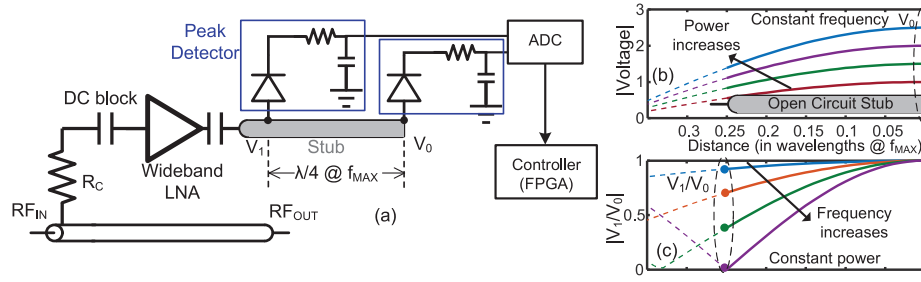


Fig. 2. (a) System-level diagram of the interferer detection part. Peak detectors sense the standing wave voltages on an open stub, which reveal the power and the frequency of the interferer. (b) Voltage at the open end of the stub is power-dependent. (c) Normalized voltage $\lambda/4$ away from the open end is a bijective function of the interferer frequency.

detectable frequency f_{MAX} . Since the voltage there, V_1 , is also power dependent, it is imperative to normalize it to V_0 . This normalization results in a bijective relationship to frequency. From transmission line theory, it can be shown that this relationship is

$$\left| \frac{V_1}{V_0} \right| = \left| \cos \left(\frac{\pi}{2} \frac{f}{f_{\text{MAX}}} \right) \right| \quad (1)$$

where f is the interferer frequency. This relationship is plotted in Fig. 2(c) for various interferer frequencies. From (1), it can be seen that frequencies above f_{MAX} result in a non-bijective relationship between the normalized V_1 and the frequency.

The voltages from the peak detectors are read using an Analog to Digital Converter (ADC). A controller (implemented in an FPGA in this demonstration) reads the voltages from the ADCs, normalizes V_1 , and takes the necessary control decision to tune the BSF based on the available lookup table.

III. IMPLEMENTATION

A. Design

The interference detection is designed on a 20-mil-thick RO-4003 substrate. The following components are used. LNA: HMC8410, peak detector Schottky diodes: MADS-002502-1246HP, ADCs: LTC2315CTS8. The assembled PCB is shown in Fig. 3(a). The coupling resistor R_C is 150 Ω , followed by a 0.5 pF capacitor. The BSF used in this work is a substrate-integrated structure [6], [7], with PIN diode tuning ability.

B. Characterization

First, the response of the through transmission line (RF_{IN} to RF_{OUT}) is measured to demonstrate the effect of the coupling. This measurement is shown in Fig. 3(b). It can be seen that the coupling exhibits no adverse impact on the transmission line performance.

Since V_0 is directly proportional to the input power, Fig. 3(c) shows this relationship versus frequency. These data are used to determine whether the input power is above a given threshold. While ideally V_0 should not vary versus frequency, the amplifier gain response, in addition to non-linear effects from the diodes, cause those frequency-dependent variations. Nevertheless, these variations have no major effect on the performance of the system.

Fig. 3(d) shows the measured normalizing ratio from (1). This relationship is used to determine the frequency

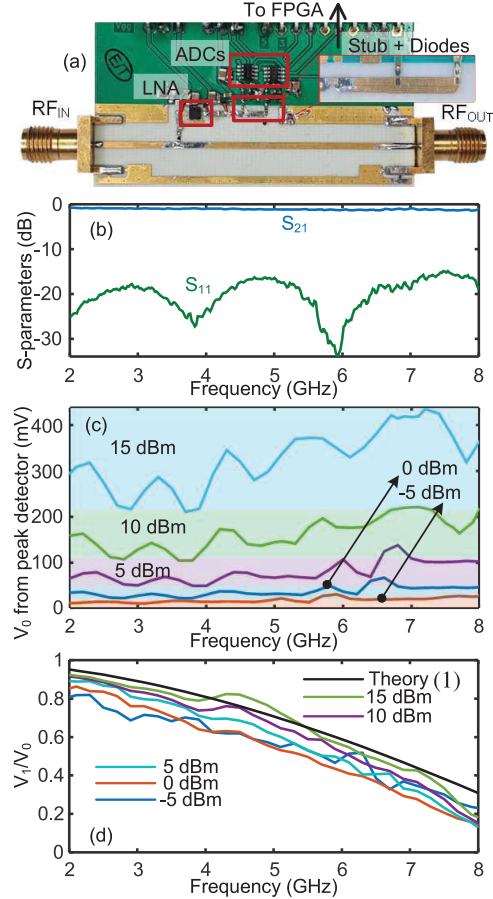


Fig. 3. (a) Implemented PCB of the interference detector along with its associated components. (b) Through measurement of the RF line showing minimal effect of the detection method on the frequency response. (c) Measured voltage at the open end of the stub (V_0 in Fig. 2). This voltage reveals the input power. (d) Ratio V_1/V_2 reveals the frequency of the interferer.

of the interferer. The measurements generally align with the theoretical analysis. The deviations are primarily due to the above-mentioned non-ideal effects, in addition to the power-dependent response of the active components. This, however, does not impair the operation of the detection because the power is already known (from measuring V_0). As a result, the proper curve is selected during operation. In addition, the ripple in Fig. 3(d) is within the bandwidth of the BSF, which implies that the detector can still suppress the interferer. Since the circuit contains no nonlinear components in the main RF path, the linearity is not affected.

TABLE I
COMPARISON WITH STATE-OF-THE-ART. (#: ESTIMATED FROM TECHNOLOGY. COTS: COMMERCIAL OFF-THE-SHELF)

Ref. Tech.	[4] MEMS	[5] COTS	[8] COTS	[9] COTS	[10] COTS	[11] COTS	This work COTS
BW (GHz)	2.3–2.8 [#]	1.5–2	< 0.05	0.25–0.3	1–1.3	1.9–2.2 [#]	2–8
Interference detection	N	Y	Y	Y	N	N	Y
Power activation	Y	Y	Y	Y	Y	Y	Y
Arbitrary interference frequency	N	N	Y	Y	Y	N	Y
Response time	100's μ s [#]	100's ms [#]	40 μ s	NA	16 ns	NA	1.1 μ s

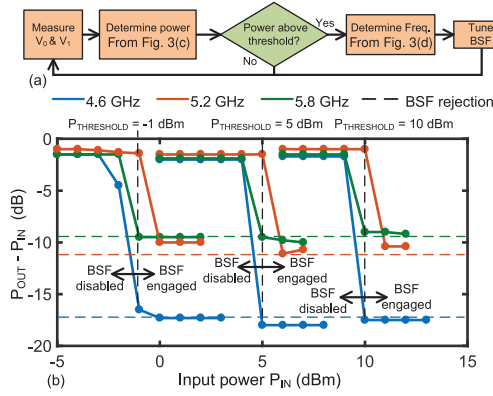


Fig. 4. (a) Flowchart describing the operation of the FPGA controller of the interference detector. (b) Detector, along with a BSF, is used as a programmable frequency-selective power limiter. The measurements shown are at various frequencies and different power thresholds with no user intervention. The suppression is only limited by the performance of the BSF.

IV. MEASUREMENTS

The FPGA controller is constantly reading the voltages V_0 and V_1 to make decisions based on the interferer frequency and power. The flowchart in Fig. 4(a) summarizes its operation. The overall power consumption is 800 mW. Lower power, however, is possible to achieve using integrated solutions.

A. Power Limiting

The measurements in Fig. 4(b) show how the detector is used in a frequency-selective power limiter. The threshold power level ($P_{THRESHOLD}$) is user-programmable (no hardware redesign is required). The demonstrated power levels are -1 , $+5$, and $+10$ dBm. The demonstrated frequencies are only limited by the available bandwidth of the employed BSF. The same applies to the suppression level of the interferer. Hence the interferer suppression is only limited by the quality of the employed BSF and not the detection scheme. It is worth noting here that this curve works in both directions of input power: low-to-high and high-to-low.

B. Response Time

The response time of the detector is a critical protection metric. To measure the response time, the setup in Fig. 5(a) is used. Two signals are monitored with the oscilloscope. The first is the sensed output RF power from the detector and the BSF, and the second is an “Interference Detected” logic signal from the FPGA. In this measurement, the input power is pulsed between -5 and $+12$ dBm with a 5μ s width.

First, the setup is measured with the BSF disabled. This way, the output of the power sensor can be measured for comparison

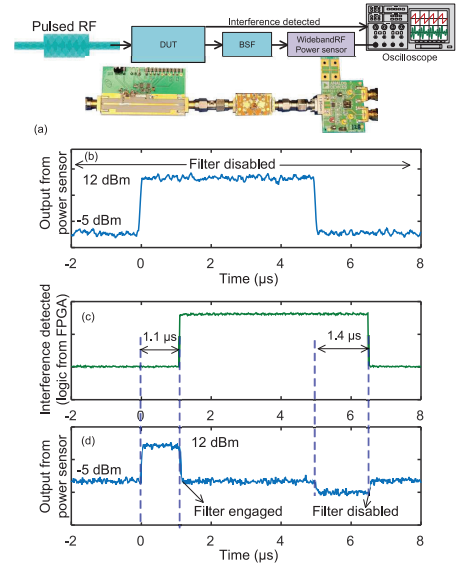


Fig. 5. (a) Response time measurement setup. (b) Output of the power sensor when excited with an RF pulse (5.5 GHz). The BSF is disabled. (c) Logic output of the FPGA showing an interference detection when the RF pulse is at the high power. (d) Output of the power sensor when the BSF is enabled. The system is able to suppress the interferer within 1.1μ s.

purposes. The result in Fig. 5(b) shows the expected output from the power sensor.

Next, the BSF is enabled. It can be seen from Fig. 5(c) that the interference is detected after 1.1μ s. This time is approximately equally divided between the peak detectors and the ADCs. This is faster than search-based methods [12].

Once the FPGA detects the interferer, it tunes the BSF to the detected frequency (by switching the proper PIN diodes). This causes the output power to drop. This is shown in Fig. 5(d). Conversely, when the RF high-power pulse ends, the filter is no longer necessary, and it is removed from the signal path. This recovery response time is 1.4μ s.

Table I compares the achieved performance to published state-of-the-art. The presented detector is significantly wider in bandwidth, has a much faster response time, and is more adaptive by requiring no prior knowledge of the interferer.

V. CONCLUSION

The first wideband interference detection and suppression method with approximately 1μ s response time for an interferer with unknown frequency and power has been presented. The effect of the interferer bandwidth is subject for further research. In addition to the concept and design, we demonstrate a proof-of-concept system with two octaves bandwidth (2–8 GHz) capable of sensing the power and frequency of unknown interferers. This state-of-the-art performance is critical for protecting sensitive receivers from harmful RF pulses.

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