nature electronics

Article

https://doi.org/10.1038/s41928-022-00836-5

An elastic and reconfigurable synaptic transistor based on a stretchable bilayer semiconductor

Received: 20 September 2021

Accepted: 16 August 2022

Published online: 29 September 2022

Check for updates

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Neurons of the ventral tegmental area of the brain contain single axon terminals that release excitatory and inhibitory neurotransmitters, creating reconfigurable synaptic behaviour. Artificial synaptic transistors that exhibit similar excitatory and inhibitory behaviour—and hence synaptic function reconfiguration—could provide diverse functionality and efficient computing in various applications. However, some of these applications, such as soft robotics and wearable electronics, require synaptic devices that are mechanically soft and deformable. Here we report an elastic and reconfigurable synaptic transistor that exhibits inhibitory and excitatory characteristics even under mechanical strain. The synaptic device uses a top-gated configuration and is made using a stretchable bilayer semiconductor and an encapsulating elastomer as the gate dielectric. The device exhibits memory characteristics when operating with a presynaptic pulse of only 80 mV, resulting in a low specific energy consumption. When applied to a model artificial neural network for dual-directional image recognition of the Modified National Institute of Standards and Technology dataset, a recognition accuracy of over 90% is achieved even when the transistors are stretched by 50%.

The single axon terminal in neurons of the ventral tegmental area display reconfigurable and bilingual (that is, excitatory and inhibitory) synaptic behaviour by releasing excitatory and inhibitory neurotransmitters[1]. A mechanically stretchable, artificial synaptic device that can exhibit similar excitatory and inhibitory synaptic behaviours could be of use for a range of applications, including soft robots[2], wearable health monitors[3] and abiotic prosthetics[4]. Although deformable and stretchable synaptic transistors have been developed, they typically exhibit monosynaptic behaviours[5,6]. These synaptic transistors are primarily constructed from p-type organic semiconductors with ion gel dielectrics[5,7,8], whose operational mechanism is associated with transient charge transport and dynamics, which makes it difficult to realize both excitatory and inhibitory synaptic behaviour. In addition, the operation of an ion-gel-based gated device involves the

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https://doi.org/10.1038/s41928-022-00836-5

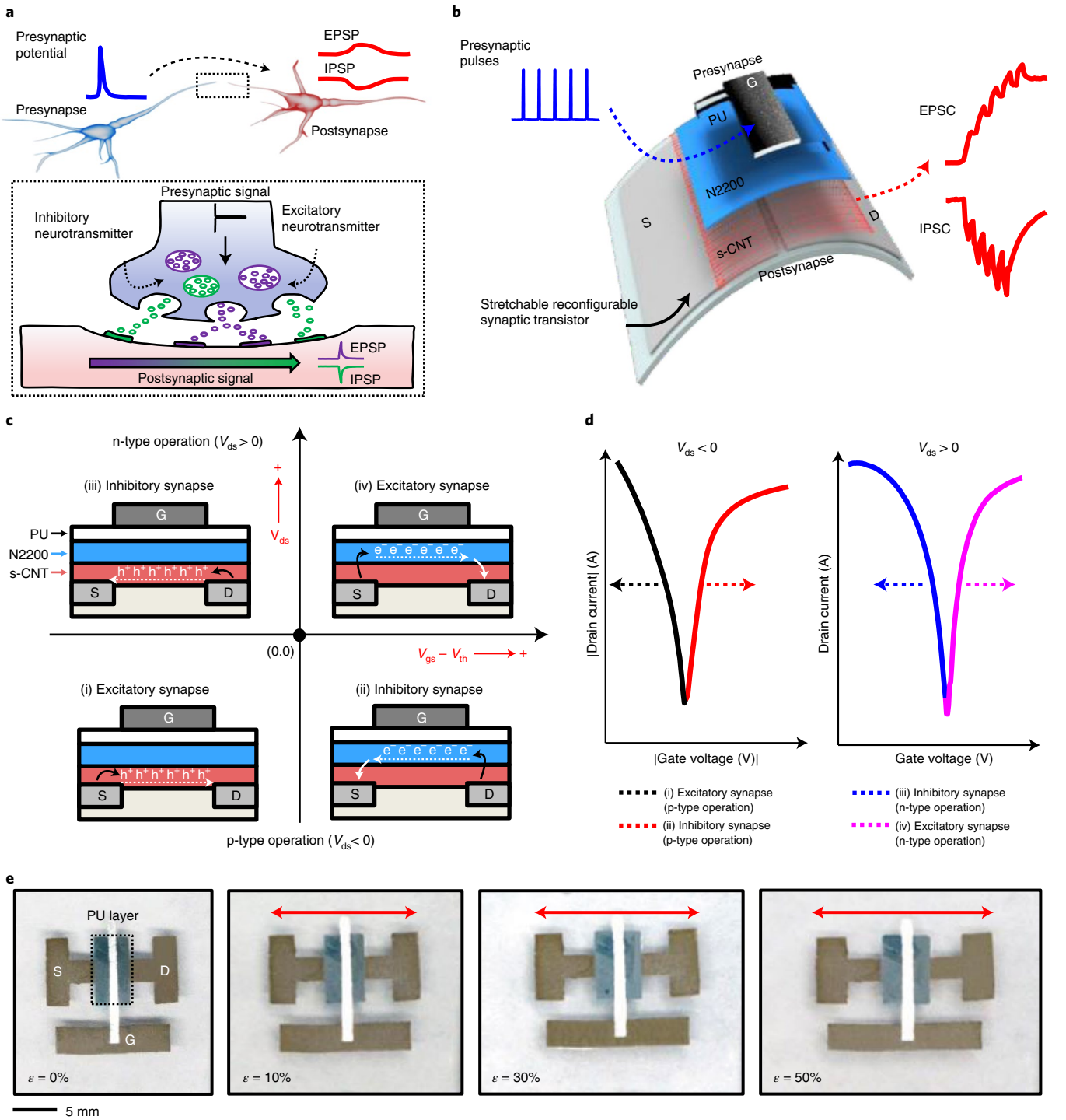

Fig. 1 | Overview of the stretchable reconfigurable synaptic transistor. a, Schematic of a synapse present in the ventral tegmental area and its synaptic transmission process in a bilingual synapse. **b**, Stretchable reconfigurable synaptic transistor emulates the behaviours of a bilingual synapse. **c**, Working mechanism of the device depending on the applied bias voltage. **d**, Schematic of the transfer curves of the transistor with corresponding excitatory and inhibitory synaptic behaviours. **e**, Set of optical images of the stretchable reconfigurable synaptic transistor before and after uniaxial stretching by 10%, 30% and 50% along the channel length direction. S, source; D, drain; G, gate.

electrochemical doping of the bulk semiconductor layer, which leads to inevitable device degradation over time[9].

In this Article, we report a stretchable and reconfigurable synaptic transistor created using a stretchable bilayer semiconductor. The bilayer semiconductor channel consists of a thin layer of poly[(*N*,*N*′-bis(2-octyldodecyl)-naphthalene-1,4,5,8-bis(dicarboximide)-2,6-diyl)-*alt*-5,5′(2,2′-bithiophene)] (P(NDI2OD-T2) or N2200) film on a network of semiconducting single-walled carbon nanotubes (s-CNTs); a polyurethane (PU) elastomer is used as the gate dielectric, instead of an ion gel dielectric. Polar functional groups in the PU dielectric allow charge trapping, which results in the synaptic characteristics of the transistor[10]. The stretchable synaptic transistor exhibits both excitatory and inhibitory characteristics and allows the synaptic functions to switch from one to the other. Its performance is retained even after

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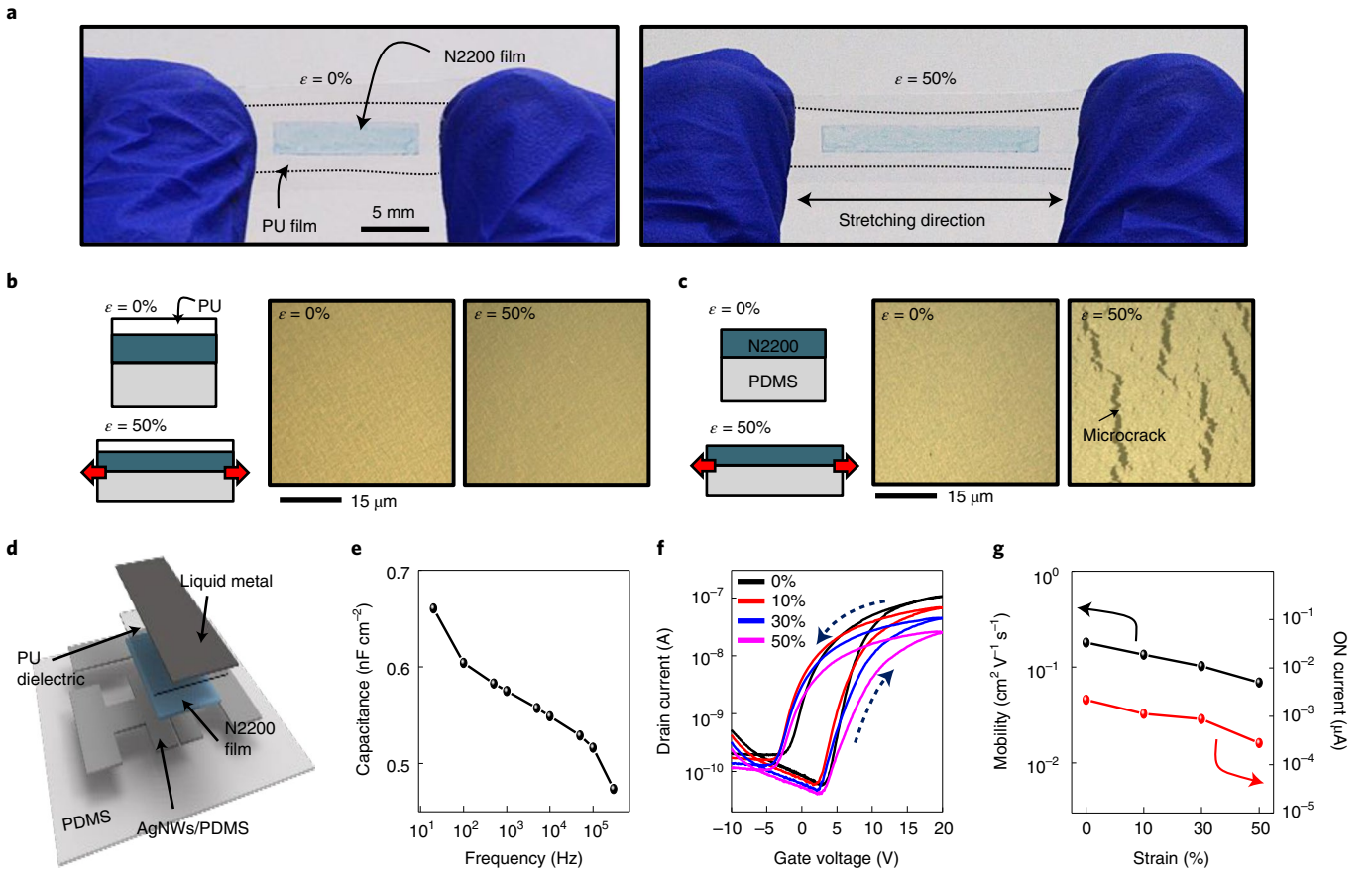

Fig. 2 | Thin, stretchable N2200 n-type semiconductor film. a, Optical images of PDMS/N2200/PU without strain (left) and with 50% strain (right). **b**, Effect of strain on the structure of PDMS/N2200/PU. **c**, Effect of strain on the structure of PDMS/N2200. **d**, Schematic of the N2200-thin-film-based transistor. **e**, Frequency-dependent capacitance of the PU gate dielectric per unit area. **f**, Transfer curves of the transistor under mechanical strains of 0%, 10%, 30% and 50%. **g**, Values of μ_{FE} and ON currents under different mechanical strains of 0%, 10%, 30% and 50% along the channel length direction.

being stretched by 50%. Additionally, the device possesses memory characteristics with a low-amplitude presynaptic pulse of 80 mV and the lowest specific energy consumption compared with other organic synaptic transistors[11–13]. The architecture of the bilayer semiconductor with elastomer dielectric encapsulation also enhances device stability, with function retained for more than 90 days. Dual-directional image recognition of the Modified National Institute of Standards and Technology (MNIST) dataset of handwritten digits simulated in an artificial neural network (ANN) of our artificial synaptic devices shows a recognition accuracy of over 90%, even when stretched by 50%.

Overview of a stretchable reconfigurable synaptic transistor

Figure 1a shows the schematic of a bilingual synapse that co-releases excitatory and inhibitory neurotransmitters[1,14]. The bilingual synapse acts as both excitatory and inhibitory synapses, showing both excitatory postsynaptic potentials (EPSPs) and inhibitory postsynaptic potentials (IPSPs), respectively. The capability to emulate such behaviours of the bilingual synapse could offer critical benefits in soft intelligent systems that can simultaneously achieve diverse functions, simplified circuit design and efficient computing. The stretchable reconfigurable synaptic transistor was constructed by using stretchable bilayer semiconductors (Fig. 1b). Specifically, the device was fabricated by using the stacked channel of N2200 and s-CNT networks, PU, silver nanowires in polydimethylsiloxane (AgNWs/PDMS) and eutectic liquid metal alloy of gallium–indium as the bilayer semiconductor, gate dielectric, source/drain electrode and gate electrode, respectively. The dielectric encapsulation restricts the formation and propagation of microcracks within the semiconductor thin film on applying large levels of mechanical strain, which lead to improvement in device stability, especially for the n-type semiconductor[10]. The detailed fabrication procedure of the devices is described in Methods. The postsynaptic current (PSC) of the device can be tuned depending on both applied drain and gate voltages, and thus, the device generates both excitatory postsynaptic current (EPSC) and inhibitory postsynaptic current (IPSC) from presynaptic pulses. Figure 1c illustrates the working mechanism of the reconfigurable synaptic transistor. Depending on the applied drain voltage and gate voltage, different charge carriers (electrons and holes) and charge transport direction would determine the synaptic behaviour. Figure 1d illustrates the schematic of the transfer curves of the transistor with the corresponding excitatory and inhibitory synaptic behaviours, which further explains its characteristics on different operation conditions. Figure 1e exhibits a set of optical images of the stretchable reconfigurable synaptic transistor before and after uniaxial stretching by 10%, 30% and 50% along the channel length direction.

Stretchable synaptic transistor based on N2200 thin film

To study the stretchable reconfigurable synaptic transistor, we first investigated the stretchable synaptic transistors based on a single-layer n-type or p-type semiconductor with excitatory characteristics. Figure 2a shows the optical images of an ~100-nm-thick N2200 film on a PDMS substrate covered with a PU layer, without strain and with uniaxial stretching ($\varepsilon = 50\%$). The N2200 film was prepared by spin

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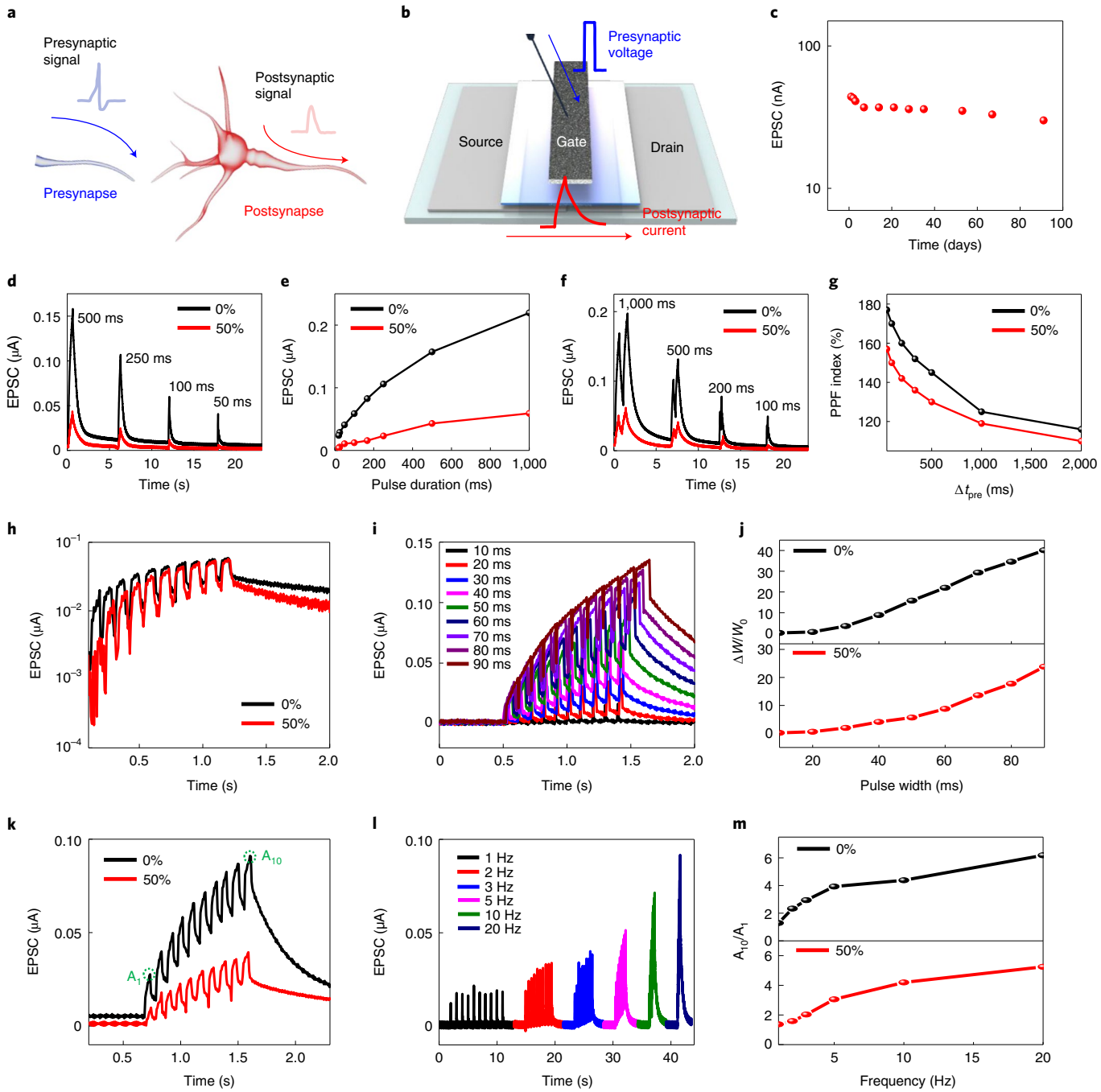

Fig. 3 | Stretchable synaptic transistor based on the N2200 thin film. **a**, Schematic of a biological synapse and its synaptic transmission process. **b**, Schematic of the device structure and operation of the synaptic transistor. **c**, EPSC results of the synaptic transistor in the ambient environment over 90 days. **d**, Representative single-pulse-induced EPSC for the device without strain and with 50% strain. **e**, EPSC peaks with respect to the pulse widths for the device without strain and with 50% strain. **f**, Representative EPSC results triggered by two successive pulses without strain and with 50% strain. **g**, PPF index results with respect to Δt_{pre} for the device without strain and with 50% strain. **h**, EPSC results of the stretchable synaptic transistor with the application of ten successive presynaptic pulses without strain and with 50% strain. **i**, Results of memory characteristics with respect to the different pulse widths for the device without strain and with 50% strain. **j**, Values of $\Delta W/W_0$ with respect to different pulse widths for the device without strain and with 50% strain. **k**, Representative EPSC results of the device without strain and with 50% strain on the application of ten successive presynaptic pulses (+10 V, 50 ms). **l**, Results of filtering characteristics with respect to different pulse frequencies. **m**, Calculated gain of EPSCs (A_{10}/A_1) with respect to different pulse frequencies for the device without strain and with 50% strain.

coating an N2200 solution in mesitylene (5 mg ml^{-1}) at 1,000 rpm for 60 s on top of a PDMS substrate, followed by baking at 90 °C for 1 h in N_2. Next, the PU solution in tetrahydrofuran (75 mg ml^{-1}) was spin coated at 1,000 rpm for 60 s, followed by baking at 100 °C for 1 h to solidify the film. Note that the N2200 film with PU encapsulation (that is, PU/N2200/PDMS) can be uniaxially stretched up to 50% without fracture failure or a notable amount of cracks (Fig. 2b). In contrast, a bare N2200 film on a PDMS substrate (that is, N2200/PDMS) prepared with the same procedures presented many microcracks when stretched (Fig. 2c). Supplementary Fig. 1 shows the detailed morphologies of the N2200 films without PU (Supplementary Fig. 1a) and with PU (Supplementary Fig. 1b) encapsulation after stretching by 50% and then

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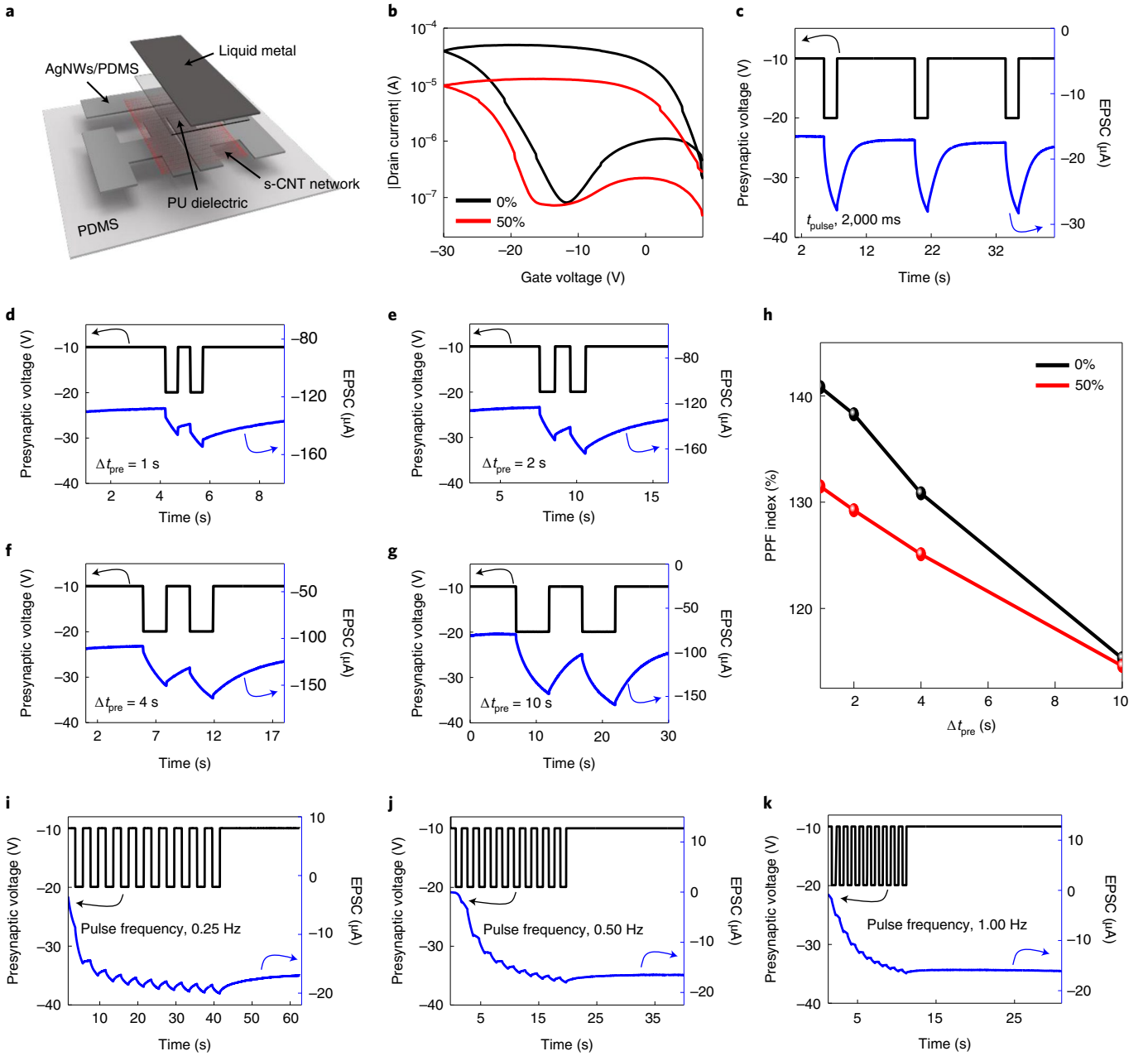

Fig. 4 | Stretchable synaptic transistor based on the s-CNT network. **a**, Schematic of the device structure of the stretchable synaptic transistor based on the p-type s-CNT network. **b**, Transfer curves of the device without strain and with 50% strain. **c**, Representative single-pulse-induced EPSC results. **d**–**g**, EPSC triggered by two successive pulses (−10 V) with different Δt_{pre} values of 1 s (**d**), 2 s (**e**), 4 s (**f**) and 10 s (**g**) applied to the gate with V_{ds} of −10 V. **h**, Summarized PPF index with respect to different Δt_{pre} values without strain and with 50% strain. **i**–**k**, EPSCs with variable pulse frequencies of 0.25 Hz (**i**), 0.50 Hz (**j**) and 1.00 Hz (**k**).

releasing to 0% strain. Note that the data in Supplementary Fig. 1b are obtained after the chemical removal of PU by immersing the sample in dimethylformamide. Since N2200 is an intrinsically non-stretchy material, on stretching, microcracks form and propagate, which has been reported elsewhere[15]. However, PU encapsulation leads to restriction on the microcracks with much lower crack density, owing to the competing shear stress applied on the bottom and top surfaces of the N2200 film[16] from the PDMS substrate and PU encapsulation, respectively.

Figure 2d shows a schematic of the thin stretchable N2200-thin-film-based transistor with a PU gate dielectric. The detailed fabrication procedure and steps are shown in Methods and Supplementary Fig. 2, respectively. Note that Kapton shadow masks were used to pattern the materials in a layer-by-layer fashion. The specific capacitance per unit area of the PU gate dielectric is 0.662 nF cm^{-2} at 20 Hz and 0.474 nF cm^{-2} at 300 kHz (Fig. 2e). Figure 2f shows the transfer curves of the transistor under mechanical strains of 0%, 10%, 30% and 50% along the channel length direction. All of them exhibit current–voltage hysteresis, which is essential for emulating a biological synapse[6,8]. Note that a similar trend of degradation was observed when the device was under mechanical strains of 0%, 10%, 30% and 50% perpendicular to the channel length direction (Supplementary Fig. 3). The maximum drain currents (that is, ON current) and the calculated field-effect mobility (μ_{FE}) of the stretchable n-type transistor under different strains are summarized in Fig. 2g. Note that we calculated the μ_{FE} value on the basis of the linear regime of these transfer curves (Supplementary Information). When stretched along the

channel length direction by 50%, the μ_{FE} value decreases from 0.18 to 0.07 $cm^2 V^{-1} s^{-1}$. These results indicate that the device retains reasonable transport properties under large strain.

The excitatory synaptic behaviour of the device was systematically investigated. Figure 3a shows the schematic of a biological synapse and its synaptic transmission process. A presynaptic signal from the presynaptic terminal is transferred to the postsynaptic membrane by neurotransmitter migration through the synaptic cleft, which induces postsynaptic signals. In the synaptic transistor, a positive presynaptic pulse delivered to the gate electrode results in electron accumulation at the interface with the PU gate dielectric, leading to an EPSC (Fig. 3b)[17]. In addition, the synaptic transistor exhibited a very stable EPSC output over time due to PU encapsulation. We investigated single-pulse-induced EPSCs in the ambient environment for up to 90 days. The presynaptic pulse (+10 V, 500 ms) was applied to the gate with a drain voltage (V_{ds}) of +10 V. Although several n-type organic semiconductors are typically unstable under ambient conditions[18], our device retained ~70% of the EPSC even after ~90 days (Fig. 3c). To further characterize the single-pulse-induced EPSC response of the device, we chose pulses with different widths ranging from 20 to 1,000 ms. Figure 3d shows the representative EPSC results of the stretchable synaptic transistor without strain and with 50% strain, demonstrating excellent operation under mechanical deformation. The EPSC increased with the pulse width because the number of electrons at the interface between the N2200 semiconductor and PU gate dielectric increased. The EPSC peaks as a function of the pulse duration for devices without strain and with 50% strain are summarized in Fig. 3e and Supplementary Figs. 4 and 5. Similarly, the EPSC peaks increased when the amplitude of the presynaptic pulse increased (Supplementary Figs. 6 and 7). Two successive presynaptic pulses (+10 V) with a pulse interval (Δt_{pre}) ranging from 50 to 2,000 ms were also applied to the gate with V_{ds} of +10 V, and the representative EPSC results are shown in Fig. 3f. The EPSC results for different Δt_{pre} values without strain and with 50% strain are shown in Supplementary Figs. 8 and 9, respectively. The second EPSC peak (A_2) is higher than the first EPSC peak (A_1) when Δt_{pre} decreases, which results in an increased paired-pulse facilitation (PPF) index, defined as the ratio between the amplitude of the second EPSC peak (A_2) and that of the first EPSC peak (A_1), that is, A_2/A_1. This phenomenon is observed because some of the induced electrons in the first pulse remain at the interface between the PU gate dielectric and N2200 semiconductor when the second pulse is applied. The PPF index decreased from 177% to 116% when Δt_{pre} increased from 50 to 2,000 ms. Note that the original value of the PPF index was retained after uniaxial stretching at 50% along the channel length direction (Fig. 3g).

We further studied the short-term memory (STM) to long-term memory (LTM) transition of the stretchable synaptic transistor. Two sets of ten successive presynaptic pulses were applied to the gate[8]. The application of ten successive presynaptic pulses (+10 V, 50 ms) and the corresponding EPSC results (without strain and with the device under 50% strain) are shown in Fig. 3h. The results show the emulation of the typical transition from STM to LTM of the human brain during the repetitive learning process[19–23], which has no substantial change even after 50% strain. The results of memory characteristics with different pulse widths from 10 to 90 ms (step of 10 ms) are presented in Fig. 3i. As the pulse width increases, the amplitude of the EPSC increases and slowly decreases back to the initial state. The governing mechanism is the same as that of the PPF index described previously. The results of the memory characteristics with the device under 50% strain are shown in Supplementary Fig. 10. The long-term weight change, that is, the relative synaptic weight change, is calculated as $\Delta W/W_0$, where W_0 and ΔW denote the initial current (before the presynaptic pulse) and current change (after the presynaptic pulse), respectively. As the pulse width increases, $\Delta W/W_0$ increases (Fig. 3j). These results show that the stretchable synaptic transistors still retain their synaptic characteristics even after being uniaxially stretched by 50%. The memory characteristics of ten successive presynaptic pulses (+10 V, 50 ms) with variable frequencies from 1 to 15 Hz (without strain and with 50% strain) are shown in Supplementary Fig. 11. The trend of $\Delta W/W_0$ is similar to that of the aforementioned results, which has a clear dependence on pulse frequency (Supplementary Fig. 12).

The high-pass filtering characteristic was also studied by applying presynaptic pulses (+10 V) with different frequencies ranging from 1 to 20 Hz (V_{ds} = +10 V). The duty cycle was fixed at 50%. Figure 3k shows the representative EPSC results without strain and with 50% strain after the application of ten successive presynaptic pulses (+10 V, 50 ms). Note that the last EPSC peak (A_{10}) is higher than the first EPSC peak (A_1). The EPSC results with variable frequencies from 1 to 20 Hz are summarized in Fig. 3l, which clearly exhibit the high-pass filtering characteristic. The results obtained from the device under 50% strain are presented in Supplementary Fig. 13. The gain of the EPSC is defined as A_{10}/A_1 and is used for the estimation of the filtering characteristic. Figure 3m summarizes the calculated gain with respect to different frequencies. The gain increased from 1.30 to 6.18 when the frequency increased from 1 to 20 Hz. The gain was still retained when the device was stretched by 50% strain.

Stretchable synaptic transistor based on s-CNT network

The p-type-semiconductor-based stretchable synaptic transistors were also constructed and their excitatory characteristics were studied. Specifically, the s-CNT network was chosen as a p-type semiconductor. Scanning electron microscopy images of the s-CNT network revealed that no obvious cracks were observed under mechanical strain (Supplementary Fig. 14). The synaptic transistor has a top-gated configuration with the s-CNT network and PU gate dielectric. The detailed device fabrication procedures are described in Methods. Figure 4a shows a schematic of the exploded view of the stretchable synaptic transistor. In the transfer curves (Fig. 4b), the transistor also showed hysteresis[24,25]. Figure 4c shows the representative single-pulse-induced EPSC results after applying a presynaptic pulse (−10 V (that is, −10 to −20 V); 2,000 ms) to the gate with V_{ds} of −10 V. The EPSC results for the device with 50% strain are presented in Supplementary Fig. 15. Two successive presynaptic pulses with different Δt_{pre} values, ranging from 1 to 10 s, to the gate with V_{ds} of −10 V were also applied (Fig. 4d–g). The second EPSC peak is higher than the first EPSC peak. The summarized PPF index with different Δt_{pre} values without strain and with 50% strain is presented in Fig. 4h. The PPF index decreased from 141% to 115% when Δt_{pre} increased from 1 to 10 s, yet it was maintained when the device was stretched by 50% along the channel length direction. The detailed EPSC results with different Δt_{pre} values for the device under 50% strain are shown in Supplementary Fig. 16. We further tested the EPSCs by applying ten successive presynaptic pulses with an amplitude of −10 V; duty cycle of 50%; and variable pulse frequencies ranging from 0.25, 0.50 and 1.00 Hz (Fig. 4i–k). The STM to LTM transition clearly exists. The LTM characteristic during a longer time is presented in Supplementary Fig. 17.

Stretchable reconfigurable synaptic transistor

Finally, the stretchable reconfigurable synaptic transistor was constructed by using stretchable bilayer semiconductors (Fig. 5a,b). The device fabrication processes are detailed in Methods. The transfer characteristics and hysteresis behaviours of the device depending on different operational voltages are shown in Fig. 5c,d, respectively. The minimum operational voltage (V_{ds}) was confirmed as +1 V (n-type operation) or −1 V (p-type operation), which ensures low energy consumption, as described later. The synaptic characteristics of the stretchable n-type and p-type transistors serve as the foundation for understanding the stretchable reconfigurable synaptic transistors with both excitatory and inhibitory postsynaptic features. The EPSC is defined as the case when the PSC increases on the application of positive pulses or when the PSC decreases on the application of negative pulses. On

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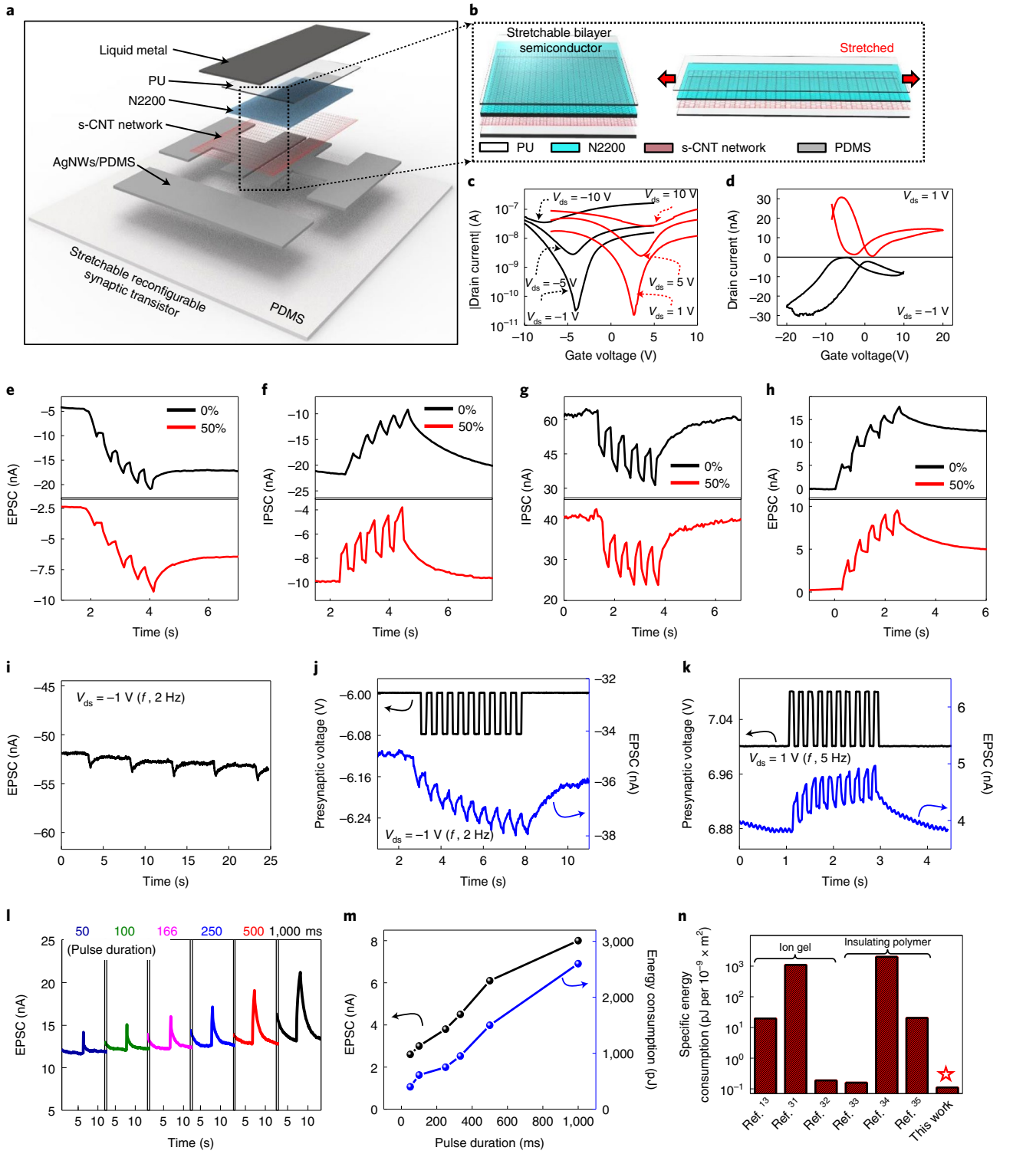

Fig. 5 | Stretchable reconfigurable synaptic transistor based on bilayer semiconductors. a, Schematic of the exploded view of the reconfigurable synaptic transistor. **b**, Schematic of stretchable bilayer semiconductors. **c**, Transfer characteristics of the device depending on different operational voltages. **d**, Hysteresis behaviours of the device at +1 V (n-type operation) and −1 V (p-type operation), respectively. **e**, EPSC results triggered by five successive pulses for the device without strain and with 50% strain, that is, operation in region (i), Fig. 1c. **f**, IPSC results triggered by five successive pulses for the device without strain and with 50% strain, that is, operation in region (ii), Fig. 1c. **g**, IPSC results triggered by five successive pulses for the device without strain and with 50% strain, that is, operation in region (iii), Fig. 1c. **h**, EPSC results triggered by five successive pulses for the device without strain and with 50% strain, that is, operation in region (iv), Fig. 1c. **i**, Single-pulse-induced EPSC results, corresponding to presynaptic pulses (−80 mV, 250 ms) with V_{ds} of −1 V. **j**, EPSC results of the reconfigurable synaptic transistor with the application of ten successive presynaptic pulses (−80 mV, 250 ms) with V_{ds} of −1 V. **k**, EPSC result of the reconfigurable synaptic transistor with the application of ten successive presynaptic pulses (+80 mV, 100 ms) with V_{ds} of 1 V. **l**, Single-pulse-induced EPSCs of the reconfigurable synaptic transistor. **m**, Peak currents of EPSCs and energy consumption with respect to different pulse durations. **n**, Summarized specific energy consumption of currently reported organic synaptic transistors.

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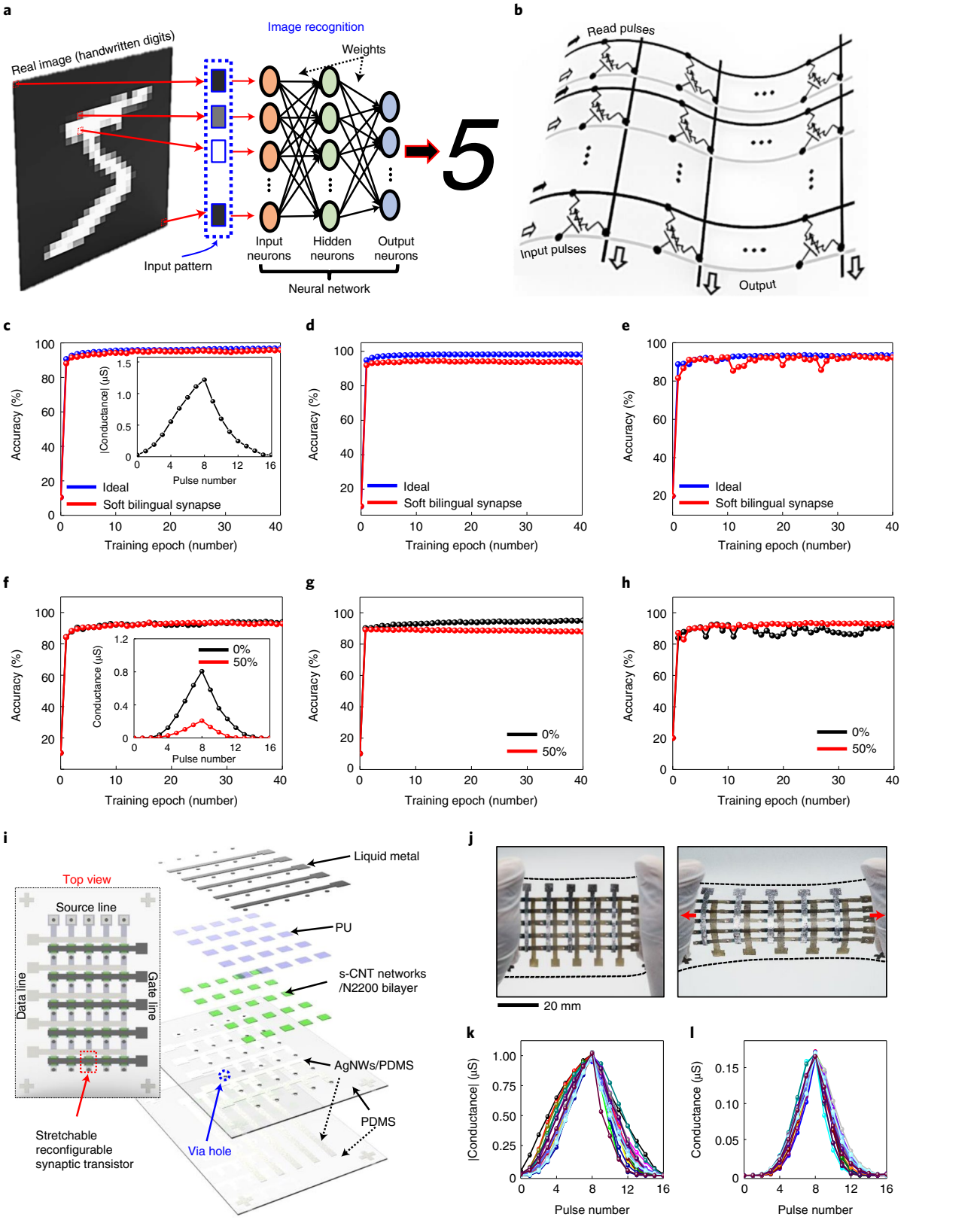

Fig. 6 | Dual-directional image recognition. a, Schematic of ANNs for image recognition. **b**, Schematic of a deformable crossbar array, considered as part of a 'neural core'. **c**–**e**, Backpropagation training results using 8 × 8 pixel images (small) (**c**), 28 × 28 pixel images (large) (**d**) and Sandia file classification dataset (**e**) using experimentally measured linear potentiation and depression ($V_{ds} < 0$). **f**–**h**, Backpropagation training results using 8 × 8 pixel images (small) (**f**), 28 × 28 pixel images (large) (**g**) and Sandia file classification dataset (**h**) using experimentally measured linear potentiation and depression without strain and with 50% strain ($V_{ds} > 0$). **i**, Schematic of the exploded view of the stretchable reconfigurable synaptic transistor array. The inset on the left image shows the device's top view. **j**, Optical images of the stretchable reconfigurable synaptic transistor array at the initial (left) and stretchable (right) states. **k**,**l**, Linear potentiation and depression of 25 devices in both p-type operation (**k**; $V_{ds} < 0$) and n-type operation (**l**; $V_{ds} > 0$), using which the device-to-device variations are calculated.

the other hand, the IPSC is defined as the case where positive pulses result in a decrease in the PSC or negative pulses result in an increase in the PSC[26].

The PSCs were characterized with the application of five successive presynaptic pulses for each operational region (Fig. 1c). Excitatory synapse in p-type operation: a presynaptic pulse (5 V (from −5 to −10 V); 250 ms) was applied to the gate with V_{ds} of −1 V (Fig. 1c(i)). Inhibitory synapse in p-type operation: a presynaptic pulse (10 V (from +5 to −5 V); 250 ms) was applied to the gate with V_{ds} of −1 V (Fig. 1c(ii)). Inhibitory synapse in n-type operation: a presynaptic pulse (10 V (from −7 to +3 V); 250 ms) was applied to the gate with V_{ds} of +1 V (Fig. 1c(iii)). Excitatory synapse in n-type operation: a presynaptic pulse (7 V (from +3 to +10 V); 250 ms) was applied to the gate with V_{ds} of +1 V (Fig. 1c(iv)). In region (i), for the device without strain and with 50% strain, the PSC increased when five successive negative pulses were applied to the gate (that is, EPSC) (Fig. 5e), which confirms the excitatory synaptic behaviour. In region (ii), the PSC decreased when five successive negative pulses were applied to the gate (that is, IPSC) (Fig. 5f), which indicates that the reconfigurable synaptic transistor can also act as an inhibitory synapse[27–29]. On stretching by 50%, the IPSC decreased, yet the synaptic behaviour remained. Similarly, in regions (iii) and (iv), the stretchable reconfigurable synaptic transistor shows EPSC (Fig. 5g) and IPSC (Fig. 5h), respectively. Note that the overall PSC was retained without notable performance degradation even when the device is stretched by 50%.

Figure 5i shows the single-pulse-induced EPSC results from a very low-amplitude presynaptic pulse (−80 mV, 250 ms) applied to the gate with V_{ds} of −1 V. An EPSC of ~1.67 nA was generated per pulse and decreased back to the initial state within 1.3 s. On the application of ten successive presynaptic pulses, the EPSC increased due to the accumulation of electrons at the interface of the PU gate dielectric and semiconductor (Fig. 5j). Figure 5k demonstrates a similar characteristic, corresponding to presynaptic pulses (+80 mV, 100 ms) applied to the gate with V_{ds} of +1 V. These characteristics mean that it might be possible to directly interface the device with biological neurons.

The energy consumption of a synaptic device, defined as IPSC × V_{ds} × t, is a critical measure, particularly for neuromorphic computing systems[30]. Figure 5l shows the single-pulse-induced EPSC results when presynaptic pulses (from +3 to +10 V) with variable pulse durations ranging from 50 to 1,000 ms were applied to the gate with V_{ds} of +10 V. The EPSC increased as the pulse duration increased. The peak currents of the EPSCs and energy consumption with respect to different pulse durations are presented in Fig. 5m. The energy consumption increases from 400 to 2,600 pJ when the pulse duration increases from 50 to 1,000 ms. Similarly, the single-pulse-induced EPSC results are shown in Supplementary Fig. 18a, when presynaptic pulses (from −5 to −10 V) with variable pulse durations ranging from 50 to 1,000 ms were applied to the gate with V_{ds} of −10 V. As the pulse duration increases, the EPSC and energy consumption increase accordingly. The peak current of the EPSC and energy consumption with respect to pulse duration are summarized in Supplementary Fig. 18b,c, respectively. The lowest energy consumption of the reconfigurable synaptic transistor is calculated to be 40 pJ (V_{ds} = +1 V), which is much lower than that of conventional complementary-metal–oxide–semiconductor-based synapse (~900 pJ per peak)[12]. The specific energy consumption, that is, the energy consumption per unit channel area, was calculated to be 0.11 pJ per 10^{-9} m^2. Figure 5n shows the summarized specific energy consumption of currently reported organic synaptic transistors[13,31–35]. Our reconfigurable synaptic transistor has a lower specific energy consumption than previously reported organic synaptic transistors[11–13], which is a critical feature in the development of neuromorphic computing.

Dual-directional image recognition

The bilingual synaptic weight updates enable the device to accomplish both single-directional[36] and dual-directional[37,38] learning processes in neuromorphic computing. Based on the measured binary synaptic weight updates of our reconfigurable synaptic transistor, we simulated a three-layer network (one hidden layer) for training with backpropagation based on its experimentally measured linear potentiation and depression[36,39]. The schematic of the ANNs for image recognition is shown in Fig. 6a. The circles and arrows represent the artificial neurons and connections between the input and output artificial neurons, respectively. The input neurons transmit the electrical signals to the next neurons regarding the conductance status. All the neurons are connected to each other through the artificial synapses. For network simulation, three different datasets were used as input patterns: 8 × 8 pixel images (small images) of handwritten digits from MNIST, 28 × 28 pixel images (large images) of handwritten digits and the Sandia file classification dataset[29,39–41]. Figure 6b presents the schematic of a stretchable crossbar array, which is a part of a 'neural core' to implement vector–matrix multiplication and outer-product update operations[29,36,40,42]. A total of 40 cycles for the ANNs in both ideal numerical and our artificial synaptic device were simulated. The trained reconfigurable synaptic transistor exhibited an accuracy of 96.26% for small digits, 94.81% for large digits and 93.00% for file types (Fig. 6c–e), respectively. Figure 6c, inset, shows the experimentally measured linear potentiation and depression in p-type operation (excitatory synapse, V_{ds} < 0). The eight write (−6 V, 500 ms) and eight erase (6 V, 500 ms) presynaptic pulses were applied with V_{ds} of −1 V. Linear potentiation and depression during 40 cycles are shown in Supplementary Fig. 19. The same simulation was also carried out in n-type operation (excitatory synapse, V_{ds} > 0) by taking advantage of binary synaptic weight update. Experimentally measured linear potentiation and depression without strain and with 50% strain are presented in Fig. 6f, inset. The eight write (7 V, 500 ms) and eight erase (−7 V, 500 ms) presynaptic pulses were applied with V_{ds} of 1 V. Successive linear potentiation and depression during 40 cycles without strain and with 50% strain are shown in Supplementary Fig. 20. The trained reconfigurable synaptic transistor showed an accuracy of ~93.59% for small digits, ~95.00% for large digits and ~91.00% for file types (Fig. 6f–h, respectively). Even when stretched by 50%, the device showed similar image recognition accuracy (Fig. 6h).

To demonstrate the device-to-device variation, we fabricated a stretchable reconfigurable synaptic transistor array. The schematic of the exploded view of the synaptic transistor array is shown in Fig. 6i. The fabricated synaptic transistor array operation was achieved by applying respective voltages through individual data and gate nodes, whereas the source nodes were grounded (Fig. 6i, inset). Figure 6j shows the optical images of the synaptic transistor array at the initial (left) and stretchable (right) states. The synaptic transistor array could endure uniaxial deformation due to the stretchable nature of all the materials used to fabricate the device. As described above, 25 synaptic transistors were characterized by measuring linear potentiation and depression under the same condition. The linear potentiation and depression measurements showed that device-to-device variations are approximately <7% (V_{ds} < 0) and <6% (V_{ds} > 0) (Fig. 6k,l, respectively), which shows good device-to-device uniformity of our devices. High image recognition accuracy and low device-to-device variation results even under 50% mechanical strain collectively indicate that the stretchable reconfigurable synaptic transistor could be used in soft neuromorphic computing.

Conclusions

We have reported an elastic, reconfigurable synaptic transistor that can exhibit inhibitory and excitatory synaptic characteristics. The synaptic functionality was achieved using a top-gated transistor with a stretchable bilayer semiconductor—consisting of a polymer film on s-CNT networks—as the channel and PU as the gate dielectric. The rubber dielectric encapsulation on the semiconductor thin film suppresses crack formation and propagation of cracks under mechanical stretching, as well as imparting long-term stability by providing

a physical barrier between the semiconductor and ambient environment. Due to all the materials being stretchable, the reconfigurable synaptic transistor retains its functions even when stretched by 50%. An ANN simulation using our reconfigurable synaptic transistor for dual-directional image recognition using the MNIST dataset showed recognition accuracy over 90% and under 50% strain. The lowest specific energy consumption of the reconfigurable synaptic transistor suggests that it is a promising candidate for neuromorphic computing in applications where large mechanical deformations are expected. Neuromorphic computing and recognition systems constructed using our elastic reconfigurable synaptic transistor could have a notably reduced number of transistors and simplified circuitry[43–45] compared with complementary metal–oxide–semiconductor technologies, and could be of use in applications such as soft neuromorphic computing systems[46], wearable electronics[47], soft robotics[48], neural interfaces[49] and human–machine interfaces[50].

Methods

Preparation of stretchable AgNWs/PDMS conductor

The AgNWs were patterned onto a glass substrate by drop casting the AgNWs solution (Agnw-120, ACS Material) through a shadow mask that was prepared by a programmable cutting machine (Silhouette Cameo), followed by baking at 95 °C for 10 min. The PDMS precursor (SYLGARD 184; weight ratio of prepolymer:curing agent is 10:1) was spin coated on the patterned AgNW electrode at 300 rpm for 60 s; the sample was then cured in an oven at 95 °C for 2 h. The preparation of AgNWs/PDMS composite electrodes was completed after the solidified AgNWs embedded in PDMS were peeled off from the glass substrate.

Preparation of N2200 semiconductor

The N2200 solution (5 mg ml^{-1}) was prepared by dissolving N2200 (M_W = 49 kDa; polydispersity index, 2.6; Flexterra) in mesitylene (98%, Sigma-Aldrich). Then, the solution was kept overnight in ambient conditions to fully dissolve the polymer in the solution. The prepared solution was spin coated on top of the channel region of the AgNWs/PDMS-composite-based stretchable electrodes through a Kapton-film-based shadow mask, followed by annealing at 150 °C for 1 h under a N_2 atmosphere.

Preparation of elastic PU gate dielectric

The PU (Selectophore grade, Sigma-Aldrich) was dissolved and stirred in tetrahydrofuran (anhydrous, ≥99.99%, Sigma-Aldrich) with a concentration of 75 mg ml^{-1} at 80 °C for 2 h and was coated on top of the N2200 film through spin coating at 1,000 rpm for 60 s. Then, the sample was annealed at 100 °C for 1 h.

N2200-thin-film-based synaptic transistor fabrication

The fabrication process of the stretchable synaptic transistor involved preparing the AgNWs/PDMS-conductor-based source and drain electrodes and spin coating the N2200 semiconductor and PU gate dielectric in a successive manner. Finally, the top gate based on liquid metal (gallium–indium eutectic, Sigma-Aldrich) was formed on top of the PU gate dielectric by a doctor-blading process with a shadow mask to complete the device fabrication.

Synaptic transistor fabrication based on s-CNT network

The source and drain electrodes were prepared in the same manner as mentioned above. The channel region was treated by exposing it under an ultraviolet/ozone lamp (BHK Inc.) for 18 min and 1% (3-aminopropyl) triethoxysilane solution for 10 min to develop the amine groups on the channel region. The s-CNT solution (IsoNanotubes-S, single walled; mean diameter, 1.4 nm; mean length, ~0.5 µm; purity, 98%; NanoIntegris Technologies) with a volume of 10 µl was dropped on the channel region and then dried at 90 °C for 10 min under ambient conditions. The formed channel was rinsed with deionized water to remove the surfactant and heated at 90 °C for 1 h. The PU gate dielectric and liquid metal were then added on top to complete the fabrication steps.

Stretchable reconfigurable synaptic transistor fabrication

The device fabrication was started by creating a stretchable source and drain electrode as mentioned above. The s-CNT networks and N2200 film were sequentially added on top of the channel region of the stretchable electrode through spin-coating and baking processes. Thereafter, the PU gate dielectric and liquid metal gate were constructed on top of the stretchable bilayer semiconductors to complete the device fabrication.

Stretchable synaptic transistor array fabrication

The stretchable reconfigurable synaptic transistor array fabrication started with the preparation of a stretchable AgNWs/PDMS electrode array (Supplementary Fig. 21). To prepare a layer with a stretchable synaptic transistor array, s-CNT networks/N2200 and PU were patterned on another AgNWs/PDMS electrode array, as described above. Then, via holes were formed through a hand puncher for interconnection between the layers. Finally, the layer with a stretchable synaptic transistor array (top) was assembled with the stretchable electrode array (bottom), followed by injecting liquid metal into the via holes to complete the stretchable reconfigurable synaptic transistor array fabrication (Supplementary Fig. 22).

Material characterization and device measurements

The frequency-dependent capacitance of the PU was measured by an impedance analyser (M204, Autolab). The measurement of the synaptic transistor was carried out using a semiconductor analyser (4200SCS, Keithley Instruments). A function generator (DG4062, RIGOL Technologies) was used to apply the presynaptic pulses to the gate electrode, and the PSC was measured by applying constant V_{ds}.

Data availability

The data that support the findings of this study or additional data related to this paper are available from the corresponding author upon request.

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Acknowledgements

C.Y. would like to acknowledge financial support from the Office of Naval Research grant (N00014-18-1-2338) under the Young Investigator Program, as well as the National Science Foundation grants of CAREER (1554499), EFRI (1935291) and CPS (1931893 and 2227062). T.J.M. and A.F. acknowledge support from the Air Force Office of Scientific Research grant (FA9550-18-1-0320 and FA9550-22-1-0423) and the Northwestern University MRSEC grant National Science Foundation DMR (1720139).

Author contributions

H.S. and C.Y. conceived and designed the research. H.S., S.P. and Y.Z. performed the experiments. H.S. and C.Y. analysed the data. H.S. and F.E. performed the simulation work. B.W., Z.C., T.J.M. and A.F. provided the materials and advised on the experiment. H.S. and C.Y. wrote the manuscript. All the authors revised the manuscript.

Competing interests

The authors declare no competing interests.

Additional information

Supplementary information The online version contains supplementary material available at https://doi.org/10.1038/s41928-022-00836-5.

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Peer review information *Nature Electronics* thanks Huipeng Chen, Zheng Yan and the other, anonymous, reviewer(s) for their contribution to the peer review of this work.