Transmission Electron Microscopy Study on the Effect of Thermal and Electrical Stimuli on Ge_2Te_3 based Memristor Devices

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Abstract

Memristor devices fabricated using the chalcogenide Ge_2Te_3 phase change thin films in a metal-insulator-metal structure are characterized using thermal and electrical stimuli in this study. Once the thermal and electrical stimuli are applied, cross-sectional transmission electron microscopy (TEM) and X-ray energy-dispersive spectroscopy (XEDS) analyses are performed to determine structural and compositional changes in the devices. Electrical measurements on these devices showed a need for increasing compliance current between cycles to initiate switching from low resistance state (LRS) to high resistance state (HRS). The measured resistance in HRS also exhibited a steady decrease with increase in the compliance current. High resolution TEM studies on devices in HRS showed the presence of residual crystalline phase at the top-electrode/dielectric interface, which may explain the observed dependence on compliance current. XEDS study revealed diffusion related processes at dielectric-electrode interface characterized, by the separation of Ge_2Te_3 into Ge- and Te- enriched interfacial layers. This was also accompanied by spikes in O level at these regions. Furthermore, in-situ heating experiments on as-grown thin films revealed a deleterious effect of Ti adhesive layer, wherein the in-diffusion of Ti leads to further degradation of the dielectric layer. This experimental physics-based study shows that the large HRS/LRS ratio below the current compliance limit of 1 mA and the ability to control the HRS and

LRS by varying the compliance current are attractive for memristor and neuromorphic computing applications.

1 Introduction

Recently, various nanoscale memory devices have been demonstrated by the scientific community, which have the potential to store data in very high density and design new in-memory computing systems which mimic cognitive behavior for information processing, such as synaptic modifications, postsynaptic currents, and memory consolidation [1]. Memristor is one of the most studied devices for the new paradigm computing system. Leon Chua proposed the mathematical model of the memristor in 1971, which was claimed as the missing fourth fundamental element of the electrical circuits [2]. The proposed memristive behavior was first realized after the nanoscale model [3] and experimental fabrication [4]. The signature characteristics of the presence of memresistance of a nanoscale device is the current-voltage relationship that shows a pinched hysteresis loop through the origin [5]. This property makes the device a suitable candidate for performing as a non-volatile memory device. The most vital characteristic of a memristor is that the conductance can be modified dynamically with input excitation. This dynamic behavior allows a memristor to be utilized as an artificial synapse which is a fundamental building block for hardware-based neuromorphic computing [6]. In addition, memristors can be laid out in a high-density grid known as a crossbar structure [7], which gives them the potential to be fabricated with an areal density greater than that of synapses in the human brain [8]. These crossbars can be used to produce high density, extremely low-power, neuromorphic hardware capable of performing many parallel operations in the analog domain [9].

Recent studies based on the simulation of memristor crossbars show promising results with these large high-density structures. Furthermore, it has been shown that neuromorphic systems based on memristor crossbars have potential to perform at a power efficiency of 6 to 8 orders of magnitude lower than that of traditional RISC processors [7]. For ultra-high data storage and low power computing, many materials and devices have been investigated, such as resistive memory [3,10], ferroelectric materials [11], magnetic materials [12,13], and phase change materials (PCMs) [14].

PCMs attract more attention among the candidate materials due to their very high switching efficiency, stable data retention, long data endurance, and extraordinary scalability [15-18]. In addition, their rapid phase transition, low energy consumption, stability at high temperature, and structural distinctiveness in the crystalline and amorphous states [15] are attractive for fabricating phase-change random access memory (PCRAM) [16] and electrical probe memory [17]. The electrical properties of PCMs (e.g., resistivity/conductivity) can be controlled continuously by external stimulus, which opens application areas such as synaptic devices (memristor) and neuromorphic circuits [18].

For PCMs to change from amorphous to crystalline phase, they need to be heated to a temperature that allows crystallization. For phase transition from crystalline to amorphous phase, the temperature needs to be high enough to melt the material and then be rapidly cooled to freeze it in the amorphous/disorganized state. To affect the phase changes in the PCM based memristor, the PCM is sandwiched between bottom and top electrodes to create a metal/insulator/metal (MIM) structure. The MIM structure gives the ability to electrically bias the device and change its state through the flow of electrical current and the resulting Joule heating. To heat the structure to its

melting point, a fast and a higher amplitude pulse is applied, quickly raising the temperature, followed by a rapid freeze causing the formation of the amorphous state / high resistance state (HRS). To change the device to its crystalline state / low resistance state (LRS), a voltage pulse with lower magnitude and longer width is applied which allows the device to be heated to a temperature that crystalizes the structure well below its melting point [19], [20], [21], [22]. The large HRS/LRS ratio possibility in PCM based memristors is attractive for analog neuromorphic computing as one can obtain multiple resistance states corresponding to synapse weights.

In this study, we will focus on Ge_2Te_3 (GeTe), a chalcogenide PCM and investigate its phase change characteristics in a memristor structure through thermal and electrical stimuli [23, 24]. Once the thermal and electrical stimuli are applied, we compare results gathered from transmission electron microscopy (TEM) and X-ray energy-dispersive spectroscopy (XEDS) analyses to determine structural and compositional changes in the devices. The electrical measurements are corelated to the structural and compositional changes in the devices.

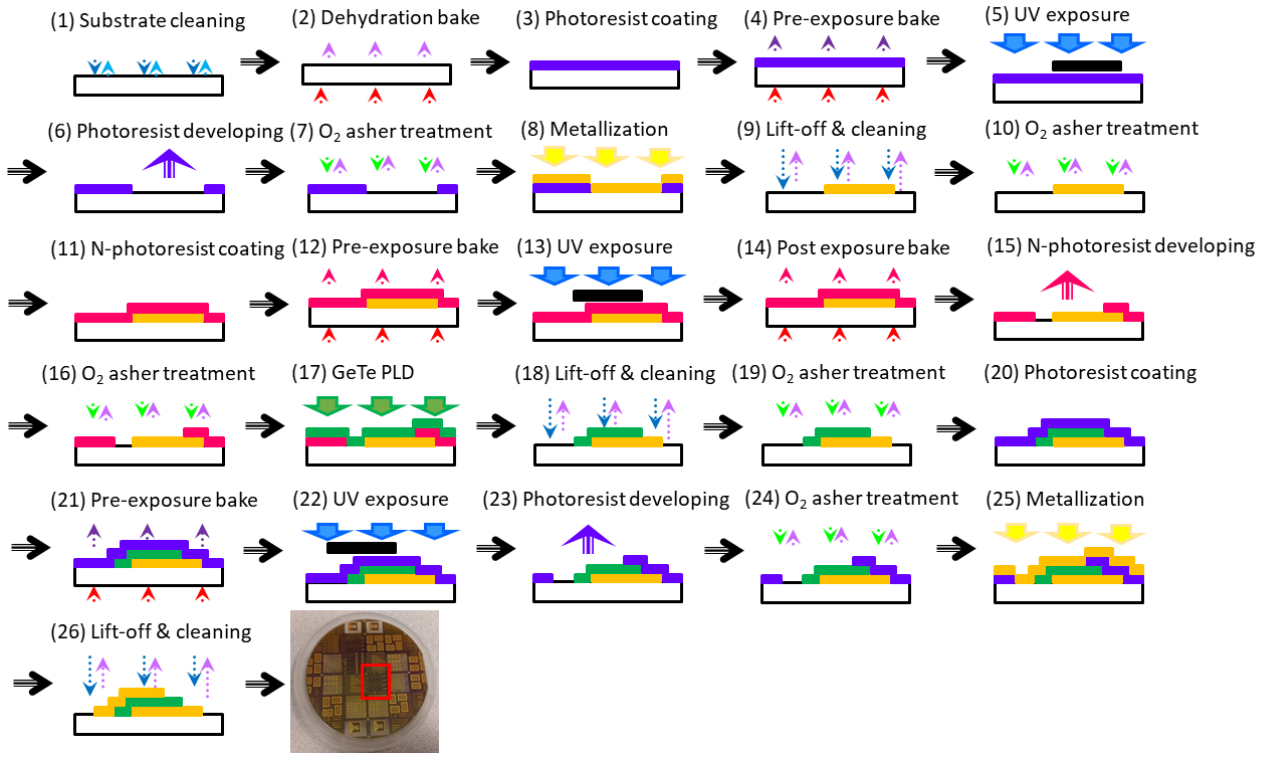
2. Experimental Methods

2.1 Fabrication

The GeTe-based memristor devices presented in this work were deposited in a Metal-Insulator-Metal (MIM) stack on Si wafers. The 5 µm x 5 µm devices were fabricated on a 100 nm thermal SiO_2 coated high resistivity Si(100) wafer. Each device consists of a bottom metal electrode stack of Ti+Pt, a GeTe thin film layer, and a top metal electrode stack of Ti+Pt as shown in Fig. 1. For patterning, the bottom and top electrodes, conventional photolithography, and lift-off processes were utilized as shown in Fig. 1a. The top and bottom metal electrodes were deposited by e-beam evaporation technique. A 50 nm-thick GeTe thin film was grown as the memristive switching layer by pulsed laser deposition (PLD) technique on the bottom electrode stack. The GeTe film is sandwiched between the bottom and the top electrodes as shown in Fig. 1b.

For fabricating the GeTe thin films, a homemade PLD system was utilized. The separation distance between the target and substrate was 50 mm, and the output of a KrF eximer laser (λ = 248 nm) was used to ablate a GeTe target. The laser energy density at the target surface was set to approximately 3.6 J/cm^2, and the laser repetition rate was maintained at 10 Hz. During the deposition process, the PLD chamber pressure and the substrate temperature were maintained below 1×10^{-5} Torr and room temperature (< 25 °C). For synthesizing 50 nm-thick film, 200 laser pulses were used.

(a)



(b)

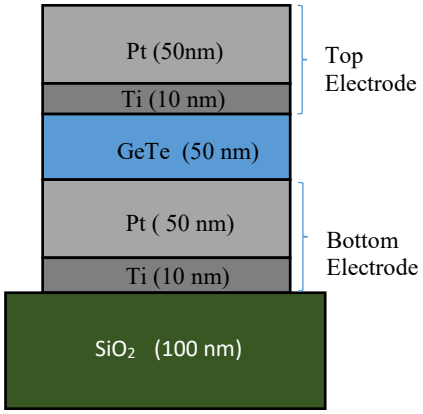


Figure 1 (a) Detailed steps in the device fabrication process and (b) the cross-section of the final device structure.

2.2 Characterization

Samples for TEM observation were prepared by focused ion beam (FIB) milling using a Ga source. Before TEM observation, an additional cleaning procedure was performed by Ar-ion milling to reduce the surface amorphous layer and residual Ga that could be deposited due to the FIB process. The TEM observations were performed using a Talos 200-FX (ThermoFisher Scientific) TEM operated at an acceleration voltage of 200 kV. The samples were imaged using conventional high-resolution TEM (HRTEM) and high-angle annular dark-field scanning TEM (HAADF-STEM) techniques. In addition, X-ray energy dispersive spectroscopy (XEDS) measurements were performed in the HAADF-STEM mode, using the ChemiSTEM^{TM} (ThermoFisher Scientific) technology. Acquisition and processing of the XEDS data was performed by spectrum imaging technique using the Esprit 1.9 (Brucker Inc.) software.

The electrical characterization measurements were carried out using a MicroXact probe station and Keysight B1500A semiconductor analyzer with two waveform generators/fast measurement units (WGFMU) modules. The set (crystallization) and reset (amorphization) processes of the GeTe memristors were preformed utilizing electrical pulses. The set pulse has an amplitude of 2.5 V, with a pulse-width of 15 µs, a rise time of 1 ns and a fall time of 5 µs. The reset pulse has an amplitude in the range of 4 – 10 V with a pulse-width of 1 µs and a rise and fall time of 1 ns. Since devices are switched between the high and low resistance states, a read operation is performed using a low voltage DC sweep from 0-100 mV to determine the change of resistance between the HRS and LRS. Due to the lower voltage compared to the set and reset process, the GeTe layer does not undergo any phase changes during the read operation and will maintain that resistance until another pulse with sufficient potential is applied to the device. Devices were also cycled using a DC voltage sweep from -2 V– +4 V – -2 V with various current compliance (CC) limits.

3. Results and Discussions

3.1 Electrical Measurements

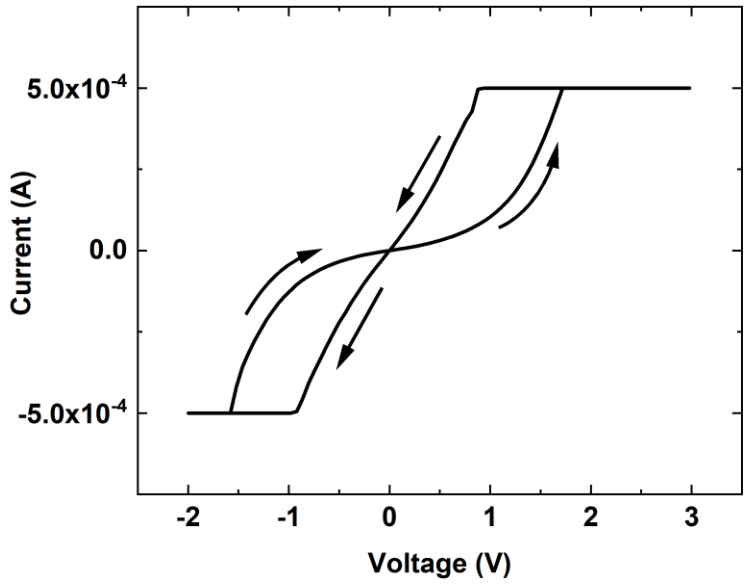
Devices were first tested for proper switching through the set and reset pulses. By applying repetitive set pulses, the devices were locally heated to > 250 °C causing crystallization to occur. After setting the devices to the LRS, the device resistance was between 1.5 kΩ to 20 kΩ. A single reset pulse is applied to reset the device in the HRS. Once reset, the resistance would typically read approximately 500 kΩ or show open circuit indicating that the analyzer could not measure any current through the device.

Additionally, with the information gathered from the TEM analysis on the heated device showing a significant change in its structure, devices were then tested under strenuous electrical stimuli to determine if similar structural changes are observed for electrical tests. Devices were first cycled with a 500 µA current compliance (CC) limit which was then increased to 1 mA, 1.5 mA, 2 mA, and 5 mA. After multiple cycles at the 500 µA CC limit, the hysteresis loop began to pinch (Fig. 2 a,b), showing little to no changes in resistance. After 5 DC sweeps the device showed a completely pinched hysteresis. When increasing the CC, no pattern was observed in the number of cycles required to see the pinched hysteresis loop. It was determined that the negative voltage during the DC sweep drove the device's resistance further into the LRS, causing the pinching of the hysteresis. This pinching represents a unipolar switching behavior for the devices due to the

phase change characteristic of GeTe. Once a completed pinched hysteresis was observed at the 500 µA CC limit, the device's LRS was read at approximately 5 kΩ. To switch the device into its HRS after cycling, the 1 µs and 4 V reset pulse was applied. After resetting, the device's resistance showed an increase to approximately 100 kΩ. Due to the device not reaching its previous HRS values of approximately 500 kΩ, the pulse amplitude was increased to 6 and 8 V but no further change in resistance was observed.

The previous process was then repeated with an increased CC limit of 1 mA. The results showed similar properties when compared to the 500 µA tests. The LRS resistance after cycling was 2 kΩ, which indicates that the higher CC limit also causes a lower resistance. After resetting, the highest obtainable resistance was now 25 kΩ compared to the previous 100 kΩ. The device was then retested at a 500 µA CC limit to determine if it will maintain similar I-V characteristics to the previous 500 µA cycles. It was observed that the device was already near a completely pinched hysteresis loop. Without resetting, the CC limit is raised back to 1 mA and a more evident change in resistance is observed (Fig. 2c). This indicates that the device is no longer operational at CC limits less than 1 mA. Furthermore, after the 1.5 mA, 2 mA and 5 mA CC limit testing the same trend is observed. As illustrated in Fig. 3a, the LRS resistance values continue to decrease to approximately 1.5 kΩ, 1 kΩ, and 850 Ω. Concurrently, the HRS resistance values drop to approximately 10 kΩ, 8 kΩ, and 5 kΩ. With the continued decrease in the HRS's highest achievable resistance under increasing current compliance indicates that an irreversible process is taking place within the device.

(a)



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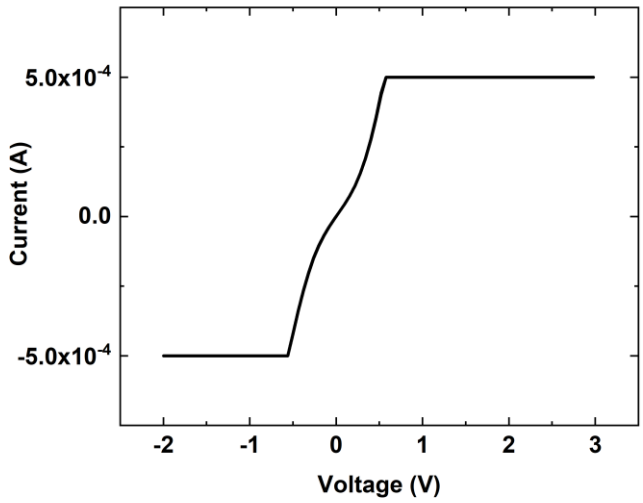

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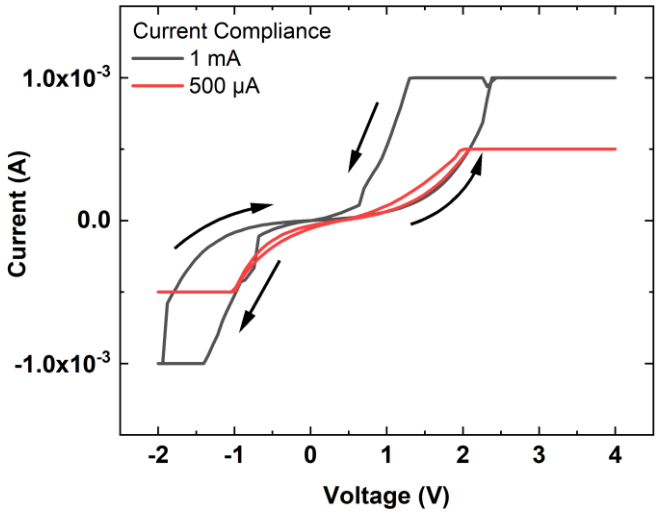


Figure 2 Plot of the I-V characteristic GeTe memristor showing switching behavior in the form of a hysteresis loop (a) and pinched hysteresis (b), (c) DC voltage sweep at 500 µA current compliance after cycling at 1 mA (red) and a DC voltage sweep at 1 mA after the 500 µA sweep (black).

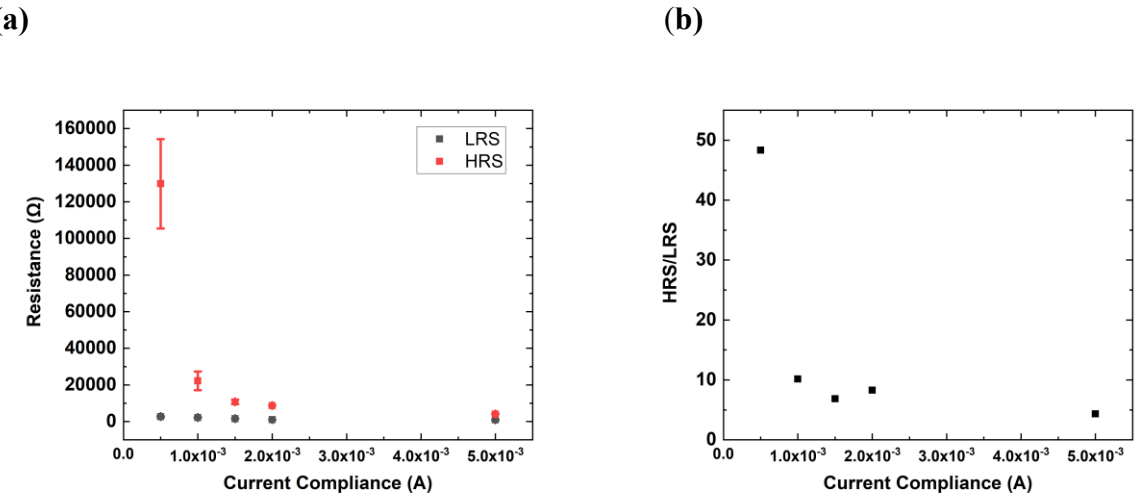


Figure 3 a) Low resistance state values following DC sweeps at current compliances of 500 µA, 1 mA, 1.5 mA, 2 mA and 5 mA (black) and high resistance state values following each reset pulse (red) for a single device b) HRS/LRS ratio for each current compliance.

In spite of the dropping HRS and LRS levels, the ratio of the HRS/LRS stays close to 10 up to a CC of 2 mA and drops down to roughly 5 at a CC of 5 mA as shown in Figure 3b. HRS/LRS ratio above 10 is possible if we operate below the CC of 1 mA. This region below CC of 1 mA could be useful for low power neuromorphic computing. Clearly, the HRS values and the HRS/LRS ratio are tunable by varying the current compliance. This could be useful for implementing artificial synapses in neuromorphic processors.

3.2 TEM Analysis

TEM investigations were performed on the PCM based memristor devices to understand the HRS dependence on current compliance presented in Figure 3. While the switching between the two resistance states is primarily driven by amorphous to crystalline transition due to electrical bias induced Joule heating, it is important to note that the atomistic processes at the dielectric/electrode interface may also play a role in the observed dependence. Based on these considerations, the TEM analysis was focused on two aspects: HAADF-STEM/XEDS studies to examine compositional changes due to inter-diffusion at the dielectric/electrode interfaces and HRTEM imaging to examine structural changes in the overall device region. Furthermore, these investigations were performed on samples extracted from actual devices and compared with in-situ heating experiments performed on GeTe thin films in the as-grown condition (prior to device fabrication).

Figure 4 shows the XEDS map (a) and the corresponding line profiles of elemental distribution (b) across the device structure. These results were obtained from the device tested in Figure 3 with a final compliance current of 5 mA. An examination of Ge and Te profiles (Fig. 4b) reveals separated spikes adjacent to the top electrode region, indicating dissociation of Ge_2Te_3 into Ge- and Te- enriched regions. In addition, the formation of enriched regions is accompanied

(a) **(b)**

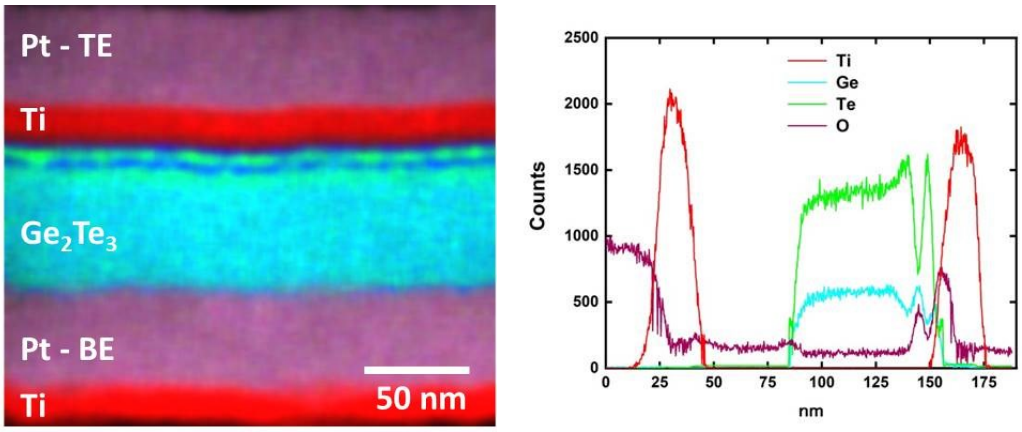


Figure 4 (a) XEDS map and (b) elemental line profiles of overall device structure after electrical biasing. Note that the top and bottom Pt electrodes are abbreviated TE and BE, respectively.

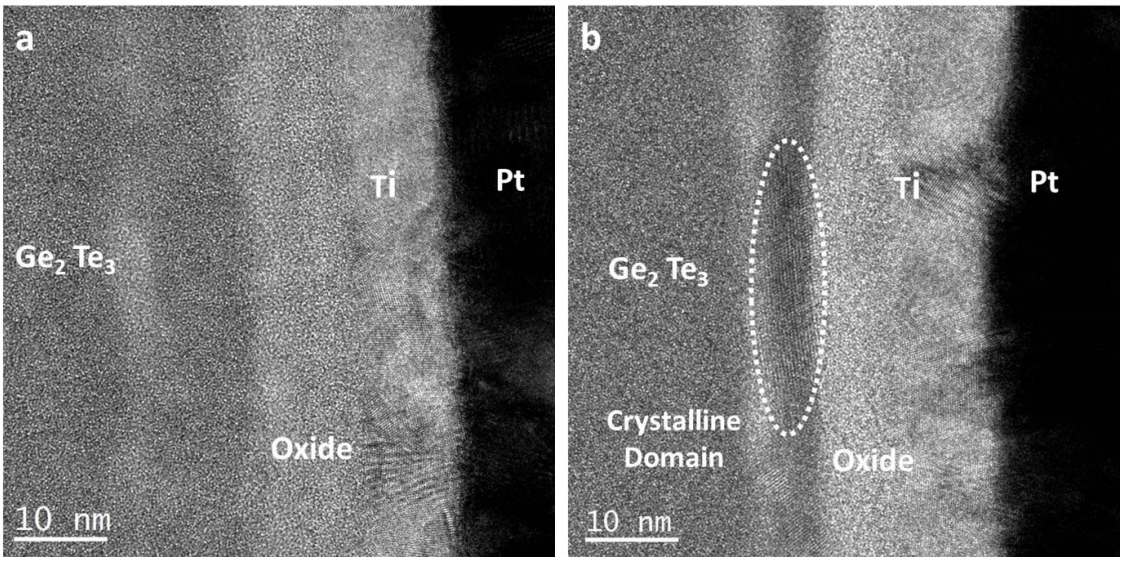


Figure 5 HRTEM image of top dielectric/electrode interface showing (a) an amorphous structure in Ge_2Te_3 prior to electrical biasing and (b) the presence of a crystalline domain in dielectric/ electrode interface after cyclic electrical biasing to HRS (enclosed in the dotted region).

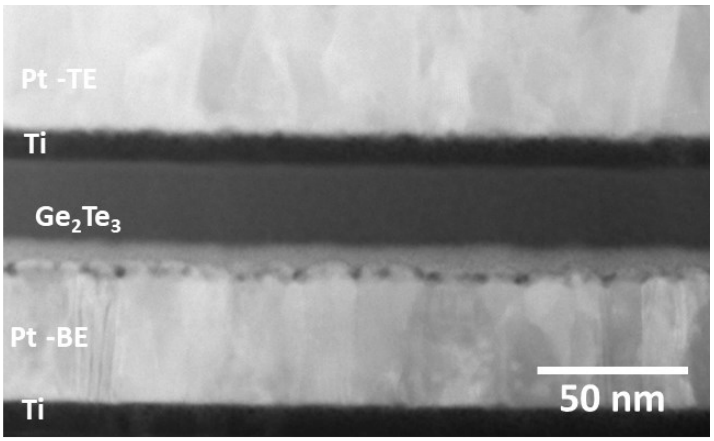
by spikes in the O profile. The dissociation of Ge_2Te_3 appears as alternating green and blue bands adjacent to the top Pt electrode in XEDS map (Fig. 4a). Although not shown, similar results were also observed in the XEDS data obtained from devices in the unbiased condition, indicating that Ge_2Te_3 is triggered by surface oxidation during device processing.

Further studies were performed by HRTEM to examine the structure of Ge and Te enriched interfacial layers observed in the XEDS maps. The HRTEM images of the top electrode region extracted from devices before and after electrical biasing are shown in Figures 5 (a) and (b), respectively. The region corresponding to the spike in O profile is identified in the two images. Furthermore, the regions corresponding to the Ge- and Te- enrichment in the XEDS map are revealed by subtle change in contrast in the Ge_2Te_3 region adjacent to the oxide layer. An examination of the region beneath the oxide layer in the unbiased sample (Fig. 5a) shows the expected amorphous structure. However, an examination of a similar region in the electrically biased sample (Fig. 5b) clearly shows the presence of a crystalline phase, indicating phase change due to Joule heating.

To further understand the results from the XEDS and HRTEM described above, an in-situ heating experiment was performed on device structures in the as-grown condition, with the temperature gradually raised in steps of 20 ºC up to 450 ºC. HAADF-STEM imaging and XEDS measurements were performed at different step intervals, after allowing settling time for sample thermal drift. Figure 6 shows the HAADF-TEM images of device structure in the as-grown condition (Fig. 6a) and after heating to 200 ºC (Fig. 6b), wherein the individual layers are identified. Significant changes in contrast are evident at the interfacial regions adjoining the Ge_2Te_3 layer and the top/bottom electrodes. In particular, we observe the appearance of additional layers in the vicinity of the Ti adhesive layer at the top electrode interface. Furthermore, HRTEM image of the Ge_2Te_3 layer (Fig. 6c) after heating to 200 ºC indicated crystalline phase formation (it is noted that the HRTEM image of Ge_2Te_3 layer at room temperature showed amorphous structure as in Fig. 5a). The formation of crystalline phase could explain the lowering in resistance observed in Fig. 3. Furthermore, its persistence could also explain the need for higher compliance current to initiate switching.

To understand the origin of the observed change in contrast at the top electrode in the HAADF-STEM images, we compared the XEDS maps acquired at room temperature (Fig. 7a) and at 200 ºC (Fig. 7b). A comparison of the two maps reveal significant intermixing upon heating at the top Ti/Ge_2Te_3 interface as indicated by the presence of a distinct green band corresponding to this region in Fig. 7b. Further insight on the nature of this intermixing is gained by examination of the line profile of the individual elemental distribution across layers in the device structure shown in Fig. 8. The aforementioned spikes in the Ge and Te distribution are present in the as-grown condition at room temperature (Fig. 8a), although to a lesser degree in comparison to those observed in Fig. 4, presumably due to lower O level observed in the line profile. However, upon heating to 200 ºC significant increase of Ge- and Te- spikes is evident, which is also accompanied by noticeable increase in the O-profile. Furthermore, a comparison of Ti profile shows noticeable change in Ti at the top electrode after heating, as indicated by a shrinking in profile closer to the electrode and the presence of a shoulder in the region corresponding to the spike in the Te profile. In comparison, the Ti profile at the bottom electrode does not exhibit noticeable change upon heating. The XEDS profiles indicate significant in diffusion of Ti, which upon further heating results in the eventual dissolution of Ti into the Ge_2Te_3 layer as shown in the XEDS maps in Fig.9.

(a)



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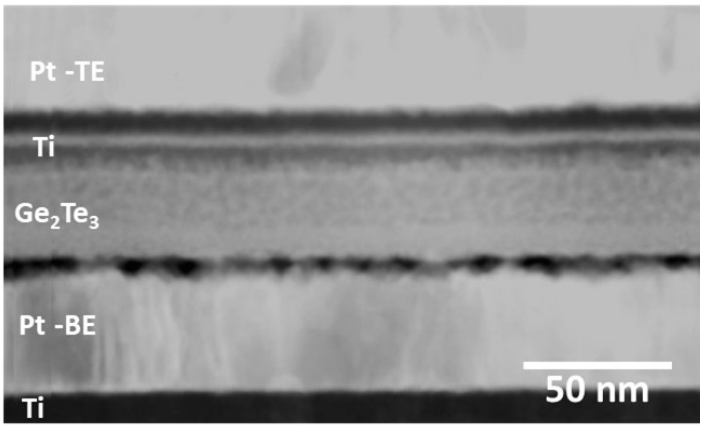

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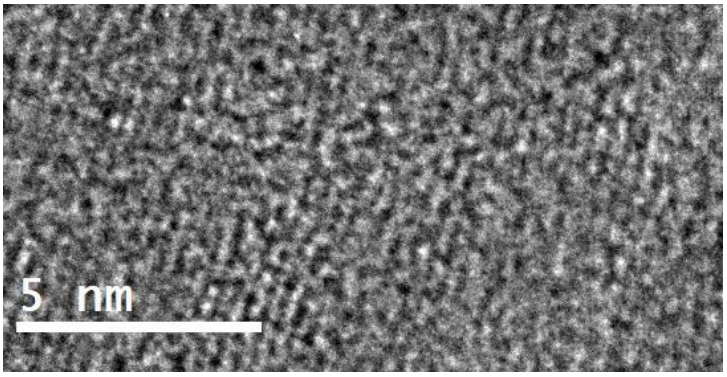
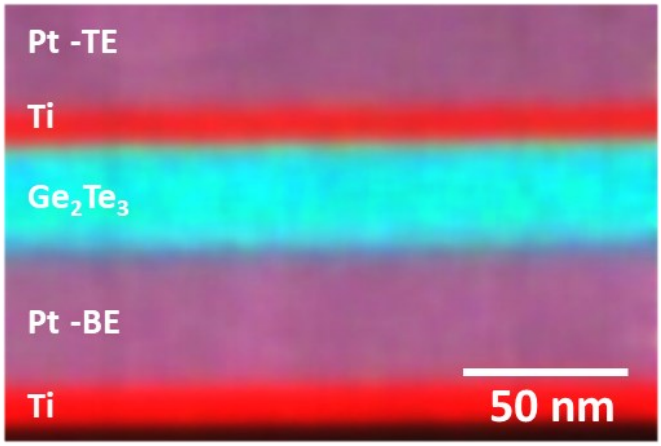


Figure 6 HAADF-STEM images showing the overall device structure in (a) as-grown condition at room temperature, (b) after heating to 200 ºC and (c) HRTEM image of Ge_2Te_3 after heating to 200 ºC

(a)



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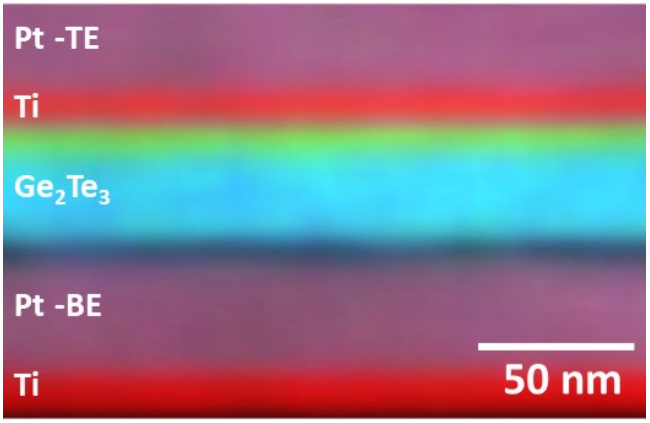

Figure 7 XEDS maps of the device structure (a) in the as-grown condition at room temperature and (b) after heating to 200 ºC.

(a) **(b)**

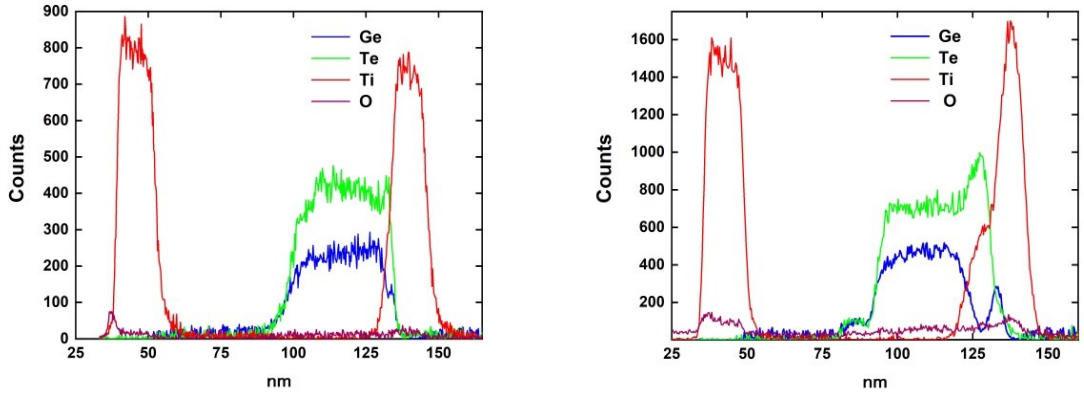

Figure 8 Elemental Line profiles from the XEDS maps of the device structure (a) in the preformed condition and (b) after heating to 200 ºC

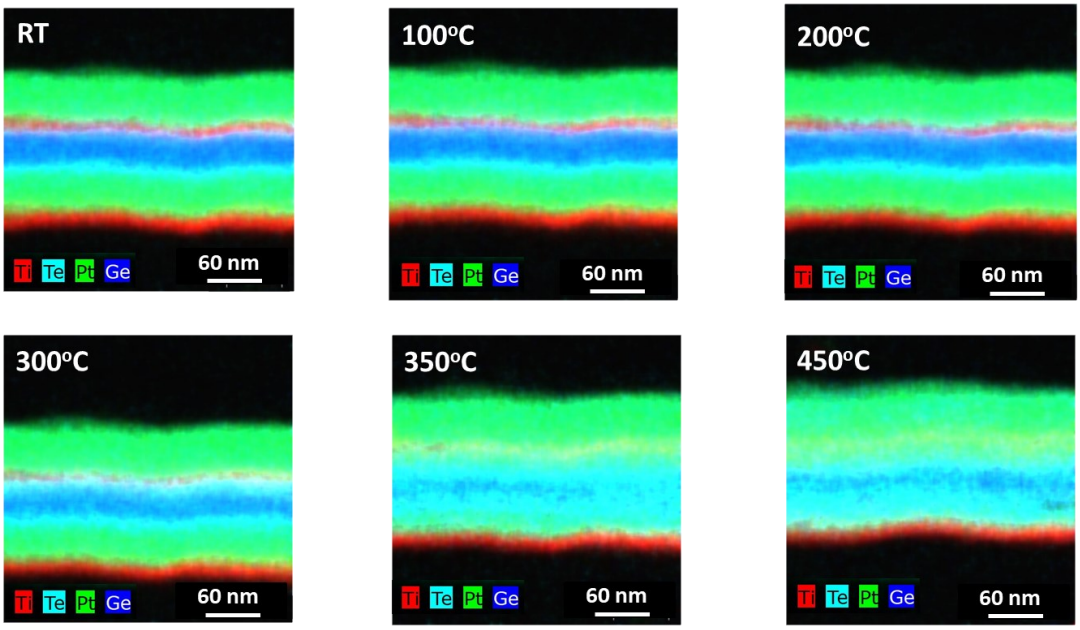

Figure 9 Composite XEDS elemental maps obtained from in-situ heating experiments starting at room temperature (RT), showing in-diffusion of Ti into the Ge_2Te_3 layer with increase in temperature.

The role of O observed in the in-situ TEM heating experiments are consistent with the results reported in the literature, wherein the Ge_2Te_3 separation is caused by an oxidation process triggered by preferential migration of Ge towards the surface [26]. In addition, the oxidation could also result in a lowering of the crystallization temperature and resistivity which supports the observations made in the HRTEM imaging and electrical biasing experiments. In this study, the

oxidation process seems to be enhanced much more during the device fabrication process due to the break in vacuum after the deposition of the electrodes. It is also worth noting that the observations pertaining to Ti diffusion are also consistent with earlier annealing studies reported on bulk samples [27], indicating that the effect of TEM sample preparation is not significant in the present study. Although the XEDS profiles may seem to indicate that the Ti diffusion in the electrically biased samples is not as drastic as those seen in the in-situ heating experiments, it should be noted that the heating experiments were performed over several minutes, whereas bias experiments are conducted over shorter pulses. The deleterious effect of Ti diffusion is still likely to be relevant for reliable device operation in the long-term. These observations indicate the need for developing mature processing steps to combat the effects of O and Ti in Ge_2Te_3-based memristor devices.

Conclusion

Memristor devices fabricated using the chalcogenide Ge_2Te_3 phase change thin films in a metal-insulator-metal structure are characterized using thermal and electrical stimuli in this experimental study. A cross-sectional transmission electron microscopy (TEM) study is performed to investigate microstructural phenomena that control the switching behavior and integrity of the dielectric-electrode interface in Ge_2Te_3-based memristor devices. We report successful switching of the GeTe memristors with distinct high and low resistance states. Electrical measurements on these devices showed steady decrease in resistance at HRS and a higher compliance current required to initiate LRS to HRS switching. Cross-sectional TEM studies indicate that this dependence could be explained by crystalline phase formation at around 200 ^{o}C. However, the separation of the GeTe layer with the spike in oxygen upon heating and diffusion of Ti adhesive layer could have a significant influence on the switching characteristics. This experimental study shows that the ability to control the HRS and LRS by varying the compliance current are attractive for implementing artificial synapse in neuromorphic computing applications.

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Conflict of Interest Statement:

Krishnamurthy Mahalingam is employed by UES, Inc. 4401 Dayton-Xenia Road, Dayton, OH 45432

Cynthia T. Bowers is employed by UES, Inc. 4401 Dayton-Xenia Road, Dayton, OH 45432

Albert Hilton is employed by UES, Inc. 4401 Dayton-Xenia Road, Dayton, OH 45432

Benson Athey was employed by UES, Inc. 4401 Dayton-Xenia Road, Dayton, OH 45432

The remaining authors declare that the research was conducted in the absence of any commercial or financial relationships that could be construed as a potential conflict of interest.

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