

Far-End Crosstalk Modeling and Prediction for Stripline With Inhomogeneous Dielectric Layers (IDLs)

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Abstract—Far-end crosstalk (FEXT) is a critical factor that limits signal integrity performance in high-speed systems. The FEXT level is sensitive to the dielectric inhomogeneity of the stripline in fabricated printed circuit boards (PCBs). The dielectric of the stripline is manufactured with multiple inhomogeneous dielectric layers (IDLs) of various resin and glass fiber bundles. A marginal difference in the dielectric permittivity of the IDLs can lead to a significant change FEXT level. In this article, a practical FEXT modeling methodology for striplines is proposed by introducing the extraction method for ϵ_r of IDLs. The new stripline model is constructed with three IDLs comprised of core, prepreg, and resin pocket, to improve the model accuracy. With the cross-sectional geometry and measured S-parameters of the coupled striplines, ϵ_r of IDLs can be extracted. In addition, an analytical model to predict the FEXT polarity and magnitude of the stripline caused by the inhomogeneity is proposed targeted for prelayout application. The proposed models have been verified using measurement. The proposed models can provide useful analysis methodology and design guidelines to mitigate the FEXT level in high-speed systems, especially for high-volume PCB tests in the prelayout and postlayout stages.

Index Terms—Delta-L, dielectric material, dielectric material property, extended unterminated line (EUL), far-end crosstalk (FEXT), inhomogeneous dielectric layers (IDLs), stripline.

I. INTRODUCTION

Far-END crosstalk (FEXT) needs to be well-controlled in the high-speed system design to avoid system failure due to signal integrity issues [1], [2], [3]. Therefore, during the prelayout stage, it is important to model and reduce the FEXT of high-speed channels before fabrication to meet the high-speed system design margins [4], [5], [6].

The inhomogeneity of the dielectric material is reported as a significant contributor to the FEXT [5], [6], [7]. In the fabrication

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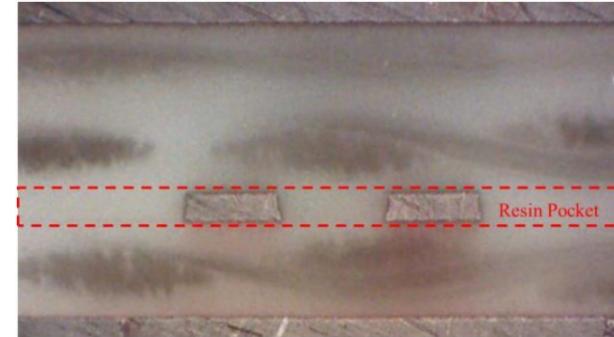


Fig. 1. Cross section of a pair of coupled stripline. The resin pocket is indicated with a dotted boundary.

of the printed circuit board (PCB), the dielectric material is laminated with different glass fiber and resin, which constructs the inhomogeneous dielectric layers (IDLs) [7], [8]. The dielectric permittivities (ϵ_r) of the resin and glass bundles are different, typically around 3 (resin) and 5 to 7 (glass), respectively. The difference in phase velocities of even and odd mode signals caused by IDLs results in nonzero FEXT noise in striplines. A marginal difference in dielectric permittivity can result in a significant FEXT level difference. For example, a difference of 0.1 between the permittivity of the core and prepreg layer could result in tens of millivolts crosstalk for a 3-in stripline in the worst cases [7] (see Fig. 4).

Stripline is typically modeled with a two-layer (2L-IDL) model constructed with a core layer and prepreg layer, which can only model the inhomogeneity between two layers. In this article, a new model with multiple IDLs (e.g., 3L-IDL model) is proposed. A model with more than three IDLs can be generated if given enough information about the glass weaves and resin content. Each IDL has different dielectric permittivity, which is a closer model of the fabricated stripline to the real products.

The additional third layer, sometimes also named “resin pocket,” is the layer that is only filled with resin between the core and prepreg layer, as is shown in Fig. 1. It is formed by resin flowing into metal gaps during the lamination process. Since the resin pocket fills the area between the two coupled traces and with a

different dielectric constant, it has a critical influence on the SI

performance of the stripline. The 3L-IDL model constructed with the resin pocket provides a more accurate representation of an actual fabricated stripline compared to a typical 2L-IDL model [9].

In order to characterize the FEXT due to the IDLs, ϵ_r of each IDL in the new model needs to be determined. Previously reported models only extracted ϵ_r of prepreg and core layers. In this article, an approach to extract ϵ_r of IDLs for the new three-layer model is proposed.

The method is validated with measurement results using a test stripline structure with the extended unterminated line (EUL) and Delta-L structures, which is widely used for high-volume PCB tests [10], [11]. The EUL structure is designed for convenient and accurate FEXT measurements, which allows only half the needed test ports while excluding the impact from FEXT due to mismatched terminals. Delta-L structures are differential striplines with different lengths [12]. With the de-embedding procedure [13], [14], [15], the vias and fixture effect can be removed so that S-parameters of the stripline is obtained. With the extracted ϵ_r of IDLs for the new three-layer model, more accurate modeling of the FEXT waveform can be achieved.

The superposition method in [4] provides a practical way to analyze and model the FEXT of the stripline in multilayer IDLs. Using the same superposition principle, the FEXT caused by the inhomogeneity of three IDLs can be decomposed into the FEXT of two sets of 2L-IDL models. Furthermore, an analytical model is proposed to predict the polarity and magnitude of FEXT in striplines caused by the IDLs. The analytical model does not require any results from the 2-D or 3-D simulation tools. The analytical model can be applied for both the traditional 2L-IDL model and the newly proposed 3L-IDL model.

As part of this article organization, in Section II, FEXT due to the IDLs is discussed. The FEXT analysis methodologies for the stripline with three IDLs are explained. Section III presents the extraction algorithm for ϵ_r of IDLs using Delta-L and EUL design. Section IV provides an analytical model and verification using measurement results. Finally, Section V concludes this article.

II. FEXT ANALYSIS METHODOLOGY

A. FEXT Caused by IDLs

FEXT noise is caused by the coupling between transmitting lines when the signal propagates from the transmit end to the receiving end. The modal analysis for the FEXT [16] separates the aggressor signal into even and odd modes and propagates through the coupling pair with different velocities

$$V_{\text{fext}} = V_{\text{even}} + V_{\text{odd}}$$

The odd and even phase velocities ($v_{p,\text{odd}}$, $v_{p,\text{even}}$) can be expressed using the per-unit-length (PUL) model inductance (L_m) and capacitance (C_m)

$$v_{p,m} = \frac{1}{\sqrt{L_m C_m}} \quad (1)$$

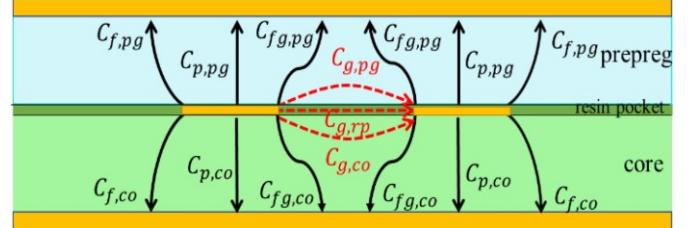


Fig. 2. Illustration of the capacitance components for the coupled striplines. The dielectric permittivity in prepreg, resin pocket, and core are $\epsilon_{r,pg}$, $\epsilon_{r,RP}$, and $\epsilon_{r,co}$, respectively.

TABLE I
DEFINITION OF THE DECOMPOSED CAPACITANCE

| Capacitance | Definition |
|-------------|---|
| C_f | Fringe capacitance on the outer side of the trace is contributed by the prepreg ($C_{f,pg}$) and core ($C_{f,co}$) regions. |
| C_p | Parallel plate capacitance of the trace, contributed by the prepreg ($C_{p,pg}$) and core ($C_{p,co}$) regions. |
| C_{fg} | Fringe capacitance near the gap between traces, contributed by the prepreg ($C_{fg,pg}$) and core ($C_{fg,co}$) regions. |
| C_g | Mutual capacitance across the gap, contributed by the prepreg ($C_{g,pg}$), resin pocket ($C_{g,RP}$), and core ($C_{g,co}$) regions. |

Here, m represents even or odd mode. The FEXT is generated during the time interval between the arrival of the odd-mode signal and the arrival of the even-mode signal.

The differences between $v_{p,\text{even}}$ and $v_{p,\text{odd}}$ can be described as the variable Δ_{LC} [7], which is defined as

$$\Delta_{LC} = L_{\text{odd}} C_{\text{odd}} - L_{\text{even}} C_{\text{even}} = 2(L_{11} |C_{21}| - C_{11} L_{21}) \quad (2)$$

To separate the contribution of each IDL on Δ_{LC} , the capacitance is decomposed [17]. In [17], the stripline is modeled with the core and prepreg layers. Based on that, the capacitance of the structure with 3 IDLs is decomposed in [4], as is shown in Fig. 2. The four categories of the PUL capacitances in the three-layer model are explained in Table I.

In reality, the thickness of the resin pocket may vary depending on the resin content of dielectrics used. In this study, since the main focus is to develop an equivalent model, we assume the thickness of the resin pocket is the same as the trace thickness. As the result, C_f , C_p , and C_{fg} are mainly related to the flux that goes

through the core and prepreg layers. The mutual capacitance across the gap C_g can be expressed as

$$\begin{aligned} C_g &= C_{g,pg} + C_{g,co} + C_{g,rp} \\ &= \varepsilon_{r,pg} C_{g,pga} + \varepsilon_{r,co} C_{g,coa} + \varepsilon_{r,rp} C_{g,rpa}. \end{aligned} \quad (3)$$

The total capacitance in the prepreg ($C_{t,pg}$) is expressed using the capacitance components with subscript “*pg*”

$$\begin{aligned} C_{t,pg} &= C_{f,pg} + C_{p,pg} + C_{fg,pg} \\ &= \varepsilon_{r,pg} \cdot (C_{f,pg}^a + C_{p,pg}^a + C_{fg,pg}^a) \\ &= \varepsilon_{r,pg} \cdot C_{t,pg}^a. \end{aligned} \quad (3a)$$

This capacitance is expressed by the product of the capacitances in the air-filled structure (denoted by the superscript “*a*”) and the permittivity of the dielectric material. The total capacitance in the core ($C_{t,co}$) is expressed similarly [18, eq. (8.86)] as

$$\begin{aligned} C_{t,co} &= C_{f,co} + C_{p,co} + C_{fg,co} \\ &= \varepsilon_{r,co} \cdot (C_{f,co}^a + C_{p,co}^a + C_{fg,co}^a) \\ &= \varepsilon_{r,co} \cdot C_{t,co}^a. \end{aligned} \quad (3b)$$

Thus, the self-capacitance in the nodal capacitance matrix can be expressed as

$$\begin{aligned} C_{11} &= C_{t,pg} + C_{t,co} + C_g \\ &= \varepsilon_{r,pg} \cdot C_{t,pga} + \varepsilon_{r,co} \cdot C_{t,coa} \\ &\quad + \varepsilon_{r,pg} C_{g,pga} + \varepsilon_{r,co} C_{g,coa} + \varepsilon_{r,rp} C_{g,rpa}. \end{aligned} \quad (4)$$

The mutual capacitance in the nodal capacitance matrix

$$|C_{21}| = C_g = \varepsilon_{r,pg} C_{g,pg}^a + \varepsilon_{r,co} C_{g,co}^a + \varepsilon_{r,rp} C_{g,rp}^a. \quad (5)$$

According to [17 [eq. (14)], the self-inductance and mutual inductance can be estimated using capacitances of the air-filled line as

$$\begin{aligned} L_{11} \left[\frac{\text{nH}}{\text{cm}} \right] &\approx \frac{10 C_{11}^a}{9 \Delta C^a} \\ &= \frac{10 (C_{t,pg}^a + C_{t,co}^a + C_g^a)}{9 \Delta C^a} \left[\frac{\text{pF/cm}}{(\text{pF/cm})^2} \right] \end{aligned} \quad (6)$$

$$\begin{aligned} L_{21} \left[\frac{\text{nH}}{\text{cm}} \right] &\approx \frac{10 |C_{21}|}{9 \Delta C^a} \\ &= \frac{10 (C_{g,pg}^a + C_{g,co}^a + C_{g,rp}^a)}{9 \Delta C^a} \left[\frac{\text{pF/cm}}{(\text{pF/cm})^2} \right] \end{aligned} \quad (7)$$

$\Delta C^a = (C_{11}^a)^2 - (C_{21}^a)^2$ where. For typical edge-coupled striplines $\Delta C^a > 0$. Then, Δ_{LC} is defined by (2) using the L and C given by (4)–(7) expressed as

$$\begin{aligned} \Delta_{LC} &= \frac{10}{9 \Delta C^a} \cdot \\ &\quad [(\varepsilon_{r,pg} - \varepsilon_{r,rp}) \cdot (C_{t,pg}^a C_{g,co}^a - C_{t,co}^a C_{g,pg}^a + C_{t,pg}^a C_{g,rp}^a) \\ &\quad + (\varepsilon_{r,co} - \varepsilon_{r,rp}) \cdot (C_{t,co}^a C_{g,pg}^a - C_{t,pg}^a C_{g,co}^a + C_{t,co}^a C_{g,rp}^a)] \end{aligned} \quad (8)$$

Where $C_{t,pg}$, $C_{t,co}$, $C_{g,pg}$, $C_{g,co}$, $C_{g,rp}$, and ΔC^a are all the capacitance with the air-filled structure, which is only related to the geometry of the stripline.

From (8), it can be noted that Δ_{LC} is proportional to the dielectric permittivity difference between prepreg and resin pocket ($\varepsilon_{r,pg} - \varepsilon_{r,rp}$) and the difference between the core and resin pocket ($\varepsilon_{r,co} - \varepsilon_{r,rp}$). In other words, the FEXT caused

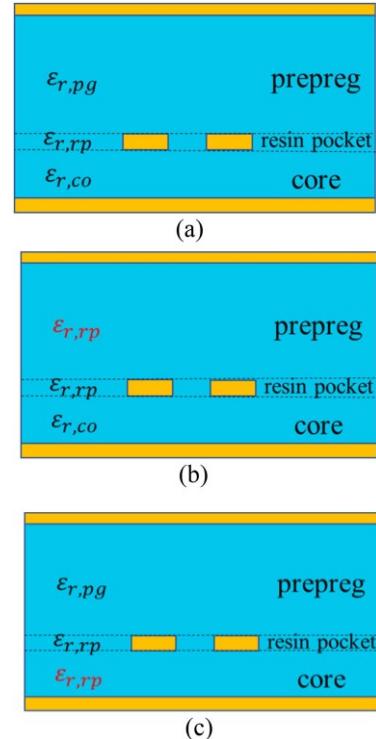


Fig. 3. (a) Case 1: The dielectric permittivity in the prepreg, resin pocket, and core layers are $\varepsilon_{r,pg}$, $\varepsilon_{r,rp}$, and $\varepsilon_{r,co}$, respectively. (b) Case 2: The dielectric permittivity in prepreg and resin pocket layers is $\varepsilon_{r,pg}$. (c) Case 3: The dielectric permittivity in core and resin pocket layers is $\varepsilon_{r,co}$.

by the 3L-IDL can be separated into two parts: FEXT caused by the inhomogeneity of prepreg and resin pocket layers and FEXT caused by the inhomogeneity of core and resin pocket layers. Accordingly, the superposition method is introduced.

B. Superposition Method

The 3L-IDL model with three different dielectric materials is not easy to analyze directly. Therefore, decomposing it into typical 2L-IDL models can help to simplify the complex structure.

As shown in Fig. 3, Case 1 is the original 3L-IDL model. The dielectric permittivity in the prepreg, resin pocket, and core

layers are $\varepsilon_{r,pg}$, $\varepsilon_{r,RP}$, and $\varepsilon_{r,co}$, respectively. Two inhomogeneous boundaries are formed in this model: the boundary between prepreg and resin pocket and the boundary between resin pocket and core, to decompose the two boundaries into two sets of relatively simple 2L-IDL models.

In Case 2, the dielectric permittivity of the prepreg layer is denoted by $\varepsilon_{r,RP}$, which is the same as the dielectric permittivity of the resin pocket. The model in Case 2 then becomes a two-layer model with only one inhomogeneous boundary between the resin pocket and core. According to (8), Δ_{LC} of Case 2 is

$$\Delta_{LC2} = \frac{10C_g^a}{9\Delta C^a} \cdot [(\varepsilon_{r,pg} - \varepsilon_{r,RP}) \cdot (C_{t,pg}^a C_{g,co}^a - C_{t,co}^a C_{g,pg}^a + C_{t,pg}^a C_{g,RP}^a)] . \quad (9)$$

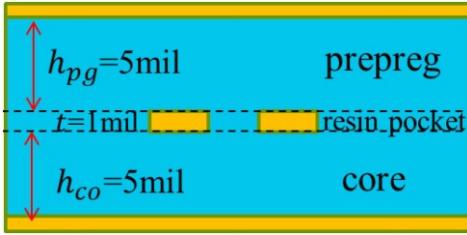


Fig. 4. Cross-sectional geometry of two coupled symmetrical stripline traces. The trace width of the trace is 7.2 mil. The spacing between the traces is 10 mil.

In Case 3, the dielectric permittivity of the core layer is denoted by $\varepsilon_{r,RP}$, which is the same as the dielectric permittivity of the resin pocket. The model in Case 3 then becomes a two-layer model with only one inhomogeneous boundary between the resin pocket and prepreg

$$\Delta_{LC3} = \frac{10C_g^a}{9\Delta C^a} \cdot [(\varepsilon_{r,co} - \varepsilon_{r,RP}) \cdot (C_{t,co}^a C_{g,pg}^a - C_{t,pg}^a C_{g,co}^a + C_{t,co}^a C_{g,RP}^a)] . \quad (10)$$

It can be assumed that the air-filled mutual capacitances across the gap contributed by each layer ($C_{g,pg}^a$, $C_{g,co}^a$, $C_{g,RP}^a$) remain the same when assigning different dielectric permittivity to the layers.

Δ_{LC1} can be expressed by the superposition of Case 2 and Case 3

$$\Delta_{LC1} = \Delta_{LC2} + \Delta_{LC3}. \quad (11)$$

Then, the FEXT caused by the inhomogeneity of the stripline with the 3L-IDL model is equivalent to the superposition of the FEXT of two two-layer models.

C. FEXT Analysis for Stripline With IDLs

As the validation of the FEXT analysis methodology, two examples are given for the stripline with IDL and with different geometries. One of the single-ended traces is considered the aggressor and the other trace is the victim. The FEXT caused

by the coupling between the two traces is discussed. The work can be easily extended to differential signaling as well.

1) *Stripline With Symmetric Prepreg and Core Dimension*: Fig. 4 demonstrates a cross section of an equivalent model of the stripline. For simplicity, the cross section of the stripline is set as rectangular instead of a typical trapezoidal shape. Both the thickness of the prepreg layer and the core layer is 5 mil. Both the dielectric permittivity in core and prepreg is 4. The dielectric permittivity in the resin pocket is set to be 2.8 as an example. The thickness of the trace is also set to be the same as the thickness of the resin pocket layer. In this example, the stripline is symmetric in that the core layer and the prepreg layer share the same thickness and material property. The FEXT level of the example can be decomposed into two cases as Fig. 3.

All three cases are simulated by ANSYS Q2D. The assignment of dielectric permittivity for the different cases is

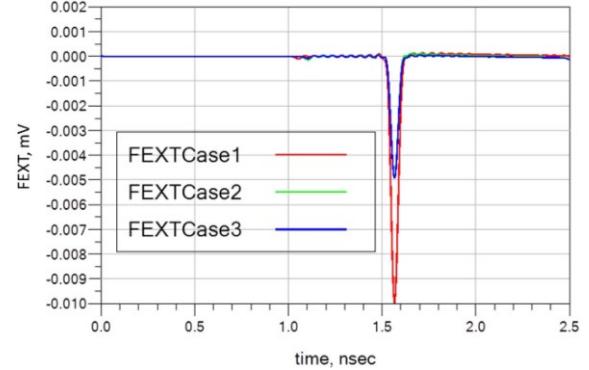


Fig. 5. FEXT waveform for the stripline model with the geometry in Fig. 4.

TABLE II
PEAK VALUE OF THE FEXT WAVEFORM WITH THE GEOMETRY IN FIG. 4

| | Case 1 | Case 2 | Case 3 |
|-----------------------|--------|--------|--------|
| ε_{preg} | 4 | 2.8 | 4 |
| ε_{resin} | 2.8 | 2.8 | 2.8 |
| ε_{core} | 4 | 4 | 2.8 |
| FEXT Peak (mV) | -9.97 | -4.96 | -4.96 |

Case 1: $\varepsilon_{r,pg} = 4$; $\varepsilon_{r,RP} = 2.8$, $\varepsilon_{r,co} = 4$.

Case 2: $\varepsilon_{r,pg} = 2.8$; $\varepsilon_{r,RP} = 2.8$, $\varepsilon_{r,co} = 4$. Case 3: $\varepsilon_{r,pg} = 4$; $\varepsilon_{r,RP} = 2.8$, $\varepsilon_{r,co} = 2.8$.

The transformed FEXT waveform result from the S-parameter of the Q2D simulation is shown in Fig. 5. Table II lists the peak value of the FEXT waveform of the three cases. The FEXT level of Case 1 is approximately equal to the sum of Case 2 and Case 3. The error is caused by the assumption during the derivation that the air-filled mutual capacitances across the gap contributed by each layer ($C_{g,pg}^a$, $C_{g,co}^a$, $C_{g,RP}^a$) are the same in different cases. The flux lines tend to get more concentrated in the region with higher dielectric permittivity. As a result, for different cases, the portion of the mutual capacitance contributed by different layers will be slightly different.

In this example, the core layer and the prepreg layer have the same thickness and dielectric. If the stripline is only modeled with core and prepreg layers, the mutual capacitance across the gap C_g can be expressed as

$$C_g = C_{g,pg} + C_{g,co} = \varepsilon_{r,pg} C_{g,pg}^a + \varepsilon_{r,co} C_{g,co}^a. \quad (12)$$

Then, replace (3) by (12) for (4)–(7), Δ_{LC} for the two-layer model is

$$\Delta_{LC} = \frac{10}{9\Delta C^a} \cdot (\varepsilon_{r,pg} - \varepsilon_{r,co}) \cdot (C_{t,pg}^a C_{g,co}^a - C_{t,co}^a C_{g,pg}^a) \quad (13)$$

where $\varepsilon_{r,pg}$ and $\varepsilon_{r,co}$ are effective dielectric permittivity for the prepreg and core layers in the two-layer model. $C_{g,pg}^a$ and $C_{g,co}^a$ are effective air-filled mutual capacitances across the gap contributed by prepreg and core layers. The FEXT level of this 2L-IDL model turns out to be close to zero, indicating that for this extreme symmetric example, the former 2L-IDL model

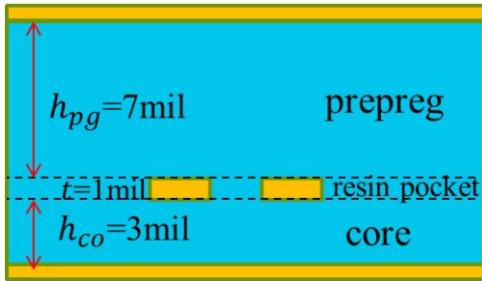


Fig. 6. Cross-sectional geometry of two coupled stripline traces. The trace width of the trace is 7.2 mil. The spacing between the traces is 10 mil.

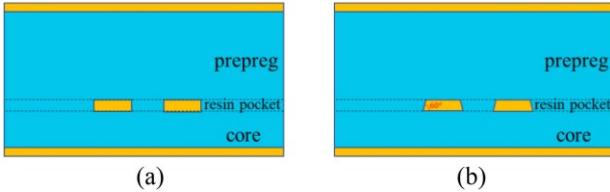


Fig. 7. Cross-section of (a) rectangle traces and (b) trapezoid traces with the 60° base angle.

cannot describe the performance of the multiple IDLs structures accurately.

2) *Stripline With Asymmetric Prepreg and Core Dimension*: Another example is the stripline with asymmetrical prepreg and core dimensions. The trace is not in the middle between the reference plane and the dielectric constant is different for different layers. The structure is more frequently used in fabricated PCB design.

The cross-sectional geometry is shown in Fig. 6. In this case, the thickness of the prepreg layer is 7 mil, whereas the thickness of the core layer is 3 mil. The dielectric permittivity in the core is 3.5. The dielectric permittivity in the resin pocket is 2.8. In fabricated multilayer PCB, due to the different glass fiber weave/content in prepreg and core, prepreg melting during lamination, and resin properties tolerances, etc. [4], [5], [6]. The dielectric permittivities in the prepreg and core layer are different in

this example, where the dielectric permittivity prepreg is defined as 3.5, 4.5, and 5.5 for different series of cases.

Table III lists the FEXT magnitude of the different cases. For the series of Case a, Case b, and Case c, the FEXT level of Case x.1 is approximately equal to the sum of Case x.2 and Case x.3 (x refers to a, b, or c), which validates the superposition method for asymmetric stack up as well.

For this asymmetrical example, the FEXT performance cannot be simply predicted from the 3L-IDL model. With the help of the superposition method, the problem is decomposed into two 2L-IDL cases and the total FEXT level can be predicted. In (9) and (10), it can be noted that Δ_{LC} is not only related to the difference of the dielectric material but also the capacitance. Then, (9) and (10) can be modified as

$$\Delta_{LC2} = \frac{10C_g^a}{9\Delta C^a} \cdot \{ (\varepsilon_{r,pg} - \varepsilon_{r,RP}) \cdot ([C_{t,pg}^a + C_{g,RP}^a] - C_{t,co}^a C_{g,pg}^a) \} \quad (14)$$

TABLE III
PEAK VALUE OF THE FEXT WAVEFORM WITH THE GEOMETRY IN FIG. 6

| | Case a.1 | Case a.2 | Case a.3 |
|-----------------------|----------|----------|----------|
| ε_{prepg} | 3.5 | 2.8 | 3.5 |
| ε_{resin} | 2.8 | 2.8 | 2.8 |
| ε_{core} | 3.5 | 3.5 | 2.8 |
| FEXT Peak (mV) | -3.65 | -6.50 | 2.95 |

| | Case b.1 | Case b.2 | Case b.3 |
|-----------------------|----------|----------|----------|
| ε_{prepg} | 4.5 | 2.8 | 4.5 |
| ε_{resin} | 2.8 | 2.8 | 2.8 |
| ε_{core} | 3.5 | 3.5 | 2.8 |
| FEXT Peak (mV) | -0.30 | -6.50 | 6.69 |

| | Case a.1 | Case a.2 | Case a.3 |
|-----------------------|----------|----------|----------|
| ε_{prepg} | 5.5 | 2.8 | 5.5 |
| ε_{resin} | 2.8 | 2.8 | 2.8 |
| ε_{core} | 3.5 | 3.5 | 2.8 |
| FEXT Peak (mV) | -3.91 | -6.50 | 10.63 |

TABLE IV
PEAK VALUE OF THE FEXT WAVEFORM

| | Symmetric Case | Asymmetric Case |
|-----------------------|----------------|-----------------|
| ε_{prepg} | 4 | 3.5 |
| ε_{resin} | 2.8 | 2.8 |
| ε_{core} | 4 | 3.5 |

| | | |
|------------------------------------|--------|-------|
| FEXT Peak of rectangle traces (mV) | -9.97 | -3.65 |
| FEXT Peak of trapezoid traces (mV) | -10.01 | -3.87 |

$$\Delta_{LC3} = \frac{10C_g^a}{9\Delta C^a} \cdot \{ (\varepsilon_{r,co} - \varepsilon_{r,RP}) \cdot [C_{t,co}^a - (C_{g,pg}^a + C_{g,RP}^a) - C_{t,pg}^a C_{g,co}^a] \}. \quad (15)$$

In this example, the thickness of the prepreg layer is larger than that of the core layer. As the result, $C_{t,pg}^a$ will be smaller than $C_{t,co}^a$. Considering that $C_{g,pg}^a + C_{g,RP}^a$ should be larger than $C_{g,co}^a$, Δ_{LC3} is expected to be a positive value. The value of the capacitance term in Δ_{LC2} is expected to be much smaller than that in Δ_{LC3} .

In all the cases, the traces are assumed to be rectangular, as is shown in Fig. 7 (a). While in reality, due to the time-controlled etching process in the PCB fabrication, the copper area is actually dissolved from the top down, which results in the trapezoid trace shape [19], as is shown in Fig. 7 (b). Comparisons between the rectangle trace and trapezoid trace are shown in Table IV. The base angle of the trapezoid shape is 60° . The average of the upper and lower edge of the trapezoid is the same as the width of the rectangle. The geometry of the symmetric case is the same as Fig. 4, whereas the geometry of the asymmetric case is the

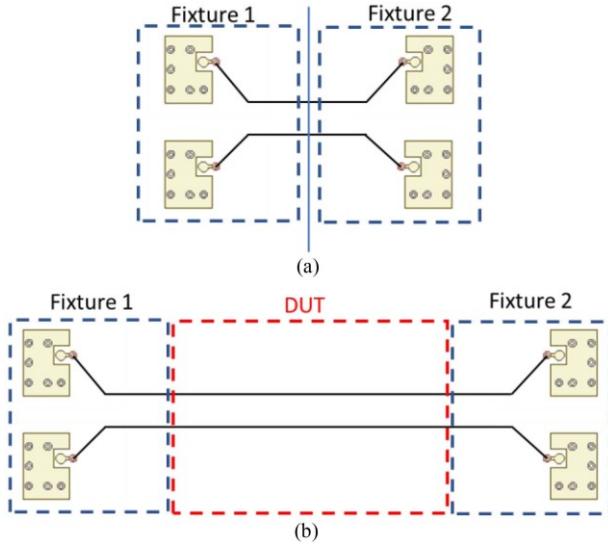


Fig. 8. Conceptual illustration of a Delta-L structure. (a) Thru. (b) Total.

same as Fig. 6. The error caused by the approximation on the trace shape is within 6%.

III. DIELECTRIC PERMITTIVITY EXTRACTION ALGORITHM

In this section, ε_r of IDLs extraction methodology using measured S-parameters of Delta-L and EUL structures within the same layer of a PCB is introduced. A two-parameter

optimization problem is formulated based on the investigations of the sensitivity of FEXT peak voltage and phase.

A. Measurement Setup

To investigate the FEXT and insertion loss of the PCB, boards with multiple striplines with EUL structure and Delta-L lines are fabricated. We use the Delta-L and EUL structures since both of them are readily available in a typical PCB electrical characterization board. Delta-L is used to characterize the insertion loss of differential interconnect (such as PCIe, etc.), and EUL is used to characterize the crosstalk of single-ended interconnect (such as DDR, etc.).

The Delta-L structures are differential striplines with different lengths, as shown in Fig. 8. The “Thru” is with a shorter length, and the “Total” is with a longer length. The test fixtures consist of connectors, pads, vias, transitions, etc. Using IPC test method 2.5.5.14, the insertion loss of “DUT” is obtained. The measurement is performed with D-probes [20]. Compared to the traditional measurement methods based on SMA connectors, more efficient tests can be performed with smaller landing space for the high-volume PCB manufacturing validation.

The striplines with EUL structures are illustrated in Fig. 9. The device under test (DUT) is a pair of coupled single-ended striplines, and the striplines are intentionally extended. The extended parts are unterminated (open) without any coupling to the other pair. With a matched long transmission line termination, the impact from FEXT due to mismatched termination can be gated in the time domain [9]. Additionally, only half the test ports

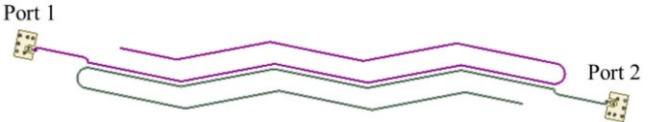


Fig. 9. Conceptual illustration of striplines with EUL structures.

are needed, therefore it eliminates the requirement for costly test equipment with additional ports.

The S-parameters measurement is performed using Keysight N5244A 4-port Network Analyzer. Two 3-in striplines with EUL structures are measured. The amplitude of the incident step signal on the aggressor line is set to $+1$ V. The rise time is 50 ps and the widow width is 1.5 ns. In this study, the Intel IMLC tool [21] is used for fast calculation and batch mode. The Delta-L and EUL structures within the same layer of a PCB are assumed to share the same ε_r of each IDL.

B. Extraction Methodology

In [22], a set of simulations are performed to investigate the FEXT's sensitivity to $\varepsilon_{r,pg}$ and $\varepsilon_{r,co}$ of the 2L-IDL modeled. The difference of $\varepsilon_{r,pg}$ and $\varepsilon_{r,co}$ has an obvious impact on the absolute value of $v_{p,odd}$ and $v_{p,even}$, leading to shorter or longer modal time of flight, which in turn affects the FEXT level. On the other

hand, the differential mode PUL phase (β_{dd}) is quite sensitive to the sum of $\varepsilon_{r,pg}$ and $\varepsilon_{r,co}$.

As of the 3L-IDL model, the resin pocket layer is only filled with resin. The dielectric constant of the resin is provided by the PCB vendor as 2.8 in this test coupon. With the superposition method, the FEXT peak value can still be expressed as a function of $\varepsilon_{r,pg}$ and $\varepsilon_{r,co}$

$$v_{\text{fext}}' = K_{\text{FEXT}}(\varepsilon_{r,pg}, \varepsilon_{r,co}). \quad (16)$$

According to Liu et al. [14], the differential propagation constant of a transmission line is related to the PUL RLGC parameters for differential mode

$$\gamma_{dd} = \sqrt{(R_{dd} + j\omega L_{dd})(G_{dd} + j\omega C_{dd})}. \quad (17)$$

Since all practical lines are low loss, that is $R \ll \omega L$ and $G \ll \omega C$, (3) can be approximated using the Taylor series expansion, and the phase (β_{dd}) can be estimated [23, eq. (2-85b)] as

$$\beta_{dd} = \text{imag}(\gamma_{dd}) \approx \omega \cdot \sqrt{L_{dd} \cdot C_{dd}}. \quad (18)$$

Since C_{dd} is contributed by the capacitance components distributed in prepreg ($C_{dd,pg}$), resin pocket ($C_{dd,rp}$), and core ($C_{dd,co}$) for differential mode. For a stripline, the capacitances in prepreg and core are in parallel [17]

$$C_{dd} = C_{dd,pg} + C_{dd,rp} + C_{dd,co}. \quad (19)$$

Thus, β_{dd} should have a strong sensitivity to the sum of $\varepsilon_{r,pg}$ and $\varepsilon_{r,co}$, since $C_{dd,pg}$ and $C_{dd,co}$ in (5) are scaled by $\varepsilon_{r,pg}$ and $\varepsilon_{r,co}$.

Then, the modeled β_{dd} is expressed as β_{dd}' and v_{fext}

$$\beta_{dd}' = K_{\beta}(\varepsilon_{r,pg}, \varepsilon_{r,co}). \quad (20)$$

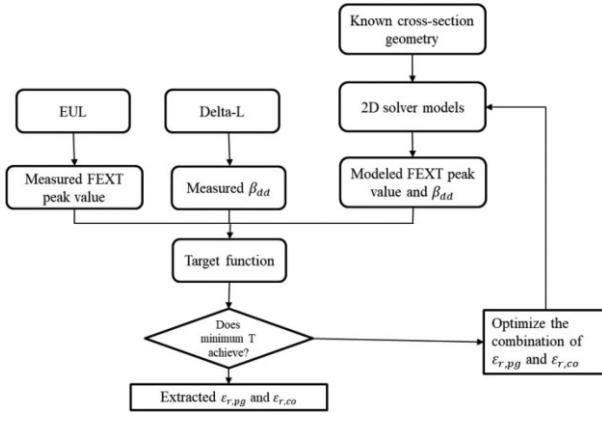


Fig. 10. Flowchart of the proposed $\varepsilon_{r,pg}$ and $\varepsilon_{r,co}$ extraction method.

TABLE V

EXTRACTION RESULT COMPARISON OF 2L-IDL MODEL AND 3L-IDL MODEL

| | Spacing [mil] | 2-IDL $\varepsilon_{r,pg}$ | 2-IDL $\varepsilon_{r,co}$ | 3-IDL $\varepsilon_{r,pg}$ | 3-IDL $\varepsilon_{r,co}$ |
|--------|---------------|----------------------------|----------------------------|----------------------------|----------------------------|
| Case 1 | 6.3 | 3.65 | 4.28 | 4.68 | 4.04 |
| Case 2 | 7.3 | 3.77 | 4.22 | 4.65 | 4.04 |

To extract the inhomogeneous dielectric permittivity ($\varepsilon_{r,pg}$, $\varepsilon_{r,co}$), a target function (T) is generated to evaluate the estimate of the error between the modeled result to the measured result. The function is defined with root-mean-squared error, which is a general-purpose error metric for numerical predictions as

$$T = \sqrt{(v_{\text{fext}}' - v_{\text{fext}0})^2 + \left[\left(\frac{\beta_{dd}'}{\omega} - \frac{\beta_{dd0}}{\omega} \right) \cdot 10^8 \right]^2}. \quad (21)$$

Here, the unit $v_{\text{fext}}' - v_{\text{fext}0}$ is millivolt, which is usually $\beta_{dd}'/\omega - \beta_{dd0}/\omega$ in the order of 10^{-1} , whereas $\beta_{dd}'/\omega - \beta_{dd0}/\omega$ is in the order of 10^{-9} . As the result, $(\beta_{dd}'/\omega - \beta_{dd0}/\omega) \cdot 10^8$ is introduced for normalization so that $v_{\text{fext}}' - v_{\text{fext}0}$ can have a comparable impact on the target function (T).

The entire extraction procedure is illustrated in the flowchart in Fig. 10. The EUL S-parameters provide the measured FEXT level and the Delta-L S-parameters after de-embedding provides β_{dd} . With the cross-sectional geometry, the simulation model is created by a 2-D solver (Intel IMLC is the 2-D tool we used for this study).

Table V shows the comparison of the extraction result with a different model. Case 1 and Case 2 are the striplines on the same layer of the same board but designed with different spacing. The extraction results of $\varepsilon_{r,pg}$ and $\varepsilon_{r,co}$ are expected to be quite close. Compared with the 3L-IDL model result, the difference of the 2L-IDL extraction results between Case 1 and Case 2 is larger. The 3L-IDL model with resin pocket model is more accurate to model the stripline behavior.

Another validation is shown in Fig. 11, which indicates the FEXT of the wide spacing model with narrow spacing extracted ε_r , compared with the result from the measured S-parameters. As the spacing increases, the trace will see more glass and less

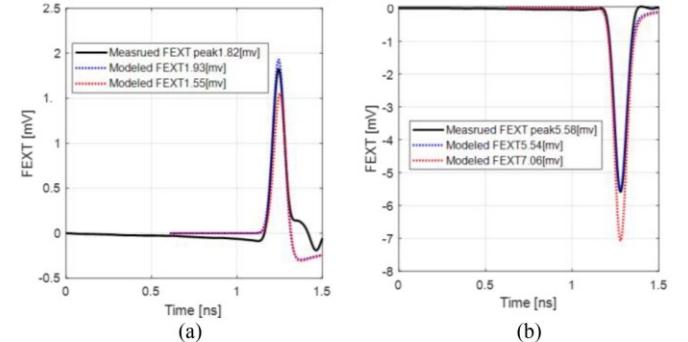


Fig. 11. FEXT of the wide spacing model with narrow spacing extracted DK. (a) Example 1. (b) Example 2. Black solid lines: FEXT result from the measured S-parameters; Blue dash lines: FEXT result from the simulated S-parameters of 3-IDL model; Red dash lines: FEXT result from the simulated S-parameters of 3L-IDL model.

resin ineffective the prepreg layer of the 2L-IDL model, which results in a larger difference between the modeled result and the measured result. Meanwhile, the 3L-IDL model can improve the accuracy of the FEXT prediction.

C. Extraction Algorithm Optimization

The initial extraction procedure used the nominal value from the PCB vendor as the starting value, which is usually the effective value of the typical stripline model with two IDLs. As a result, the procedure requires a large amount of simulations when applying gradient descent optimization. The superposition method can help to simplify the optimization procedure and reduce extraction time. The FEXT level of the decomposed Case 2 and Case 3 is simplified from (9) and (10) as

$$FEXT_{case2} = \lambda_2(\epsilon_{r,pg} - \epsilon_{r,rp}) \quad (22)$$

$$FEXT_{case3} = \lambda_3(\epsilon_{r,co} - \epsilon_{r,rp}). \quad (23)$$

Here, λ_2 and λ_3 are constant when the geometry is fixed. λ_2 and λ_3 can be achieved from the 2-D solver with known geometry. The superposition method can approximate the FEXT of the stripline with IDLs. Accordingly, the FEXT level of the 3L-IDL stripline is

$$\begin{aligned} FEXT_{case1} &= FEXT_{case2} + FEXT_{case3} \\ &= \lambda_2(\epsilon_{r,pg} - \epsilon_{r,rp}) + \lambda_3(\epsilon_{r,co} - \epsilon_{r,rp}). \end{aligned} \quad (24)$$

The FEXT level can be expressed with $\epsilon_{r,pg}$ and $\epsilon_{r,co}$ with known $\epsilon_{r,rp}$ and two simulation cases. Since the definition of the core layers of the 2L-IDL model and 3L-IDL model remain the same, the nominate value of the core layer can be used as the initial value of $\epsilon_{r,co}$. The initial value of $\epsilon_{r,pg}$ can be solved from (24). Besides, the polarity of λ_2 and λ_3 helps determine how to adjust the optimization of the combination of $\epsilon_{r,pg}$ and $\epsilon_{r,co}$.

As an example, a pair of Delta-L and EUL structures is under test. The cross-sectional geometry is shown in Table VI.

The FEXT peak value of Case 2 is 26.38 mV; the FEXT peak value of Case 3 is -35.9 mV. From (22) and (23), λ_2 is solved to be 15.51 and λ_3 is solved to be -29.92. With $\epsilon_{r,rp}$ assigned

TABLE VI
CROSS-SECTIONAL GEOMETRY OF THE DELTA-L AND EUL STRUCTURE

| Parameter | [mil] |
|-----------------------|-------|
| Prepreg thickness | 8.9 |
| Core thickness | 4.0 |
| Trace thickness | 1.2 |
| Delta-L trace spacing | 12.5 |
| Delta-L trace width | 5.4 |
| EUL trace spacing | 6.3 |
| EUL trace width | 7.1 |

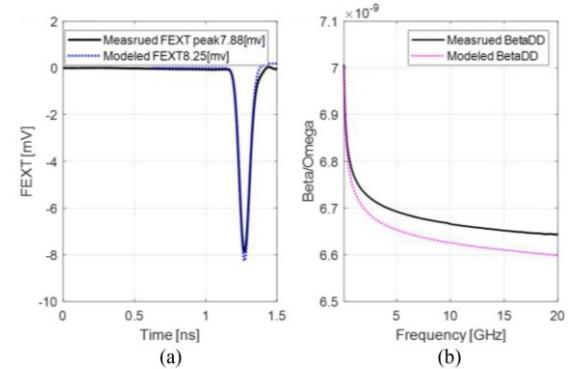


Fig. 12. Comparison between measured result and modeled result with the initial value. (a) FEXT waveform. (b) β_{dd} waveform.

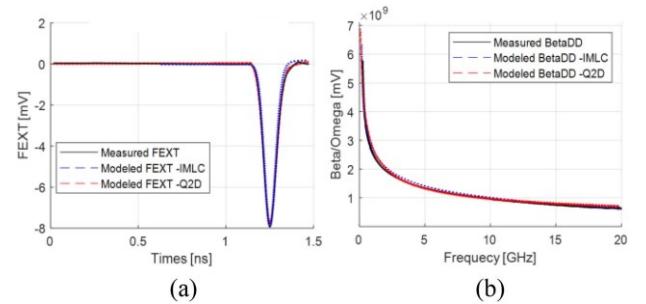


Fig. 13. Comparison between measured result and modeled result with optimized value. (a) FEXT waveform. (b) β_{dd} waveform.

to be 2.8 in (24), the FEXT level of the 3L-IDL model is

$$FEXT_{case1} = 15.51\epsilon_{r,pg} - 29.92 \cdot \epsilon_{r,co} + 40.35. \quad (25)$$

From the EUL measurement, the peak value of the measured FEXT is -7.88 mV. The nominate $\epsilon_{r,co}$ provided by the vendor is 4.0. Then, the initial $\epsilon_{r,pg}$ is solved to be 4.61.

The simulation result of the initial value is shown in Fig. 12. Modeled β_{dd} is lower than the measured result. Since β_{dd} is related to the sum of $\epsilon_{r,pg}$ and $\epsilon_{r,co}$, $\epsilon_{r,pg}$ or $\epsilon_{r,co}$ should be increased to match the measurement result. The peak value of modeled FEXT is lower than the measured result. According to (25), to increase the FEXT value, $\epsilon_{r,pg}$ should be increased or $\epsilon_{r,co}$ should be decreased. Therefore, considering both the FEXT and β_{dd} result, $\epsilon_{r,pg}$ needs to be increased. Fig. 13 shows the comparison between the modeled result and the measured result after the optimization when $\epsilon_{r,pg}$ is defined as 4.7. The modeled result matched the measured result much better. In addition to IMLC simulation results, we also performed simulation with Q2D tool commercially available. Q2D simulation result with the same material properties also validates the extraction result, as shown in Fig. 13.

IV. FEXT PREDICTION FOR STRIPLINE WITH IDLS

In practice, to improve the signal integrity performance in high-speedsystems, the FEXT needstobemitigated. The design of the stripline can be improved with the help of modeling various combinations of materials and geometry.

A method to predict the FEXT polarity and peak level of the stripline caused by the inhomogeneity with an analytical expression is proposed. The prediction only needs the calculation by analytical expressions instead of with assistance from the 2-D or 3-D solvers. Compared to time-consuming full-wave simulation, the proposed method is time-efficient when optimizing a large number of designs with different geometry.

AnalyticalexpressionoftheFEXTpeaklevelisderivedbased on the capacitance decomposing. For the model with multiple IDLs, including resin pocket, the FEXT can be expressed with the superposition of two cases with only two IDLs. The FEXT can be simplified as

$$\sim \Delta LC \approx K \frac{C_{21}^a}{(C_{11}^a)^2 - (C_{21}^a)^2} \cdot (\varepsilon_{r,pg} - \varepsilon_{r,co}) \cdot \left(\frac{1}{h_{pg}} - \frac{1}{h_{co}} \right) . \quad (26)$$

FEXT

For the typical stripline model with two IDLs with the symmetric structure in which the thickness of the core layer and the prepreg layer is the same as h , [18 eq. (8.60–8.62)] proposed expression for the capacitance of air-filled case

$$C_m^a = \frac{1}{cZ_m} \quad (27)$$

$$Z_m = \frac{30\pi}{\sqrt{\varepsilon_r}} \frac{K(k'_m)}{K(k_m)} \quad (28)$$

$$\frac{K(k'_m)}{K(k_m)} = \begin{cases} \frac{\ln\left(2\frac{1+\sqrt{k'_m}}{1-\sqrt{k'_m}}\right)}{\pi} & \text{if } 0 \leq k < \frac{1}{\sqrt{2}} \\ \frac{\pi}{\ln\left(2\frac{1+\sqrt{k'_m}}{1-\sqrt{k'_m}}\right)} & \text{if } \frac{1}{\sqrt{2}} \leq k < 1 \end{cases} \quad (29)$$

$$\begin{cases} k_o = \tanh\left(\frac{\pi w}{4h}\right) \coth\left[\frac{\pi}{4}\left(\frac{w+s}{h}\right)\right], k'_o = \sqrt{1-k_o^2} \\ k_e = \tanh\left(\frac{\pi w}{4h}\right) \tanh\left[\frac{\pi}{4}\left(\frac{w+s}{h}\right)\right], k'_e = \sqrt{1-k_e^2} \end{cases} . \quad (30)$$

Here, m represents even or odd mode. w is the trace width. s is the spacing between the traces.

The mutual capacitance and self-capacitance in (26) are expressed with the modal capacitance as

$$\begin{cases} C_{11h}^a = C_e^a \\ C_{12h}^a = 0.5(C_o^a - C_e^a) \end{cases} . \quad (31)$$

For the asymmetric structure in which the thickness of the core layer is h_{co} and the prepreg layer is h_{pg} , the capacitance is approximately expressed as

$$\begin{cases} C_{11}^a = 0.5(C_{11h_{co}}^a + C_{11h_{pg}}^a) \\ C_{12}^a = 0.5(C_{12h_{co}}^a + C_{12h_{pg}}^a) \end{cases} . \quad (32)$$

Here, $C_{11h_{co}}^a$, $C_{11h_{pg}}^a$, $C_{12h_{co}}^a$, and $C_{12h_{pg}}^a$ are the capacitance of the symmetric air-filled structure when $h = h_{pg}$ or $h = h_{co}$.

Then, the FEXT level of the stripline can be expressed as

$$\text{FEXT2-IDL} = K f'(\varepsilon_{co}, \varepsilon_{pg}, h_{co}, h_{pg}, s, w, t). \quad (33)$$

f is solved from (26) to (32). K is decided from the simulation result based on the geometry in coupon design.

For the 3L-IDL stripline, the FEXT level is predicted with the superposition method as

$$\text{FEXT3-IDL} = \text{FEXT2-IDL case2} + \text{FEXT2-IDL case3}. \quad (34)$$

As demonstrated in Fig. 3, Case 2 is the same structure as the typical stripline, which considers the resin pocket layer and the prepreg layer filled with the homogenous material. While in Case 3, the core layer and the resin pocket layer are filled with the same material, which means the thickness of the core layer should be increased by t and the thickness of the equivalent prepreg layer used for the 2L-IDL model should be decreased by t . Therefore, the FEXT expression for the decomposed cases is

$$\text{FEXT}_{\text{case2}} = K f'(\varepsilon_{co}, \varepsilon_{rp}, h_{co}, h_{pg}, s, w, t) \quad (35)$$

$$_3 = K f'(\varepsilon_{rp}, \varepsilon_{co}, (h_{co} + t), (h_{pg} - t), s, w, t). \quad (36)$$

With (33) and (34), the polarity and the FEXT level of the stripline with two IDLs and three IDLs can be predicted. Based on over 351 measured cases with a different set of boards from three different vendors, the correct rate for the polarity prediction of the 2L-IDL model is 99.43% and that of the 3L-IDL model is 98.58%.

For the FEXT peak level prediction, the passing criteria are defined as the following: When the absolute FEXT peak value of the measurement is larger than 2 mV if the difference prediction

and the measurement are less than 30%, the case is passed.; when the absolute FEXT peak value is less than 2 mV if the predicted FEXT level is less than 2 mV and polarity of the is correctly predicted, the case is passed. The passing ratio of the 2-IDL model is 90.03% and that of the three-layer model: 80.63%.

The prediction error is introduced from the following process: the analytical expressions for the capacitance and inductance; the assumption for the superposition method; and the inaccuracy of the geometry information.

With the prediction expression for the stripline, the following design guidelines are summarized to mitigate the FEXT.

- 1) The thickness of the core and prepreg layer needs to be identical, if not as similar as possible.

Table VII shows three cases of measurement with different core and prepreg thicknesses while with the same trace spacing and manufactured with the same material by the same vendor. According to (26), when the thicknesses of the core and prepreg

are designed to be closer, the FEXT level will be smaller. The measured result matches the expectation.

TABLE VII
FEXT COMPARISON WITH DIFFERENT THICKNESSES OF CORE AND PREPREG

| | h_{co} [mil] | h_{pg} [mil] | FEXT [mV] |
|--------------|----------------|----------------|-----------|
| Structure #1 | 3 | 7 | 1.68 |
| Structure #2 | 4 | 7 | 0.98 |
| Structure #3 | 5 | 6 | -0.15 |

TABLE VIII
MEASURED FEXT COMPARISON WITH DIFFERENT SPACING OF TEST COUPON

| | Spacing [mil] | FEXT [mV] |
|--------|---------------|-----------|
| Set #1 | 4.5 | -7.68 |
| | 6.0 | -4.84 |
| | 9.0 | -2.90 |
| Set #2 | 7.2 | -0.96 |
| | 9.3 | -0.47 |
| | 18.0 | -0.15 |
| | 20.3 | -0.03 |
| | 21.0 | -0.02 |

TABLE IX
FEXT COMPARISON WITH DK OF CORE AND PREPREG

| | ϵ_{preg} | ϵ_{core} | FEXT [mV] |
|----------|-------------------|-------------------|-----------|
| Board #1 | 4.08 | 3.46 | -3.74 |
| Board #2 | 3.96 | 3.87 | -0.55 |

2) The spacing between the traces should be maximized.

Table VIII shows two cases of measurement in the same layer of the same board with different spacing. The FEXT level of the larger spacing case is smaller.

3) Using the 2L-IDL model, a combination of core and prepreg should be chosen with the least difference between the two dielectric constants.

Table IX shows three cases of measurement with different boards, while with the same geometry. According to (26), when the DKs of core and prepreg are designed to be closer, the FEXT level will be smaller. The measured result matches the expectation.

4) Using the 3L-IDL model, core and prepreg combinations should be chosen to match the DK value to minimize FEXT, using the proposed analytical model, as much as possible.

To get the optimized design for the dielectric material, the expression for the FEXT of a certain stripline can be generated and the permittivity can be solved. The process is as follows.

- With known geometry information and the initial value of the permittivity, solve the FEXT level for Case 2 and Case 3 by a 2-D solver or (27)–(34).
- Generate the FEXT expression of 3L-IDL with the superposition method.

TABLE X
SUMMARY OF THE COMPARISON BETWEEN 2L-IDL AND 3L-IDL MODEL

| | Pros | Cons |
|--------------|--|---|
| 2L-IDL Model | Easy to control the permittivity in the manufacturing procedure for material selection | Inaccurate to modeling and predicting the FEXT, especially when the trace spacing is varied. |
| 3L-IDL Model | 1. Accurate characterization for the dielectric property 2. Accurate modeling and prediction of the FEXT 3. Effective FEXT mitigation for the inhomogeneous design can be generated. | More complicated modeling and extraction of material property process. Requires the superposition method for the FEXT analysis |

- Solve the equation when the FEXT is equal to zero and find the best solution for the permittivity.

For example, the structure in Fig. 6 is designed with $\epsilon_{r,RP} = 2.8$ and $\epsilon_{r,CO} = 3.5$. $\epsilon_{r,PG}$ need to be determined and can be designed for minimum FEXT. The initial value for $\epsilon_{r,PG}$ is 3.5. The FEXT for Case 2 is solved as -6.5 mV and the FEXT for Case 2 is solved as 2.95 mV. Then, the FEXT can be predicted as

$$FEXT_{predict} = 4.2(\epsilon_{r,PG} - \epsilon_{r,RP}) - 9.3(\epsilon_{r,CO} - \epsilon_{r,RP}). \quad (37)$$

Then, $\epsilon_{r,PG}$ is solved as 4.35 when $FEXT_{predict}$ is 0. The simulated FEXT is -0.3 mV. The simulated best solution of $\epsilon_{r,PG}$ is 4.5. The error between the solution of the prediction and the simulation value is 3%. Only with the superposition method and analytical prediction, the best minimize FEXT can be achieved.

V. CONCLUSION

In this article, the stripline model of 3L-IDL is proposed with improved FEXT prediction accuracy compared to the 2L-IDL model by separating the resin pocket from the traditional stripline model and using the superposition principle. A summary table is shown in Table X.

To better model the FEXT, ϵ_r of IDLs is extracted using measured S-parameters of Delta-L and EUL structures. The extraction algorithm is optimized with the superposition principle. Moreover, the prediction for the FEXT polarity and magnitude of the stripline caused by the inhomogeneity can be predicted using the proposed analytical model and is verified with the measurement data. With the stack up information, the

polarity can be predicted with over 98% accuracy and the FEXT level can be predicted with over 80% accuracy. This article also provides a design guide to minimize FEXT induced by IDLs for PCB material designers.

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REFERENCES

- [1] B. Pu, J. He, A. Harmon, Y. Guo, Y. Liu, and Q. Cai, "Signal integrity design methodology for package in co-packaged optics based on figure of merit as channel operating," in *Proc. IEEE Int. Joint EMC/SI/PI EMC Eur. Symp.*, 2021, pp. 492–497.
- [2] B. Chen, S. Pan, J. Wang, S. Yong, M. Ouyang, and J. Fan, "Differential crosstalk mitigation in the pin field area of serdes channel with trace routing guidance," *IEEE Trans. Electromagn. Compat.*, vol. 61, no. 4, pp. 1385–1394, Aug. 2019.
- [3] B. Chen et al., "Differential integrated crosstalk noise (ICN) mitigation in the pin field area of SerDes channel," in *Proc. IEEE Int. Symp. Electromagn. Compat., Signal Integr., Power Integr.*, 2018, pp. 533–537.
- [4] Y. Guo et al., "The simulated TDR impedance in PCB material characterization," in *Proc. IEEE Int. Joint EMC/SI/PI EMC Eur. Symp.*, 2021, pp. 831–834.
- [5] Y. Liu et al., "Far-end crosstalk analysis for stripline with inhomogeneous dielectric layers (IDL)," in *Proc. IEEE Int. Joint EMC/SI/PI EMC Eur. Symp.*, 2021, pp. 825–830.
- [6] S. Yong, K. Cai, B. Sen, J. Fan, V. Khilkevich, and C. Sui, "A comprehensive and practical way to look at crosstalk for transmission lines with mismatched terminals," in *Proc. IEEE Symp. Electromagn. Compat., Signal Integr., Power Integr.*, 2018, pp. 538–543.
- [7] S. Yong et al., "Prepreg and core dielectric permittivity (ϵ_r) extraction for fabricated striplines' far-end crosstalk modeling," *IEEE Trans. Electromagn. Compat.*, vol. 64, no. 1, pp. 209–218, Feb. 2022.
- [8] Y. Guo et al., "Far-end crosstalk control strategy for high-volume high-speed PCB manufacturing: The concept of critical resin content percent," in *Proc. IEEE Int. Joint EMC/SI/PI EMC Eur. Symp.*, 2021, pp. 820–824.
- [9] H. Zhang, S. Krooswyk, and J. Ou, *High Speed Digital Design: Design of High Speed Interconnects and Signaling*. Amsterdam, The Netherlands: Elsevier, 2015, pp. 129–131.
- [10] X. Ye, A. Sutono, D. Liu, and V. Gupta, "Extended unterminated line (EUL) for accurate and efficient crosstalk measurement," in *Proc. IEEE Int. Symp. Electromagn. Compat. IEEE Asia-Pacific Symp. Electromagn. Compat.*, Singapore, 2018, pp. 155–159.
- [11] Y. Guo et al., "Robust extended unterminated line (EUL) crosstalk characterization techniques for high-speed interconnect," in *Proc. IEEE Int. Symp. Electromagn. Compat. Signal/Power Integr.*, 2020, pp. 155–157.
- [12] J. Hsu, T. Su, K. Xiao, X. Ye, S. Huang, and Y. L. Li, "Delta-L methodology for efficient PCB trace loss characterization," in *Proc. 9th Int. Microsyst., Packag., Assem. Circuits Technol. Conf.*, 2014, pp. 113–116.
- [13] Y. Chen, B. Chen, J. He, R. Zai, J. Fan, and J. Drewniak, "De-embedding comparisons of 1X-reflect SFD, 1-port AFR, and 2X-Thru SFD," in *Proc. IEEE Int. Symp. Electromagn. Compat. IEEE Asia-Pacific Symp. Electromagn. Compat.*, 2018, pp. 160–164.
- [14] Y. Liu et al., "S-parameter de-embedding error estimation based on the statistical circuit models of fixtures," *IEEE Trans. Electromagn. Compat.*, vol. 62, no. 4, pp. 1459–1467, Aug. 2020.
- [15] S. Yong et al., "A practical de-embedding error analysis method based on statistical circuit models of fixtures," in *Proc. IEEE Int. Symp. Electromagn. Compat., Signal Power Integr.*, 2019, pp. 45–50.
- [16] S. H. Hall and H. L. Heck, *Advanced Signal Integrity for High-Speed Digital Designs*. Hoboken, NJ, USA: Wiley, 2009.
- [17] S. S. Bedair, "Characteristics of some asymmetrical coupled transmission lines (short paper)," *IEEE Trans. Microw. Theory Techn.*, vol. MTT-32, no. 1, pp. 108–110, Jan. 1984.
- [18] K. C. Gupta, R. Garg, I. Bahl, and P. Bhartia, *Microstrip Lines and Slotlines*, 2nd ed. Norwood, MA, USA: Artech House, 1996.
- [19] G. Parry, "Etching process and technologies," in *Printed Circuits Handbook*, 7th ed., C. Coombs and H. Holden, Eds. New York, NY, USA: McGraw-Hill, 2016, ch. 37.
- [20] Y. Chen et al., "Signal-signal D-probe and unified launch pad designs," *IEEE Electromagn. Compat. Mag.*, vol. 7, no. 3, pp. 101–106, Jul.–Sep. 2018.
- [21] Intel Memory Latency Checker, 2022. [Online]. Available: <https://www.intel.com/content/www/us/en/developer/articles/tool/intelrmemory-latency-checker.html>
- [22] S. Yong et al., "Prepreg and core dielectric permittivity (ϵ_r) extraction for fabricated striplines' far-end crosstalk modeling," *IEEE Trans. Electromagn. Compat.*, vol. 64, no. 1, pp. 209–218, Feb. 2022.
- [23] D. M. Pozar, *Microwave Engineering*, 4th ed. Hoboken, NJ, USA: Wiley, 2012.



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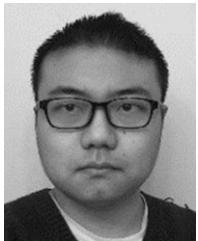
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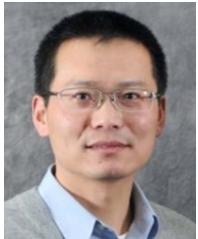
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