

Efficient DC and AC Impedance Calculation for Arbitrary-Shape and Multilayer PDN Using Boundary Integration

Ling Zhang¹, Member, IEEE, Jack Juang, Student Member, IEEE, Zurab Kiguradze, Bo Pu², Senior Member, IEEE, Shuai Jin, Member, IEEE, Songping Wu³, Senior Member, IEEE, Zhiping Yang⁴, Fellow, IEEE, Er-Ping Li⁵, Fellow, IEEE, Jun Fan⁶, Fellow, IEEE, and Chulsoon Hwang⁷, Senior Member, IEEE

Abstract—This article presents an efficient methodology based on boundary integration to calculate the dc and ac impedance of power distribution networks (PDNs) for arbitrary-shape and multilayer printed circuit boards (PCBs). The proposed method adopts a boundary element method to extract inductances for the arbitrary parallel-plane shapes. Subsequently, the equivalent circuit formed by the via inductances and plane capacitances is solved using the node voltage method. By merging the parallel and serial inductances and simplifying the equivalent circuit, the computation time can be significantly reduced for a large number of vias and layers. This matrix manipulation strategy can be applied to various PCB structures without human intervention or commercial circuit solvers. Moreover, a contour integral method is employed to calculate the dc resistances for arbitrary shape and multilayer PDNs. Therefore, the wideband PDN impedance from dc to ac frequencies can be efficiently calculated through 1-D boundary integration, which can be performed more quickly than full-wave simulations. The proposed method can aid in the development of electronic design automation tools for PDN design.

Index Terms—AC impedance, boundary element method (BEM), boundary integration, contour integral method, dc impedance, electronic design automation, power distribution network (PDN).

I. INTRODUCTION

EFFICIENTLY and accurately simulating the direct-current (dc) and alternating-current (ac) impedance of power distribution networks (PDNs) is crucial to the power integrity

Manuscript received December 4, 2021; revised February 27, 2022; accepted March 25, 2022. Date of publication April 14, 2022; date of current version May 6, 2022. This work was supported in part by the National Science Foundation under Grant IIP-1916535, in part by the Google Faculty Research Award, in part by the Zhejiang Provincial Natural Science Foundation of China (ZPNSFC) under Grant LD21F010002, and in part by the Natural Science Foundation of China (NSFC) under Grants 62071424 and 62027805. (Corresponding author: Ling Zhang.)

Ling Zhang and Er-Ping Li are with the College of Information Science and Electronic Engineering, Zhejiang University, Hangzhou 310027, China (e-mail: lingzhang_zju@zju.edu.cn; liep@zju.edu.cn).

Jack Juang, Zurab Kiguradze, Bo Pu, Jun Fan, and Chulsoon Hwang are with the Electromagnetic Compatibility Laboratory, Missouri University of Science and Technology, Rolla, MO 65409 USA (e-mail: jjryb@mst.edu; kiguradzz@mst.edu; bobpu@ieee.org; jfan@mst.edu; hwangc@mst.edu).

Shuai Jin, Songping Wu, and Zhiping Yang are with the Google Inc., Mountain View, CA 94043 USA (e-mail: shuaijin@google.com; songpingwu@google.com; zhipingyang@google.com).

Digital Object Identifier 10.1109/TSIPL.2022.3164037

of integrated circuits (ICs) in the pre-layout design and optimization stage. However, it is generally inefficient to

perform impedance modeling using commercial full-wave simulation tools for complex PDN designs with irregular board shapes and multi-layer stackups. Some modeling methodologies have been developed to calculate the ac impedance for PDNs [1]–[9]. The cavity model method [1] can efficiently calculate inductances between vias. Based on the cavity model approach, equivalent circuits were reconstructed for multiple PDN structures, and specific matrix rules were developed to simplify the circuits [2] [3]. But the cavity model method [1]–[3] can only handle rectangular board shapes. The plane-pair partial equivalent element circuit (PPP) method [4] can tackle irregular plane shapes, but it requires solving a 2D mesh circuit and is not computationally efficient for optimization purposes.

Some boundary integration methods [5]–[10] that require only 1D discretization and integration along the boundary can deal with irregular plane shapes. An integral-equation equivalent circuit (IEEC) method was proposed to calculate the impedance for single-layer [5] and multi-layer [6] PDN structures. A similar contour integral method was proposed to calculate the voltage distribution and impedance between the two parallel planes [7]. Also, a boundary integral-equation method was developed to compute the radial scattering matrix for any irregular-shape plate pair [8]. A fast contour integral method was further proposed for wideband power integrity analysis [9]. However, these boundary integration methods [5]–[9] have issues with low-frequency breakdown and hence are not suitable for calculating the PDN impedance from dc to ac frequencies. A boundary element method (BEM) has been proposed [10] to calculate quasi-static inductances for arbitrary-shape parallel planes, which resolves the low-frequency breakdown issue. However, the impedance calculation for multi-layer PDN structures was not addressed in [10].

The dc impedance, which determines the IR drop, is also a critical factor for PDN systems. Some methods using 2-D finite-difference discretization [11], [12] have been adopted to accelerate the calculation of the dc IR drop, but these methods are not adequately time-efficient because 2-D meshes are required. A contour integral method (CIM) that requires only

1-D boundary integration has been developed to rapidly compute

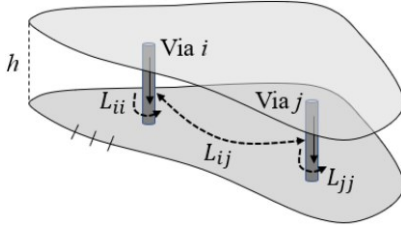


Fig. 1. Illustration of the BEM for calculating quasi-static inductances between vertical vias in arbitrary-shape cavities.

dc resistances for arbitrary-shape power planes [13]. However, to the best of our knowledge, there are no well-developed methods or commercial tools that can efficiently compute dc and ac impedances over a wide frequency range for complex PDN structures. Some commercial tools are commonly used in industries to simulate dc and ac impedances separately; however, such approaches are too time-consuming for repetitive design optimizations.

This article proposes an approach that can rapidly calculate dc and ac impedances based on boundary integration. An equivalent L - C circuit is constructed for multilayer PDN structures by extracting inductances based on the BEM. Similarly, an equivalent resistive circuit is created for multilayer designs by utilizing the CIM. Hence, the ac and dc impedances can both be computed by solving the two circuits. Instead of using commercial circuit solvers [2], [3], such as SPICE, a matrix manipulation method is introduced to simplify and solve the equivalent circuits based on the well-known node voltage method.

Compared with the previous works [2], [3], [10], [13], this article presents a novel method that can simultaneously address dc and ac for multilayer PDN structures. Moreover, in contrast to the traditional equivalent-circuit modeling approach based on the cavity model [2], [3], the proposed method can handle irregular board shapes without the need for commercial circuit solvers. The proposed methodology can aid in developing electronic design automation (EDA) tools for PDN design and optimization independent of other commercial products.

The rest of this article is organized as follows. In Section II, the BEM and CIM are briefly introduced. Section III elaborates the matrix manipulation method used to solve the equivalent circuit network and simplify the matrices based on the node voltage method. Full-wave simulations are used to validate the approach in Section IV. Finally, Section V concludes this article.

II. BOUNDARY INTEGRATION METHODS

This section briefly introduces the boundary integration method adopted in this article—the CIM for calculating dc resistances [13] and the BEM for calculating ac inductances [10]. These two methods were both derived from Green's

second identity. The corresponding equations can be found in [10] and [13], and are not explicitly described in this article.

A. Boundary Element Method

Based on Green's second identity, Friedrich and Leone [10] derived the BEM to calculate quasi-static inductances between

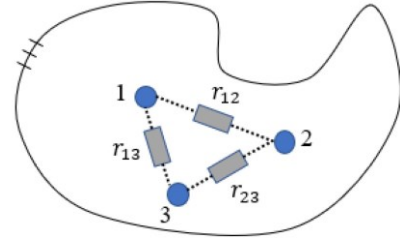


Fig. 2. Illustration of the CIM for calculating the resistance network between nodes in arbitrary-shape metal planes.

parallel planes, as illustrated in Fig. 1. This method requires that the plane edge can be approximated as a perfect magnetic conductor (PMC), which is a reasonable approximation when the plate separation h is much smaller than the wavelength and plane size. Moreover, because the quasi-static inductance is calculated, the BEM cannot work well at high frequencies when the printed circuit board (PCB) starts to resonate. However, the abovementioned preconditions are well suited for typical PDN scenarios in PCBs with solid metal layers at frequencies below a few hundred megahertz.

The calculation process of the BEM [10] is organized and shown in the Appendix section, and (19)–(32) are used to calculate the inductance matrix. In this process, the small port approximation reduces the number of segments by treating each circular port as a single segment. Each port needs to be excited to calculate the inductance terms (including the self-terms) between this port and the other cells. The calculation time increases with the via number nearly proportionally rather than exponentially. Afterward, an equivalent circuit with inductances and capacitances can be produced for multilayer structures. In Section III, a matrix manipulation method for solving the L - C circuit will be described.

B. Contour Integral Method

The CIM [13] was proposed for calculating the dc resistances between conductive nodes within an arbitrary-shape metal plane. The boundary, including the outer and inner boundaries, is approximated and discretized into straight segments. The equations used for the CIM calculation are organized and explained in the Appendix section, from (33) to (42). A mesh resistor network example is illustrated in Fig. 2, where three conductive nodes are used as an example. There is a branch resistor between every two nodes in the mesh resistor network. In multilayer PDN structures, this mesh resistor network and the via resistances can

be integrated to obtain the total dc resistance, which will be discussed in Section III.

III. SPECIALIZED CIRCUIT SOLVER

A. AC Network

For a multilayer PDN structure, an equivalent circuit can be built by connecting the via inductances calculated by the BEM and the plane capacitances. A simple PDN example with three layers and four vias is shown in Fig. 3 to aid in the following

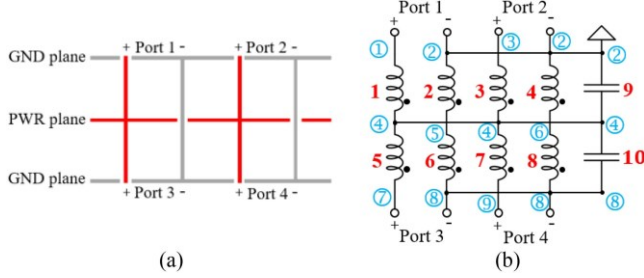


Fig. 3. Simple example to demonstrate the equivalent L - C circuit for a multilayer PCB. (a) Stackup and vias of the PCB. (b) Equivalent L - C circuit. Numbers with circles represent node numbers, and numbers without circles represent branch numbers.

explanation. Fig. 3(a) shows the stackup and vias of the PCB, and Fig. 3(b) depicts the equivalent circuit network.

For the example shown in Fig. 3, four ports are defined between the power vias and ground vias on the top and bottom layers. In this article, the Z -parameter matrix of the PDN is calculated first. Afterward, the Z -parameter matrix is cascaded to the Z -parameter of the decaps to be placed at the corresponding locations to obtain the total PDN impedance because the same PCB will be used to connect with different decaps iteratively in the decap optimization process. Using Z -parameters for calculation is much more efficient than repeatedly solving the entire circuit.

Fig. 3(b) shows the node and branch number assignment for an equivalent circuit. The node and branch numbers are marked by numbers with and without circles, respectively. There are nine nodes ($n = 9$) and ten branches ($b = 10$) in total. The branch numbers are successively assigned to different via segments in different cavities. The node numbers are also assigned consecutively, except that the node numbers given to nodes connecting to the same plane are identical. An algorithm that automatically assigns node and branch numbers for different PCB stackups can be conveniently designed following this strategy.

B. Node Voltage Method

The node voltage method is a well-known approach for solving circuits using matrix formulations [14]. The process of the node voltage method can be summarized by

$$(A \cdot Y_b \cdot A^T) \cdot V_n = I_n \quad (1)$$

where A is the reduced incidence matrix with dimension $n \times b$, in which n is the number of nodes and b is the number of branches; Y_b is the branch admittance matrix with size $b \times b$; and V_n and I_n are the node voltage matrix and node current matrix with size $n \times 1$, respectively.

In the reduced incidence matrix A , each row corresponds to a node, and each column corresponds to a branch. The elements of A are defined as

$$a_{jk} = \begin{cases} 1, & \text{branch } k \text{ leaves node } j \\ -1, & \text{branch } k \text{ enters node } j \\ 0, & \text{branch } k \text{ not connected to } j. \end{cases}$$

It is worth noting that (1) can be regarded as a matrix form of Kirchhoff's current law (KCL). If there are n nodes in the circuit, there will be n KCL equations corresponding to the n rows of the matrix operation in (1). One can find that these KCL equations are not independent due to undefined reference potential, which means that the original matrix $(A \cdot Y_b \cdot A^T)$ is a singular matrix that cannot be inverted. To make the matrix $(A \cdot Y_b \cdot A^T)$ invertible, a standard solution in the node voltage method is to select a reference node, so that all the other voltages will be referenced to this node. The corresponding row and column of this node must also be deleted from the matrix $(A \cdot Y_b \cdot A^T)$.

For example, the matrix A in Fig. 3(b) is

$$A = \begin{bmatrix} 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 1 & 0 & 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ -1 & 0 & -1 & 0 & 1 & 0 & 1 & 0 & -1 & 1 \\ 0 & -1 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & -1 & 0 & 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 & -1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & -1 & 0 & -1 & 0 & -1 \\ 0 & 0 & 0 & 0 & 0 & 0 & -1 & 0 & 0 & 0 \end{bmatrix}. \quad (3)$$

The impedance matrix for the branches Z_b is

$$Z_b = \begin{bmatrix} j\omega [L_{\text{cavity}_1}] & 0 & 0 & 0 & 0 \\ 0 & 0 & 2] & 0 & 0 \\ & & & \frac{1}{j\omega C_9} & 0 \\ 0 & j\omega [L_{\text{cavity}_-} & & \frac{1}{j\omega C_{10}} & \\ & & & & \\ & & & & \\ 0 & & & & 0 \\ & & & & 0 \end{bmatrix} \quad (4)$$

where ω is the angular frequency, C_9 and C_{10} are the capacitances for the two cavities represented by branches 9

and 10, respectively, $L_{\text{cavity_1}}$ and $L_{\text{cavity_2}}$ are the inductance matrices for the vias in the two cavities, respectively, expressed as follows:

$$[L_{\text{cavity_1}}] = \begin{bmatrix} L_{11} & L_{12} & L_{13} & L_{14} \\ L_{21} & L_{22} & L_{23} & L_{24} \\ L_{31} & L_{32} & L_{33} & L_{34} \\ L_{41} & L_{42} & L_{43} & L_{44} \end{bmatrix} \quad (5)$$

$$L_{\text{cavity_2}} = \begin{bmatrix} L_{55} & L_{56} & L_{57} & L_{58} \\ L_{65} & L_{66} & L_{67} & L_{68} \\ L_{75} & L_{76} & L_{77} & L_{78} \\ L_{85} & L_{86} & L_{87} & L_{88} \end{bmatrix} \quad (6)$$

where L_{ij} denotes the mutual inductance between branch i and j , and L_{ii} is the self-inductance of branch i .

The branch admittance matrix Y_b is the inverse matrix of the branch impedance matrix Z_b , namely

$$Y_b = Z_b^{-1}. \quad (7)$$

As mentioned earlier, a reference node must be selected, and the corresponding row and column must be removed from the matrix $(A \cdot Y_b \cdot A^T)$. Thus, the relationship between V_n and I_n

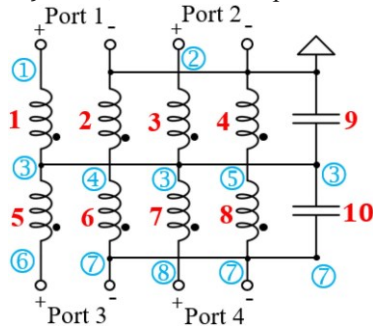


Fig. 4. New node and branch number assignment obtained after choosing node 2 in Fig. 3(b) as the reference node.

can be acquired as

$$V_n = (A \cdot Y_b \cdot A^T)^{-1} \cdot I_n. \quad (8)$$

Namely, the Z-matrix Z_n for all defined nodes (except for the reference node) is

$$Z_n = (A \cdot Y_b \cdot A^T)^{-1}. \quad (9)$$

For the case in which the chosen reference node is node 2, the new node number assignment after removing the reference node is shown in Fig. 4. The node Z-matrix Z_n is then an 8×8 matrix. Eventually, we need a 4×4 Z-matrix for ports 1–4. Therefore, Z_n must be partially extracted by selecting the node indices of the corresponding ports.

The reference node (original node 2 in Fig. 3) is already the negative node for ports 1 and 2; hence, ports 1 and 2

correspond to nodes 1 and 2, respectively. However, the negative node for the bottom ports 3 and 4 is node 7, which is different from the reference node. Thus, node 7 must also be considered to obtain the Z-parameters corresponding to ports 3 and 4.

The node Z-matrix Z_n describes the relationship between V_n and I_n

$$\begin{bmatrix} V_{n1} \\ \vdots \\ V_{n6} \\ V_{n7} \\ V_{n8} \end{bmatrix} = \begin{bmatrix} Z_{11} & \cdots & Z_{16} & Z_{17} & Z_{18} \\ \vdots & \ddots & \vdots & \vdots & \vdots \\ Z_{61} & \cdots & Z_{66} & Z_{67} & Z_{68} \\ Z_{71} & \cdots & Z_{76} & Z_{77} & Z_{78} \\ Z_{81} & \cdots & Z_{86} & Z_{87} & Z_{88} \end{bmatrix} \cdot \begin{bmatrix} I_{n1} \\ \vdots \\ I_{n6} \\ I_{n7} \\ I_{n8} \end{bmatrix}. \quad (10)$$

Because ports 3 and 4 share the same negative node, which is node 7, I_{n6} , I_{n7} , and I_{n8} should satisfy

By substituting (11) into (10), we can obtain (12) shown at the bottom of this page. Specifically, to acquire the Z-parameters corresponding to the bottom ports, we must subtract the rows and columns corresponding to the negative nodes of the bottom ports from the rows and columns corresponding to the positive nodes.

Finally, the Z-parameter matrix for ports 1–4 can be extracted from (12) as

$$Z_{\text{final}} = \begin{bmatrix} Z_{11} & Z_{12} & Z_{16} - Z_{17} & Z_{18} - Z_{17} \\ Z_{21} & Z_{22} & Z_{26} - Z_{27} & Z_{28} - Z_{27} \\ \begin{pmatrix} Z_{61} \\ -Z_{71} \end{pmatrix} & \begin{pmatrix} Z_{62} \\ -Z_{72} \end{pmatrix} & \begin{pmatrix} Z_{66} - Z_{76} \\ -Z_{67} + Z_{77} \end{pmatrix} & \begin{pmatrix} Z_{68} - Z_{78} \\ -Z_{67} + Z_{77} \end{pmatrix} \\ \begin{pmatrix} Z_{81} \\ -Z_{71} \end{pmatrix} & \begin{pmatrix} Z_{82} \\ -Z_{72} \end{pmatrix} & \begin{pmatrix} Z_{86} - Z_{76} \\ -Z_{87} + Z_{77} \end{pmatrix} & \begin{pmatrix} Z_{88} - Z_{78} \\ -Z_{87} + Z_{77} \end{pmatrix} \end{bmatrix}. \quad (13)$$

The matrix manipulation method introduced previously can be applied to more complex scenarios. The inductances and total impedance matrix can be bridged through the node voltage method and Z-matrix manipulation to avoid the need for SPICE-like circuit solvers. The impedance matrix can be further cascaded with Z-matrices of decaps to attain the total impedance of a PDN system.

C. Matrix Reduction

Because the number of nodes and branches increases with the number of vias and layers, the computation speed of the previous matrix calculations will decrease correspondingly. The most time-consuming calculation step is (9), which requires matrix multiplication and inverse calculation. To accelerate the calculation process, we can merge parallel and serial inductances to reduce the number of nodes and branches and, thus, reduce the matrix size of A and Y_b .

Kim *et al.* [2] and Shringarpure *et al.* [3] introduced specific rules for merging inductances and simplifying equivalent circuits for complex production-level PCBs. However, it is

difficult to explicitly program these rules or generalize them to various board configurations without human intervention. This article introduces a criterion that automatically identifies and merges branches based on the assigned node and branch numbers.

Fig. 5 shows an example for identifying parallel and serial branches that can be combined. Branches i and j are parallel branches: the

voltages on these two branches are equal because both of their terminal nodes are connected, namely $V_i = V_j$.

$$I_{n7} = -(I_{n6} + I_{n8}). \quad (11)$$

$$\begin{bmatrix} V_{n1} \\ \vdots \\ \begin{pmatrix} V_{n6} \\ -V_{n7} \end{pmatrix} \\ \begin{pmatrix} V_{n8} \\ -V_{n7} \end{pmatrix} \end{bmatrix} = \begin{bmatrix} Z_{11} & \cdots & Z_{16} - Z_{17} & Z_{18} - Z_{17} \\ \vdots & \ddots & \vdots & \vdots \\ \begin{pmatrix} Z_{61} \\ -Z_{71} \end{pmatrix} & \cdots & \begin{pmatrix} Z_{66} - Z_{76} \\ -Z_{67} + Z_{77} \end{pmatrix} & \begin{pmatrix} Z_{68} - Z_{78} \\ -Z_{67} + Z_{77} \end{pmatrix} \\ \begin{pmatrix} Z_{81} \\ -Z_{71} \end{pmatrix} & \cdots & \begin{pmatrix} Z_{86} - Z_{76} \\ -Z_{87} + Z_{77} \end{pmatrix} & \begin{pmatrix} Z_{88} - Z_{78} \\ -Z_{87} + Z_{77} \end{pmatrix} \end{bmatrix} \cdot \begin{bmatrix} I_{n1} \\ \vdots \\ I_{n6} \\ I_{n8} \end{bmatrix}$$

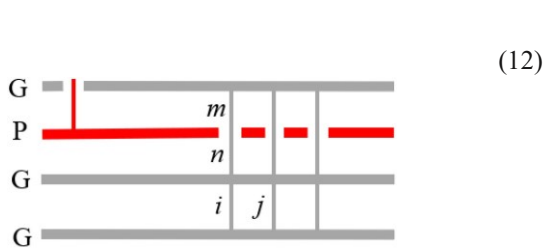


Fig. 5. Illustration of parallel and serial branches that can be merged.

Branches m and n are serial branches: the currents on the two branches are identical because there is only one current path from branch m to n , namely $I_m = I_n$. Other parallel and serial branches that satisfy the requirements are not marked in Fig. 5 to clarify the following explanation.

Assume that N is the total number of inductance branches, matrix $[L]$ is a large inductance matrix including all inductance branches, and matrix $[B]$ is the inverse of $[L]$, as expressed in the following:

$$\begin{bmatrix} V_1 \\ \vdots \\ V_m \\ \vdots \\ V_n \\ \vdots \\ V_N \end{bmatrix} = j\omega \begin{bmatrix} L_{11} & \cdots & L_{1m} & \cdots & L_{1n} & \cdots & L_{1N} \\ \vdots & \ddots & \vdots & \cdots & \vdots & \cdots & \vdots \\ L_{m1} & \vdots & L_{mm} & \cdots & L_{mn} & \cdots & L_{mN} \\ \vdots & \vdots & \vdots & \ddots & \vdots & \cdots & \vdots \\ L_{n1} & \vdots & L_{nm} & \vdots & L_{nn} & \cdots & L_{nN} \\ \vdots & \vdots & \vdots & \vdots & \vdots & \ddots & \vdots \\ L_{N1} & \vdots & L_{Nm} & \vdots & L_{Nn} & \vdots & L_{NN} \end{bmatrix} \begin{bmatrix} I_1 \\ \vdots \\ I_m \\ \vdots \\ I_n \\ \vdots \\ I_N \end{bmatrix} \quad (14)$$

$$j\omega \begin{bmatrix} I_1 \\ \vdots \\ I_i \\ \vdots \\ I_j \\ \vdots \\ I_N \end{bmatrix} = \begin{bmatrix} B_{11} & \cdots & B_{1i} & \cdots & B_{1j} & \cdots & B_{1N} \\ \vdots & \ddots & \vdots & \cdots & \vdots & \cdots & \vdots \\ B_{i1} & \vdots & B_{ii} & \cdots & B_{ij} & \cdots & B_{iN} \\ \vdots & \vdots & \vdots & \ddots & \vdots & \cdots & \vdots \\ B_{j1} & \vdots & B_{ji} & \vdots & B_{jj} & \cdots & B_{jN} \\ \vdots & \vdots & \vdots & \vdots & \vdots & \ddots & \vdots \\ B_N & \vdots & B_{Ni} & \vdots & B_{Nj} & \vdots & B_{NN} \end{bmatrix} \begin{bmatrix} V_1 \\ \vdots \\ V_i \\ \vdots \\ V_j \\ \vdots \\ V_N \end{bmatrix} \quad (15)$$

Assume that $V_{m(n)}$ and $I_{m(n)}$ are the total branch voltage and current after branches m and n have been merged, and $V_{i(j)}$ and $I_{i(j)}$ are the total branch voltage and current after branches i and j have been merged. Here, the following relationship should be satisfied:

$$\left\{ \begin{aligned} & V_{m(n)} = V_m + V_n \\ & I_{i(j)} = I_i + I_j \\ & V_{i(j)} = V_i = V_j \end{aligned} \right\} \quad (16)$$

$$V_{m(n)} = V_m + V_n$$

$$I_{i(j)} = I_i + I_j$$

$$V_{i(j)} = V_i = V_j$$

By substituting (16) into (14) and (15), it is simple to derive (17) and (18) shown at the bottom of the next page.

From (17) and (18), we can conclude that to merge serial inductances, the corresponding rows and columns in the large inductance matrix $[L]$ should be summed. Similarly, to combine

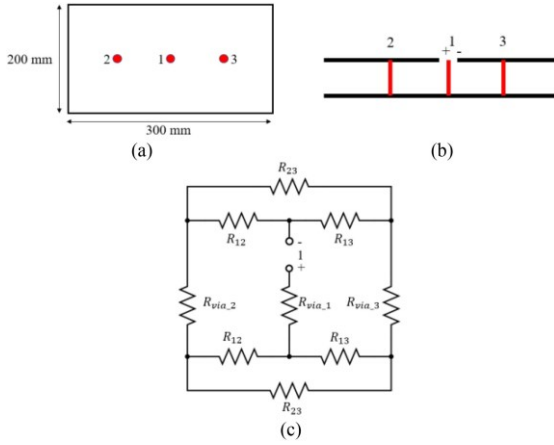


Fig. 6. Example of a constructed resistive network. (a) Top view of the board. (b) Side view. (c) Equivalent resistive network.

parallel inductances, the corresponding rows and columns in the

matrix $[B]$ should be added. Multiple serial and parallel branches in more complex scenarios can be automatically determined from predefined branch and node numbers using the same strategy without human intervention. The merged inductance matrix can then be substituted into the branch impedance matrix Z_b . The branch and node numbers can be subsequently reorganized after the merging process so that the node voltage method can be applied to calculate the total impedance.

D. DC Network

The ac network neglects the impact of dc resistance, which dominates PDN impedance at near-dc frequencies. In this article, the dc impedance is calculated separately by building a similar equivalent circuit formed by dc resistances. In Fig. 6, a simple example demonstrates how the resistive network is constructed by including plane resistances, which can be computed by the CIM, and via resistances, which can be calculated from the resistance of a cylindrical conductor.

In this example, there are three conductive vias and two metal layers. Via 1 is connected to the bottom layer but not to the top layer. Vias 2 and 3 are connected to the top and bottom layers. There is an antipad between Via 1 and the top layer. The dc resistance observation port is between the upper end of Via 1 and the nearest location on the top layer around the antipad.

Fig. 6(c) presents an equivalent resistive circuit for this two-layer example. $R_{via,1}$, $R_{via,2}$, and $R_{via,3}$ represent the via resistances, and R_{12} , R_{13} , and R_{23} denote the plane resistances between the contacting nodes with the metal planes for the three vias, which can be calculated from the CIM approach. Thus, a more complicated resistive network can be constructed for more complex board structures in the same way. The total

dc impedance can be calculated by employing the node voltage method, which is more straightforward than calculating the ac impedance and hence is omitted.

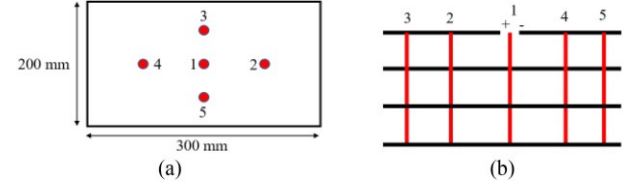


Fig. 7. Simulation case to verify the dc resistance calculation. (a) Top view. (b) Side view. The metal plane thickness is 0.02 mm, the distance between two adjacent metal layers is 0.05 mm, and the via radius is 0.1 mm.

TABLE I
DC RESULT COMPARISON

	CIM	CST
Result	1.59 mΩ	1.55 mΩ
Time	<0.1 s	>10 min

IV. SIMULATION VALIDATION

A. DC Verification

Some commercial simulation tools, such as the stationary current solver in CST [15], can simulate dc resistance for complex metal structures. The example shown in Fig. 7 is utilized to verify the resistive network through a comparison with CST simulation results. In this simulation case, there are five vias and four layers. Via 1 is not connected to the top layer but is connected to the other three layers. Vias 2–4 are connected to all four layers with an equal distance to Via 1. The equivalent resistive network is more complicated than that in Fig. 6(c) but can be constructed using the same approach.

The complex resistive circuit for the board structure in Fig. 7 is again solved using the node voltage method. The result is given in Table I. The resistive circuit based on the CIM provides

1.59 mΩ, whereas the CST stationary current solver outputs 1.55 mΩ, with a 0.04 mΩ deviation only. However, the CIM requires only 0.1 s, whereas the CST simulation requires more than 10 min.

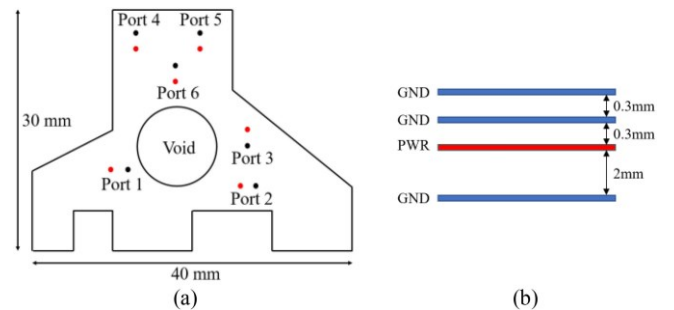


Fig. 8. Simulation verification case. (a) Board shape and port locations. (b) Board stackup.

B. AC Verification

The high-frequency structure simulator (HFSS) simulation tool [16] is utilized for comparison to verify the ac impedance calculation based on the BEM and node voltage method. Fig. 8 shows the board shape, port locations, and stackup. The board has an irregular shape that cannot be handled by the cavity model method [1]. There are six ports distributed on the board, and the power and ground vias for each port are separated by 2 mm. The ground and power vias are all stitched from the first layer to the last layer. The ground vias are connected with all three ground layers and disconnected with the power layer through antipads, and vice versa for all the power vias. The dielectric constant is 4.4. Since the proposed method neglects the influence of dielectric loss, the loss tangent of the dielectric material is set to 0. Port 1 is the impedance observation port, and ports 2–6 are connected to decaps. In the HFSS simulation, the S-parameters of decap models are simulated and then connected to the S-parameters of decap models. The parameters of the decap models used in this article are listed in Table II, including the capacitance, equivalent series resistance (ESR), and equivalent series inductance (ESL).

Using the BEM and the node voltage method, the Z-parameter of the board can be calculated and cascaded with the Z-parameters of the decaps. The entire process takes less than 1 s,

TABLE II

Model #	Capacitance (μF)	ESL (nH)	ESR (m Ω)
C1	0.47	0.18	18.3
C2	2.2	0.20	7.2
C3	10	0.26	5.2
C4	47	0.15	2.9
C5	330	0.46	1.2

TABLE III

TIME COMPARISON OF BEM AND HFSS

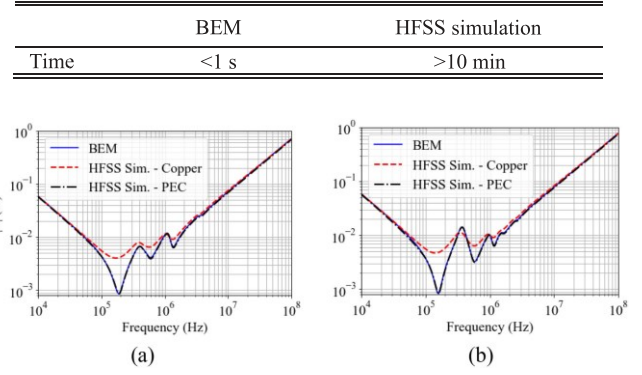


Fig. 9. Comparison of results obtained by the BEM and HFSS simulations for the case shown in Fig. 8. Port 1 is the impedance observation port. (a) Ports 2–6 are connected to decap models C5, C4, C3, C2, and C3, respectively, on the top. (b) Ports 2, 5, and 6 are connected to decap models C5, C2, and C3 on the bottom. Ports 3 and 4 are connected to decap models C4 and C3 on the top.

while the HFSS simulation requires more than 10 min, as given in Table III. Fig. 9 compares the impedances obtained by the BEM and HFSS simulation. Fig. 9(a) shows the results obtained when five top decaps are added to ports 2–6, and Fig. 9(b) shows the results obtained by adding two top decaps and three bottom decaps.

Two different metal materials, i.e., copper and perfect electric conductor (PEC), were used for the HFSS simulation. From Fig. 9, it can be concluded that the BEM result matches well with the HFSS simulation based on PEC. For copper, there are visible

$$\begin{bmatrix} V_1 \\ \vdots \\ V_{m(n)} \\ \vdots \\ V_N \end{bmatrix} = j\omega \begin{bmatrix} L_{11} & \cdots & L_{1m} + L_{1n} & \cdots & L_{1N} \\ \vdots & \ddots & \vdots & \ddots & \vdots \\ \left(\begin{smallmatrix} L_{m1} \\ +L_{n1} \end{smallmatrix} \right) & \cdots & \left(\begin{smallmatrix} L_{mm} + L_{nn} \\ +L_{nm} + L_{nn} \end{smallmatrix} \right) & \cdots & \left(\begin{smallmatrix} L_{mN} \\ +L_{nN} \end{smallmatrix} \right) \\ \vdots & \cdots & \vdots & \ddots & \vdots \\ L_{N1} & \cdots & L_{Nm} + L_{Nn} & \cdots & L_{NN} \end{bmatrix} \cdot \begin{bmatrix} I_1 \\ \vdots \\ I_{m(n)} \\ \vdots \\ I_N \end{bmatrix} \quad (17)$$

$$j\omega \begin{bmatrix} I_1 \\ \vdots \\ I_{i(j)} \\ \vdots \\ I_N \end{bmatrix} = \begin{bmatrix} B_{11} & \cdots & B_{1i} + B_{1j} & \cdots & B_{1N} \\ \vdots & \ddots & \vdots & \ddots & \vdots \\ \left(\begin{smallmatrix} B_{i1} \\ +B_{j1} \end{smallmatrix} \right) & \cdots & \left(\begin{smallmatrix} B_{ii} + B_{ij} \\ +B_{ji} + B_{jj} \end{smallmatrix} \right) & \cdots & \left(\begin{smallmatrix} B_{iN} \\ +B_{jN} \end{smallmatrix} \right) \\ \vdots & \vdots & \vdots & \ddots & \vdots \\ B_{N1} & \cdots & B_{Ni} + B_{Nj} & \cdots & B_{NN} \end{bmatrix} \cdot \begin{bmatrix} V_1 \\ \vdots \\ V_{i(j)} \\ \vdots \\ V_N \end{bmatrix} \quad (18)$$

DECAP MODELS

deviations between the BEM results and HFSS simulation at the resonance dips. The resonance dips using copper in the simulation are slightly higher than the simulation values using PEC and the calculated values using BEM. This is reasonable because adding copper resistance in the L - C series resonances at the resonance dips will raise the dip values. The discrepancies at the resonance peaks are, however, negligible. Resonance peaks of PDN impedance are usually more critical than resonance dips as they can violate a target impedance more easily.

Despite slight deviations from full-wave simulations due to the negligence of resistance, the proposed method in this article is still a powerful tool for rapidly estimating impedance in complex PDN systems.

C. DC + AC Verification

Simulating PDN impedance at dc and ac frequencies usually requires different simulation tools. Hence, it is time-consuming

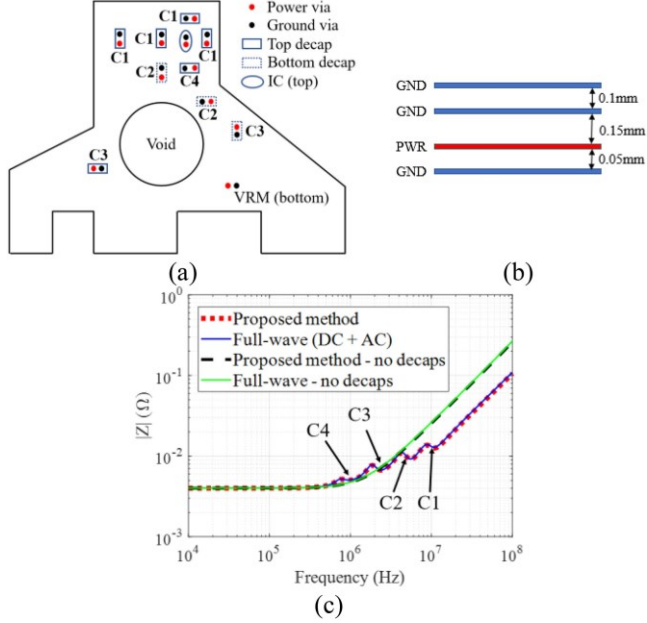


Fig. 10. Comparison of results for boundary integration and full-wave simulation from dc to ac. The metal plane thickness is 0.02 mm, and the via radius is 0.1 mm. (a) Board shape and port locations. (b) Board stackup. (c) Impedance curve comparison.

to obtain a wideband PDN impedance from dc to ac frequencies utilizing commercial full-wave simulators. In this article, the calculation time for determining the wideband PDN impedance is significantly reduced by combining the dc and ac results from the CIM and BEM.

The simulation case shown in Fig. 10 was used to verify the calculated impedance from dc to ac frequencies. Fig. 10(a) shows the locations of the IC port (the impedance observation port), voltage regulation module (VRM) port, and decap ports on the PDN board. Fig. 10(b) shows the board stackup information. Similar to the board structure in Fig. 8, the power and ground vias are stitched from the first layer to the last layer.

Because there is no commercial tool that can cover the impedance calculation from dc to ac, the dc and ac impedances were separately simulated by two different commercial tools (CST for dc impedance [15] and HFSS [16] for ac impedance) and then combined. In the dc impedance simulation with CST, copper material was used for the metal planes and vias. In contrast, PEC was used in the ac impedance simulation with HFSS to avoid dc resistance. Because VRM modeling is beyond the scope of this article, the VRM port was directly

shorted to neglect possible parasitics in the VRM. Eventually, the dc and ac simulation results were combined to represent the total impedance over a wideband frequency range.

Fig. 10(c) shows perfect agreement between the boundary integration method proposed in this paper and the full-wave simulation result with and without decaps. It can be observed that the four decap types (C1, C2, C3, and C4 given in Table II) effectively suppress the impedance curve and the high-frequency inductance value. The four bumps in the impedance curve are caused by the four decap types and are also marked in Fig. 10(c).

TABLE IV
TIME COMPARISON OF BEM AND FULL-WAVE (DC + AC)

	BEM	Full wave (dc + ac)
Time	<1 s	>15 min

The proposed method can calculate PDN impedance from dc to ac frequencies. However, to better view the physical capacitances and inductances in the impedance curve, the frequency in Fig. 10(c) is plotted in the log scale, so the frequency axis starts with 10 kHz instead of 0 Hz.

In addition, the boundary integration requires less than 1 s, while the full-wave simulations require more than 15 min, including both the dc and ac simulation, as given in Table IV. In contrast to previous works [1]–[3], our proposed method can simultaneously deal with arbitrary-shape planes and dc impedance. Moreover, our boundary integration method is more efficient than the PPP method [4] for complex board shapes.

V. CONCLUSION

This article presents an efficient method for calculating dc and ac impedances in arbitrary-shape and multilayer PDNs using 1-D boundary integration. By adopting the BEM, quasi-static inductances for arbitrary-shape parallel planes can be calculated. Subsequently, an equivalent L - C circuit can be constructed for multilayer structures. The equivalent circuit can be solved within a few seconds by applying the well-known node voltage method and a general matrix reduction approach. Using a similar CIM, the dc plane resistances in arbitrary-shape metal planes can be rapidly calculated. Thus, an equivalent resistive network can be built to calculate the dc IR drop for multilayer PDNs. Moreover, the wideband impedance from dc to ac for arbitrary-shape and multilayer PDNs can be computed without the need for commercial circuit solvers. The proposed method perfectly agrees with the full-wave simulation results but is a thousandfold faster.

Because the proposed method calculates quasi-static inductances, it is not suitable for high frequencies, where the PCB starts to have resonant modes. Nevertheless, PDN impedances are usually evaluated below a few hundred megahertz.

Thus, the proposed method is sufficiently accurate for most PDN modeling

scenarios. Although the proposed methodology can tackle arbitrary plane shapes, including voids, this method requires that the boundary, including the inner and outer boundary, can be approximated as a PMC. This precondition will lose validity for

complex structures such as meshed planes or grid PDN, although the PPP method can be considered under these circumstances. A boundary integration method was also developed for the fast ac impedance calculation of grid PDN with arbitrary shapes [17],

[18], which can be incorporated with the proposed method in this article for more complex PDN scenarios in future work. Moreover, although this article considers both dc and ac impedances, the impact of conductor resistance on ac impedance is neglected because the ESR values of decoupling capacitors are dominant in most application cases.

The proposed method considerably reduces the simulation time for PDN systems with complex board shapes, multilayered stackups, and large numbers of vias. Hence, this method can aid in EDA tool development for PDN design, such as prelayout design optimization tools [19] and machine learning applications [20].

APPENDIX

The critical equations for the BEM [10] and CIM [13] are organized and shown in this section for clarity.

A. Boundary Element Method

The board boundary must be divided into approximately straight segments to apply the BEM [10]. Assume that there are two cells m and k . The center coordinate for the observation cell k is (x_k, y_k) ; the starting location for the source cell m is (x_a, y_a) ; the ending location for the source cell is (x_e, y_e) ; the length of the cell m is l_m ; the distance between (x_k, y_k) and (x_a, y_a) is r_a .

Denote v_1 as

$$v_1 = \frac{1}{l_m} [(x_k - x_a)(x_e - x_a) + (y_k - y_a)(y_e - y_a)] \quad (19)$$

and v_2 as

$$v_2 = -\frac{1}{l_m} [(x_k - x_a)(y_e - y_a) - (y_k - y_a)(x_e - x_a)]. \quad (20)$$

First, the coefficient D_{km} is calculated by

$$D_{km} = \frac{v_2}{\pi} \left[\frac{1}{\sqrt{r_a^2 - v_1^2}} \left(\arctan \left(\frac{-v_1 + l_m}{\sqrt{r_a^2 - v_1^2}} \right) + \arctan \left(\frac{v_1}{\sqrt{r_a^2 - v_1^2}} \right) \right) - \frac{l_m}{R^2} \right] \quad (21)$$

for $v_1 \neq r_a$, where R is an arbitrary value greater than the maximum Euclidean distance between source and observation point for a given geometry.

For small circuit port cell m , or $v_1 = r_a$

$$D_{km} \approx 0, \quad \text{for small circular cell } m, \text{ or } v_1 = r_a. \quad (22)$$

The self-coefficient D_{kk} of the small circular port is

$$D_{kk} = -1 + 2\left(\frac{r_0}{R}\right)^2 \approx -1. \quad (23)$$

Then, the coefficient $\hat{G}_{km}$ is calculated as

$$\hat{G}_{km} = \frac{\mu h v_2}{4\pi S} \left[\begin{aligned} & l_m \ln \left(\frac{l_m^2 + r_a^2 - 2v_1 l_m}{R^2} \right) \\ & - v_1 \ln \left(\frac{l_m^2 + r_a^2 - 2v_1 l_m}{r_a^2} \right) \\ & - \frac{l_m^3/3 + r_a^2 l_m - l_m^2 v_1}{2R^2} - 3l_m \\ & + 2\sqrt{r_a^2 - v_1^2} \left(\arctan \left(\frac{l_m - v_1}{\sqrt{r_a^2 - v_1^2}} \right) + \arctan \left(\frac{v_1}{\sqrt{r_a^2 - v_1^2}} \right) \right) \end{aligned} \right] \quad (24)$$

where S is the board area, and h is the separation distance between the two planes.

Similar to D_{km} , the value of $\hat{G}_{km}$ is approximately zero for small circular port cell m or $v_1 = r_a$, namely

$$\hat{G}_{km} \approx 0, \quad \text{for small circular cell } m, \text{ or } v_1 = r_a. \quad (25)$$

Subsequently, the coefficient G_{km} can be calculated using

$$G_{km} \approx -\frac{\mu h}{\pi} \left[\ln \left(\frac{|\vec{r}_k - \vec{r}_m|}{R} \right) - \frac{|\vec{r}_k - \vec{r}_m|^2}{2R^2} \right] \quad (26)$$

where $|\vec{r}_k - \vec{r}_m|$ is the center-to-center distance from cell k to cell m , and G_{km} is nonzero only when cell m is on the current excitation port.

For the small circular port, the self term G_{kk} becomes

$$G_{kk} \approx -\frac{\mu h}{\pi} \ln \left(\frac{r_0}{R} \right) \quad (27)$$

where r_0 is the radius of the small circular port.

Each small circular port can be treated as a single port cell, rendering the discretization unnecessary. Assume that there are N_p small circular ports and N_b segments for the remaining boundary. Hence, the total number of cells is $N = N_p + N_b$.

The calculation process proceeds by exciting the current ports one by one to calculate the inductance terms (including the self terms) between the excitation port and other cells. The D_{km} and $\hat{G}_{km}$ terms are not related to the excitation ports and only need to be calculated once. However, for each different port excitation, the G_{km} terms need to be recalculated.

Assume that the excitation port is port j . The inductance terms between port j and other cells are

$$(\mathbf{L}) = ([\mathbf{E}] - [\mathbf{D}])^{-1} (\mathbf{G}) \quad (28)$$

where $[\mathbf{E}]$ is the identity matrix

$$(\mathbf{L}) = (L_{1j} L_{2j} \dots L_{ij} \dots L_{Nj})^T \quad (29)$$

$$(\mathbf{G}) = (G_1 G_2 \dots G_k \dots G_N)^T \quad (30)$$

$$[\mathbf{D}] = \begin{bmatrix} D_{11} & D_{12} & \dots & D_{1m} & \dots & D_{1N} \\ D_{21} & D_{22} & \dots & D_{2m} & \dots & D_{2N} \\ \vdots & & \ddots & \vdots & & \vdots \\ D_{k1} & D_{k2} & \dots & D_{km} & \dots & D_{kN} \\ \vdots & & & \vdots & \ddots & \vdots \\ D_{N1} & D_{N2} & \dots & D_{Nm} & \dots & D_{NN} \end{bmatrix} \quad (31)$$

$$G_k = \sum_m G_{km} + \sum_m \hat{G}_{km}. \quad (32)$$

For each port excitation, the the matrix $(\mathbf{G})$ must be recalculated, and the matrix $([\mathbf{E}] - [\mathbf{D}])$ only needs to be calculated and inverted once. The total calculation time is linearly proportional to the number of excitation ports.

B. CIM

Similar to the BEM, the boundary must be discretized into small segments to apply the CIM [13]. Assume that the contour C , including the inner and outer boundary of the plane, is discretized into L segments; the contour $\bar{C}$, a sum of all circular boundaries, including via nodes and antipad holes, is divided into M segments. Also, assume that there are P circular elements in total, and each circular element is discretized into K segments, namely $M = P \times K$.

First, an equation system can be established by using the Greens' identity of the second kind:

$$\sum_{j=1}^{L+M} u_{ij} \varphi_j = \sum_{j=1}^{L+M} h_{ij} I_j, \quad (i = 1, 2, \dots, L, \dots, L+M) \quad (33)$$

where

$$u_{ij} = \delta_{ij} - \frac{1}{\pi} \int_{W_j} \frac{\hat{\rho} \cdot \hat{n}'}{|\mathbf{r} - \mathbf{r}'|} ds \quad (34)$$

$$h_{ij} = \begin{cases} -\frac{1}{\kappa \pi d} \frac{1}{W_j} \int_{W_j} \ln |\mathbf{r} - \mathbf{r}'| ds, & (i \neq j) \\ -\frac{1}{\kappa \pi d} \left[\ln \left(\frac{W_i}{2} \right) - 1 \right], & (i = j) \end{cases} \quad (35)$$

where δ_{ij} is the Kronecker's delta, $\mathbf{r}$ is the location of the observation point i , $\mathbf{r}'$ is the location of the source segment j , $|\mathbf{r} - \mathbf{r}'|$ is the distance between the observation and source points, $\hat{\rho}$ is the normalized vector of $\mathbf{r} - \mathbf{r}'$, $\hat{n}'$ is the normal direction of the j th segment, κ is the electric conductivity, W_j is the width of the j th segment, and d denotes the metal thickness.

Equation (33) can be further organized into the following matrix form:

$$\begin{bmatrix} \bar{U}_{qq} & \bar{U}_{qp} \\ \bar{U}_{pq} & \bar{U}_{pp} \end{bmatrix} \begin{bmatrix} \bar{\Phi}_q \\ \bar{\Phi}_p \end{bmatrix} = \begin{bmatrix} \bar{H}_{qq} & \bar{H}_{qp} \\ \bar{H}_{pq} & \bar{H}_{pp} \end{bmatrix} \begin{bmatrix} \bar{I}_q \\ \bar{I}_p \end{bmatrix} \quad (36)$$

where q represents the index of the segments on the boundary C , and p denotes the index of the segments on the boundary $\bar{C}$. Note that the matrix $\bar{U}_{qq}$ is singular due to the undefined reference potential, and one row and column of one defined

reference potential needs to be removed from $\bar{U}_{qq}$.

Equation (36) can be organized to

$$\begin{bmatrix} \bar{\Phi}_q \\ \bar{\Phi}_p \end{bmatrix} = \begin{bmatrix} \bar{D}_{qq} & \bar{D}_{qp} \\ \bar{D}_{pq} & \bar{D}_{pp} \end{bmatrix} \begin{bmatrix} \bar{I}_q \\ \bar{I}_p \end{bmatrix} \quad (37)$$

where

$$\begin{bmatrix} \bar{D}_{qq} & \bar{D}_{qp} \\ \bar{D}_{pq} & \bar{D}_{pp} \end{bmatrix} = \begin{bmatrix} \bar{U}_{qq} & \bar{U}_{qp} \\ \bar{U}_{pq} & \bar{U}_{pp} \end{bmatrix}^{-1} \begin{bmatrix} \bar{H}_{qq} & \bar{H}_{qp} \\ \bar{H}_{pq} & \bar{H}_{pp} \end{bmatrix}. \quad (38)$$

Since no current flows on the plane boundary, namely $\bar{I}_q = 0$, so (38) can be reduced to

$$\Phi_p^- = \bar{D}_{pp}^- \bar{I}_p. \quad (39)$$

Assume the P circular elements include S via nodes and T antipad nodes. Since no dc current flows through the antipads, (39) can be further reduced to

$$\Phi_s^- = \bar{D}_{ss}^- \bar{I}_s. \quad (40)$$

By merging the segments on the same via node, a reduced equation system with the size of S as the number of nodes can be obtained

$$\bar{I}_{\text{node}} = \bar{G}_{\text{node}}^- \Phi_{\text{node}}^-. \quad (41)$$

Further, the branch resistor between two nodes i and j can be calculated as

$$r_{ij} = \begin{cases} -1/G_{ij}, & i \neq j \\ 1/\sum_{j=1}^N G_{ij}, & i = j, \end{cases} \quad (42)$$

where the coefficients G_{ij} correspond to the elements of the conductance matrix $\bar{G}_{\text{node}}$ in (41).

The branch resistors illustrated in Fig. 2 are used in the dc resistance network to calculate the total dc impedance of a PDN system.

ACKNOWLEDGMENTS

The authors would like to thank Dr. James Drewniak, Dr. Albert Ruehli, and Dr. Brice Achkir for their valuable discussions on this project. The authors would also like to thank Dr. Matthias Friedrich and Dr. Marco Leone for their help on the boundary element method through emails.

REFERENCES

- [1] J. Kim, L. Ren, and J. Fan, "Physics-based inductance extraction for via arrays in parallel planes for power distribution network design," *IEEE Trans. Microw. Theory Techn.*, vol. 58, no. 9, pp. 2434–2447, Sep. 2010.
- [2] J. Kim, K. Shringarpure, J. Fan, J. Kim, and J. L. Drewniak, "Equivalent circuit model for power bus design in multi-layer PCBs with via arrays," *IEEE Microw. Wireless Compon. Lett.*, vol. 21, no. 2, pp. 62–64, Feb. 2011.
- [3] K. Shringarpure *et al.*, "Formulation and network model reduction for analysis of the power distribution network in a production-level multilayered printed circuit board," *IEEE Trans. Electromagn. Compat.*, vol. 58, no. 3, pp. 849–858, Jun. 2016.
- [4] L. Wei *et al.*, "Plane-pair PEEC model for power distribution networks with sub-meshing techniques," *IEEE Trans. Microw. Theory Techn.*, vol. 64, no. 3, pp. 733–741, Mar. 2016.
- [5] X. C. Wei, E. P. Li, E. X. Liu, and R. Vahldieck, "Efficient simulation of power distribution network by using integral-equation and modal decoupling technology," *IEEE Trans. Microw. Theory Techn.*, vol. 56, no. 10, pp. 2277–2285, Oct. 2008.
- [6] X. Wei and E. Li, "Integral-equation equivalent-circuit method for modeling of noise coupling in multi-layered power distribution networks," *IEEE Trans. Microw. Theory Techn.*, vol. 58, no. 3, pp. 559–565, Mar. 2010.
- [7] Y. Zhang, G. Feng, and J. Fan, "A novel impedance definition of a parallel plate pair for an intrinsic via circuit model," *IEEE Trans. Microw. Theory Techn.*, vol. 58, no. 12, pp. 3780–3789, Dec. 2010.
- [8] M. Stumpf and M. Leone, "Efficient 2-D integral equation approach for the analysis of power bus structures with arbitrary shape," *IEEE Trans. Electromagn. Compat.*, vol. 51, no. 1, pp. 38–45, Feb. 2009.
- [9] H. Zhao, E. Liu, J. Hu, and E. Li, "Fast contour integral equation method for wideband power integrity analysis," *IEEE Trans. Compon. Packag. Manuf. Technol.*, vol. 4, no. 8, pp. 1317–1324, Aug. 2014.
- [10] M. Friedrich and M. Leone, "Boundary-element method for the calculation of port inductances in parallel-plane structures," *IEEE Trans. Electromagn. Compat.*, vol. 56, no. 6, pp. 1439–1447, Dec. 2014.
- [11] M. Swaminathan, D. Chung, S. Grivet-Talocia, K. Bharath, V. Laddha, and J. Xie, "Designing and modeling for power integrity," *IEEE Trans. Electromagn. Compat.*, vol. 52, no. 2, pp. 288–310, May 2010.
- [12] K. Shakeri and J. D. Meindl, "Compact physical IR-drop models for chip/package co-design of gigascale integration (GSI)," *IEEE Trans. Electron Devices*, vol. 52, no. 6, pp. 1087–1096, Jun. 2005.
- [13] X. Duan, H. Brüns, and C. Schuster, "Efficient DC analysis of power planes using contour integral method with circular elements," *IEEE Trans. Compon. Packag. Manuf. Technol.*, vol. 3, no. 8, pp. 1409–1419, Aug. 2013.
- [14] C.-W. Ho, A. Ruehli, and P. Brennan, "The modified nodal approach to network analysis," *IEEE Trans. Circuits Syst.*, vol. 22, no. 6, pp. 504–509, Jun. 1975.
- [15] CST Studio Suite. [Online]. Available: <https://www.cst.com>
- [16] Ansys HFSS. [Online]. Available: <https://www.ansys.com/products/electronics/ansys-hfss>
- [17] G. Zou, X. Wei, S. Yang, L. Ding, W. Ding, and Y. Yang, "An integral equation hybrid method for the impedance calculation of the grid power distribution network with an arbitrary shape," *IEEE Trans. Magn.*, vol. 55, no. 6, Jun. 2019, Art. no. 7203804, doi: [10.1109/TMAG.2019.2904099](https://doi.org/10.1109/TMAG.2019.2904099).
- [18] S. Yao, X.-C. Wei, and L. Ding, "Modeling of loaded nonuniform grid power distribution network with arbitrary shapes," *IEEE Trans. Compon. Packag. Manuf. Technol.*, vol. 11, no. 1, pp. 90–97, Jan. 2021, doi: [10.1109/TCPMT.2020.3041608](https://doi.org/10.1109/TCPMT.2020.3041608).
- [19] S. Liang, "A physics-based pi pre-layout tool for PCB PDN design," M.S. thesis, Missouri Univ. Sci. Technol., Rolla, MO, USA, 2021.
- [20] L. Zhang *et al.*, "Fast impedance prediction for power distribution network using deep learning," *Int. J. Numer. Model., Electron. Netw., Devices Fields*, vol. 35, no. 2, 2022, Art. no. e2956.



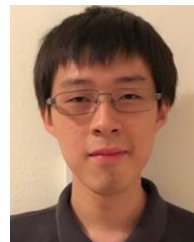
Ling Zhang (Member, IEEE) received the B.S.

degree in electrical engineering from the Huazhong University of Science and Technology, Wuhan, China, in June 2015, and the M.S. and Ph.D. degrees from the Missouri University of Science and Technology, Rolla, MO, USA, in December 2017 and January

2021, respectively.

From August 2016 to August 2017, he was with Cisco, San Jose, CA, USA, as a Student Intern. He is currently a Research Fellow with Zhejiang University, Hangzhou, China. His research interests include machine learning, power integrity, electromagnetic interference, radiofrequency interference, and signal integrity (SI).

Dr. Zhang was the recipient of the Best Paper Award in DesignCon 2019 and the Student Paper Finalist Award in ACES Symposium in 2021. He is an Organizing Committee Chair, Special Session Chair, Workshop Session Chair, and Poster Session Chair in APEMC.



Jack Juang (Student Member, IEEE) received the B.S. degree in electrical engineering, in 2020, from Missouri University of Science and Technology, Rolla, MO, USA, where he is currently working toward the M.S. degree in electrical engineering with EMC Laboratory.

He has been involved in projects relating to optimizing decoupling capacitor placement and RF susceptibility of smart devices. His research interests include power distribution network modeling and

optimization.

Zurab Kiguradze photograph and biography not available at the time of publication.



Bo Pu (Senior Member, IEEE) received the B.S. degree in electrical engineering from the Harbin Institute of Technology, Harbin, China, in 2009, and the Ph.D. degree in electronic and electrical engineering from Sungkyunkwan University, Seoul, South Korea, in 2015.

From 2015 to 2021, he was a Staff Engineer with Semiconductor Headquarter of Samsung Electronics, Hwaseong, South Korea. From 2020 to 2021, he was a Visiting Assistant Research Professor of NSF

I/UCRC for EMC with Missouri University of Science and Technology, Rolla, MO, USA. In 2021, he joined the Detool technology Company Ltd., as the Vice President. He holds ten patents about high-speed links and

2.5D/3D ICs. His research interest includes the design methodology of the EDA for chip-package-PCB systems.

Dr. Pu was the recipient of the Best Student Paper Award (2011 APEMC) and Best SIPI Symposium Paper Award (2021 IEEE EMC+SIPI) as first author, the Young Scientists Award from the URSI in 2014, the 2020 and 2021 Distinguish

Reviewer of the IEEE TRANSACTIONS ON ELECTROMAGNETIC COMPATIBILITY, best innovation awards as the first awardee in 2015–2019 from Samsung Electronics. He is a TPC Member and Session Chair in IEEE EMC+SIPI and APEMC. He is currently an Associate Editor for the IEEE ACCESS.



Shuai Jin (Member, IEEE) received the B.S. degree in biomedical engineering from the Huazhong University of Science and Technology, Wuhan, China, in 2011, and the M.S. and Ph.D. degrees in electrical engineering from the Missouri University of Science and Technology (formerly University of Missouri–Rolla), Rolla, MO, USA, in 2013 and 2017, respectively.

He is currently a Signal Integrity Engineer with GooglePlatform. His research interests include signal integrity in high-speed digital systems, power distribution network modeling, RF interference, and high-speed package modeling.

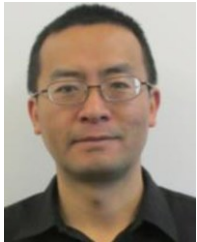


Songping Wu (Senior Member, IEEE) received the B.S. degree from Wuhan University, Wuhan, China, in 2003, the M.S. degree in electrical engineering from the Huazhong University of Science and Technology, Wuhan, China, in 2006, and the Ph.D. degree in electrical engineering from the Missouri University of Science and Technology, Rolla, MO, USA, in 2011.

He is currently an SI/PI/RF Desense Lead with the Google ChromeOS Team. Prior to joining Google, he was a Senior SI Engineer with Apple, Los Altos,

CA, USA, and a Hardware Engineer with Cisco, San Jose, CA, USA. He has authored or coauthored more than 50 research papers and holds six patents. His research results and patents have been applied to Google ChromeBooks, Apple iPhones, and Cisco UCS servers.

Dr. Wu was the recipient of the 2011 IEEE EMC Society President's Memorial Award. He is the Chair of the IEEE EMC Society TC-10 (Signal Integrity and Power Integrity).



Zhiping Yang (Fellow, IEEE) received the B.S. and M.S. degrees in electrical engineering from Tsinghua University, Beijing, China, in 1994 and 1997, respectively, and the Ph.D. degree in Electrical Engineering from the University of Missouri–Rolla, Rolla, MO, USA, in 2000.

From 2000 to 2005, he worked for Cisco Systems, San Jose, CA, USA, as a Technical Leader. From 2005 to 2006, he was with Apple Computer, Cupertino, CA, USA, as a Principal Engineer. From 2006 to 2012, he was in Nuova Systems (which was acquired by Cisco in 2008) and Cisco Systems, as a Principal Engineer. From 2012 to 2015, he was with Apple, as a Senior Manager. He is currently a Senior Hardware Manager with Google Consumer Hardware Group. He has authored or coauthored more than 40 research papers and 17 patents. His research and patents have been applied in Google Chromebook, Apple iPhone 5S/6/6S, Cisco UCS, Cisco Nexus 6K/4K/3K, and Cisco Cat6K products. His research interests include signal integrity and power integrity methodology development for die/package/board co-design, high-speed optical module, various high-speed cabling solutions, high-speed DRAM/storage technology, high-speed serial signaling technology, and RF interference.

Dr. Yang was the recipient of the 2016 IEEE EMCS Technical Achievement Award and was elevated to an IEEE Fellow in 2021.

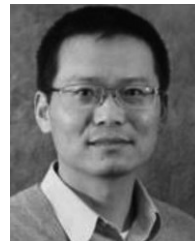


Er-Ping Li (Fellow, IEEE) received the Ph.D. degree in electrical engineering from Sheffield Hallam University, Sheffield, U.K., in 1992. He is currently a Qiushi Distinguished Professor with the Department of Information Science and Electronic Engineering, Zhejiang University, Hangzhou, China, Founding Dean of the Joint Institute of Zhejiang University–University of Illinois at Urbana-Champaign, Champaign, IL, USA. Since 1989, he has been a Research Associate/Fellow with Sheffield

Hallam University, Senior Research Fellow, Principal Research Engineer, Associate Professor, and the Technical Director with the Singapore Research Institute and Industry, Singapore. In 2000, he joined the Singapore A*STAR Research Institute of High Performance Computing, Singapore, as a Principal Scientist and the Director of the Electronic and Photonics Department. He has authored or coauthored more than 400 papers published in the referred international journals, and authored two books published by John-Wiley-IEEE

Press and Cambridge University Press. He holds and has filed a number of patents at the US patent office. His research interests include electrical modeling and design of micro/nanoscale integrated circuits, 3-D electronic package integration and nanoplasmic technology.

Dr. Li was the recipient of the IEEE EMC Technical Achievement Award, Richard Stoddard Award, and Laurence G. Cumming in 2006, 2015, and 2021, respectively.



Jun Fan (Fellow, IEEE) received the B.S. and M.S. degrees from Tsinghua University, Beijing, China, in 1994 and 1997, respectively, and the Ph.D. degree from Missouri S&T, Rolla, MO, USA, in 2000, all in electrical engineering.

From 2000 to 2007, he was a Consultant Engineer with NCR Corporation, San Diego, CA, USA. In July 2007, he joined Missouri S&T, where he was a Professor and the Director of the EMC Laboratory. He was also the Director of the National Science Foundation

Industry/University Cooperative Research Center for Electromagnetic Compatibility and a Senior Investigator with the Missouri S&T Material Research Center. He is currently an Adjunct Professor with Missouri S&T. His research interests include signal integrity and EMI design in high-speed digital systems, dc power-bus modeling, intrasystem EMI and RFI, PCB noise reduction, differential signaling, and cable/connector designs.

Dr. Fan was the recipient of the IEEE EMC Society Technical Achievement Award in August 2009. He is currently an Associate Editor for the IEEE TRANSACTIONS ON ELECTROMAGNETIC COMPATIBILITY and IEEE EMC Magazine.



Chulsoon Hwang (Senior Member, IEEE) received the B.S., M.S., and Ph.D. degrees in electrical

engineering from the Korea Advanced Institute of Science and Technology (KAIST), Daejeon, South Korea, in 2007, 2009, and 2012, respectively.

From 2012 to 2015, he was with Samsung Electronics, Suwon, South Korea, as a Senior Engineer. In July 2015, he joined Missouri University of Science and Technology (formerly University of Missouri-Rolla), Rolla, MO, USA, where he is currently an Assistant

Professor. His research interests include RF desense, signal/power integrity in high-speed digital systems, EMI/EMC, hardware security, and machine learning.

Dr. Hwang was the recipient of the AP-EMC Young Scientist Award, Google Faculty Research Award, and Missouri S&T's Faculty Research Award. He was also a co-recipient of the IEEE EMC Best Paper Award and the AP-EMC Best Paper Award, and a two-time co-recipient of the DesignCon Best Paper Award.