# Improved Current Shunt Characterization Method for Core Loss Measurement

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Abstract—With the increasing switching frequencies and power densities in modern power converters, magnetic core losses are becoming more essential for efficiency and thermal optimization. Traditionally, the two-winding method suffers from sensitivity to phaseerrorinpracticalmeasurements; this is mainly created by the unknown phase shift of a current-sensing resistor. Several methods have been developed to characterize the phase shift of a current

shuntresistor; however, the load effects of oscilloscopes are ignored. As a result, the corresponding phase shift can be significantly underestimated. This article proposes an improved method for phase shift extraction of a current shunt to solve the problem. The effectiveness of the shunt characterization method is experimentally verified up to 50 MHz. Benefits from the proposed method, the time-consuming component tuning process is not required for core loss measurement. A measurement verification at 10 MHz shows its validity. Finally, a current shunt implemented with a coaxial resistor array is designed with a phase shift of 0.05° at 10 MHz and a parasitic inductance as low as 42 pH.

*Index Terms*—Coaxial resistor, core loss, current-to-voltage impedance, two-port resistor.

#### I. INTRODUCTION

POWER converters with high efficiency and power density are increasingly pursued in modern consumer electronics. The switching frequency in a converter is then pushed to a higher range. However, a magnetic device, e.g., a transformer or an inductor, is one of the limiting factors in further improving power density. Therefore, accurate ferrite loss characterization is desired for optimizing power converters in terms of cost, form factor, and efficiency.

Various methods [1]–[8] have been developed for core loss measurement, and the dual-winding method [4]–[8] is the most widely used approach, as shown in Fig. 1. Although extra efforts are required to compensate for the mutual-winding loss [4], this method is regarded as the reference method for core loss

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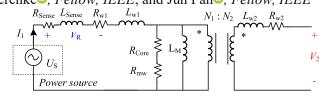


Fig. 1. Equivalent circuit for the dual-winding ferrite loss measurement setup.  $U_s$  is the winding excitation, and  $R_{w1}$ ,  $R_{w2}$ ,  $L_{w1}$ , and  $L_{w2}$  correspond to the series equivalent resistors (ESRs) and the leakage inductances of the winding wires.  $L_M$  is the magnetizing inductance,  $R_{mw}$  is the mutual-winding loss, and  $R_{Core}$  is the corresponding core loss. The winding turn ratio is defined as  $N_A \cdot N_C$ 

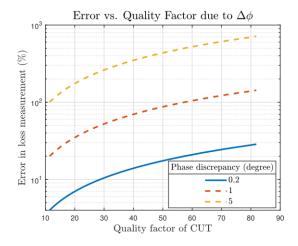


Fig. 2. Core loss measurement error due to phase discrepancy  $\Delta \varphi$ .

characterization due to its simplicity and accuracy. However, this method suffers from sensitivity to phase errors in current and voltage (I-V) measurements. The core loss error  $\Delta P$  caused by the phase discrepancy in I-V measurement  $\Delta \varphi$  for sinusoidal excitation is [9]

$$\Delta P = Q \cdot \Delta \varphi \tag{1}$$

where *Q* is the quality factor of the core-under-test (CUT).

A 1° phase error is enough to generate a 100% error in the practical core loss measurement, e.g., a core with Q of 60, as shown in Fig. 2. It is worth noting that the dominant sources of error are from the phase shift of the current sensor, which is created by the propagation delay of a current probe or the parasitic inductance of a sensing resistor.

Capacitive and inductive phase cancelation methods [5]–[7] have been proposed to overcome the drawbacks of the original

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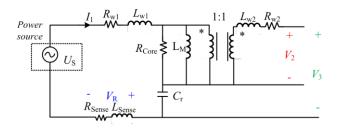


Fig. 3. Measurement setup with capacitance reactance cancelation in [5].  $C_r$  is the capacitor for reactance voltage cancelation and  $V_3$  is the voltage across the resonant tank.

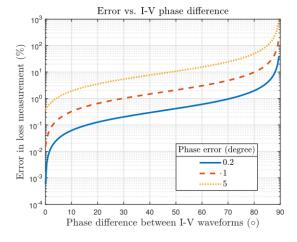


Fig. 4. Core loss measurement error due to phase discrepancy  $\Delta \varphi$  with the reactance cancelation.

two-winding method. The phase difference between the voltage and current waveforms can be reduced by introducing extra reactance cancelation components. The measurement becomes much less sensitive to the phase error [5], and the capacitive version is plotted in Fig. 3

$$\Delta P = \tan \varphi_{V-I} \cdot \Delta \varphi \tag{2}$$

where  $\varphi_{V-l}$  represents the phase difference between  $V_R$  and  $V_3$  after reactance cancelation. The errors due to phase discrepancies are demonstrated in Fig. 4.

Due to the unknown phase discrepancy in I–V measurements, perfect reactance cancelation is required [5]. However, perfect cancelation requires fine-tuning, and the characterization process is difficult to automate. We note that phase information is not required in the resonant Q approach from [3], but the method also suffers from the tedious resonant tuning process. An improved method is then proposed to avoid the tuning [7]. A cancelation factor is introduced to represent the effectiveness of the compensation, and thus, accurate core loss measurement can be achieved without fine-tuning the component value. Nevertheless, the compensation factor is obtained from perturbation testing, which is still not convenient enough for massive measurement.

The phase error cannot be eliminated due to the limitations in practical measurements [10], the efforts spent on components tuning can be greatly reduced if the phase discrepancy is controlled within subdegree level. Additionally, acceptable accuracy (e.g.,  $\Delta$  < 5%) can be achieved only with partial reactance cancelation. Probe characterization can be performed with a vector network analyzer (VNA) or a gain/phase analyzer [11]. Phase compensation can also be achieved with a highquality capacitor [12]. However, the main limitation to the abovementioned methods is the neglect of the possible nonlinearity of a current probe. Current probes are fabricated with magnetic cores, and the phase shift of a current probe can change when the excitation current is comparable with the rated value of the probe. Saturation due to dc bias can further increase the uncertainties in the phase shift. Core-less Rogowski coil is one of the solutions to avoid the saturation issue; nevertheless, the phase shift of a Rogowski coil can be influenced by the probing position [13]. The positional error is hard to eliminate in real applications.

Several core loss characterization methods have been developed based on resistors due to their simple electrical properties [5], [7], [14]. Resistive current sensors or shunts use Ohm's law for direct current-to-voltage conversion; however, the equivalent series inductance (ESL) of an ordinary two terminal resistor is typically in the nH range and can introduce tremendous error. The ESL of a resistor can be measured by an impedance analyzer [5], while the reproducibility of the ESL is extremely weak due to probe landing. The inconsistent contact between a resistor and a probe can either add or subtract series inductance to the device-undertest (DUT) [15]. Despite being a simple linear component, the resistor phase shift is almost unpredictable when it is installed on a board. Therefore, state-of-the-art current shunts are implemented with coax connectors [16], which greatly improve the reproducibility of probe-to-resistor connections.

The two-port measurement technique [17] is the reference method for low impedance measurement, and the transfer impedance, i.e.,  $Z_{21}$ , is used to define the current shunt impedance. However, such a definition is only valid when the input impedance of the detector is infinitely large. A large error is generated if the loading effect of an RF instrument is not considered, whose port impedance is typically 50  $\Omega$ . Therefore, the current-to-voltage impedance  $Z_{iv}$  of the current shunt cannot be represented by its transfer impedance  $Z_{21}$ .

Themainoriginal contribution of this article involves rigorous modeling, derivation, and experimental verification of the  $Z_{\rm iv}$  of a two-port resistor when it is connected to a 50  $\Omega$  detector. The proposed method can accelerate the measurement speed compared with existing methods. Itenables direct measurement, i.e., without reactance cancelation, for CUTs with moderate factors (<40) in the sub-MHzrange. In addition, the efforts spent on component tuning can be minimized for CUTs with high-Qfactors. The error can be controlled within 3% compared with the resonant method [5]. The rest of this article is organized as follows. The characterization method is discussed in Section II. MeasurementsareutilizedinSectionIIItoverifytheconsistency of the transfer functions under a high current input. In Section IV, the improved core loss measurement procedure and the associated results are demonstrated. Furthermore, an improved two-port resistor is demonstrated and verified in Section V. Finally, Section VI concludes this article.

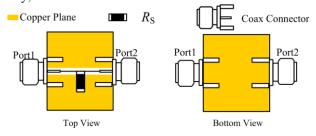


Fig. 5. Diagram of the proposed two-port resistor with SMA coaxial connectors.

## II. IMPLEMENTATION AND CHARACTERIZATION OF A TWO-PORT RESISTOR

# A. Design Considerations and Implementation of the Prototype

The structure of the proposed two-port resistor is demonstrated in Fig. 5, which consists of a shunted chip resistor (2010 thin film,  $1.2\Omega$ ), a 1-in transmission line and two coaxial connectors. Compared with existing current shunts with only one coaxial connector, the two-port design possesses two advantages. First, the resistor configuration remains the same for both impedance characterization and core loss measurement, which improves the impedance characterization fidelity. Second, the conventional two-port impedance measurement method can be applied and directly compared with the proposed method.

In the rest of the section, the current-to-voltage impedance  $Z_{iv}$  is defined to capture the loading effect of an RF instrument. Additionally, the reproducibility of  $Z_{iv}$  is discussed when the shunt is connected to real-time oscilloscopes (RTOs), whose port impedances are not exactly 50  $\Omega$ .

# B. Electrical Model of the Prototype and Its Characterization Method

The two-port resistor can be directly characterized by a VNA because coaxial connectors are used, as demonstrated in Fig. 6(a). In the measurement, port 1 is configured as the transmitter with an internal voltage source  $U_s$ , and port 2 is set as the receiver. The port impedance  $Z_0$  of both ports is 50  $\Omega$ . The calibration is performed on the end of connectors, which removes the influence of cables and adapters.  $Z_{iv}$  is defined as the ratio between the induced voltage  $V_{\rm OUT}$  across the 50  $\Omega$  load and the input current  $I_{\rm IN}$ , which is expressed as

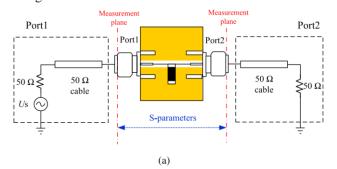
**V**OUT

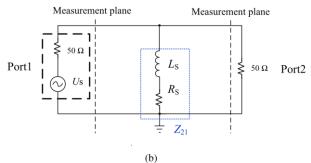
$$Z_{iv} = \underline{\qquad} (3)$$

1) Conventional Two-Port Impedance Characterization Method: The equivalent circuit of the conventional method is shown in Fig. 6(b). The current-to-voltage impedance  $Z_{iv}$  of the current shunt is approximated as the transfer impedance  $Z_{21}$ , which can be formulated as [17]

$$Z_{\rm iv} \approx Z_{21} = 25 \frac{S_{21}}{1 - S_{21}}$$
 (4)

2) Improved Current-to-Voltage Impedance Characterization Method: We note (4) is valid only if the loading effect of a





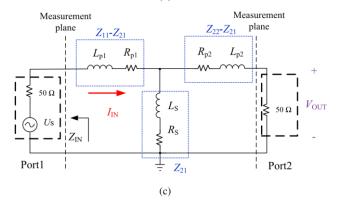


Fig. 6. (a) Measurement setup of the two-portresistor; (b) equivalent circuit of the conventional two-port impedance characterization method. Only the transfer impedance  $Z_{21}$  is extracted from the measurement, which consists of the ESR  $R_S$  and ESL  $L_S$  of the sensing resistor; (c) equivalent circuit for the improved resistor characterization method.  $L_{F1}$ ,  $R_{F1}$  and  $L_{F2}$ ,  $R_{F2}$  are the ESLs and ESRs of the test fixture.

 $50~\Omega$  port can be ignored. And thus, limits its accurate accuracy to sub-MHz range. To correctly model the current-to-voltage impedance  $Z_{iv}$  of the structure, both parasitic components of the

fixture and a 50  $\Omega$  load should be considered, as shown in Fig. 6(c). The *Z*-parameter matrix can be calculated according to the measured *S*-parameters obtained by a VNA [18]. Fig. 6(c) depicts the equivalent circuit represented by the *Z*-parameters.

In this circuit,  $\omega$  represents the source frequency. After the *Z*-parameters are obtained from the *S*-parameters, the input impedance  $Z_{\text{IN}}$  of the two-port circuits can be expressed as follows [18]:

$$Z_{\rm IN} = Z_{11} - \frac{Z_{21}^2}{Z_{22} + Z_0}. (5)$$

Then, the input current can be calculated accordingly

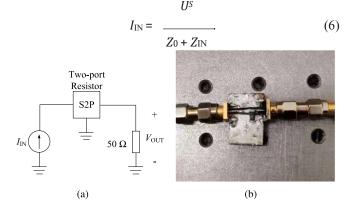


Fig. 7. (a) Simulation configuration for  $Z_{iv}$  extraction. (b) Photograph of the prototype.

The voltage  $V_{21}$  across the mutual impedance  $Z_{21}$  can then be formulated as

$$V_{21} = U_S - I_{IN}(Z_0 + Z_{11} - Z_{21}). \tag{7}$$

Theoutputvoltage  $V_{OUT}$  at the receiver with a 50  $\Omega$  impedance can be obtained as follows:

$$V_{\text{OUT}} = V_{21} \frac{Z_0}{Z_0 + Z_{22} - Z_{21}}. (8)$$

The  $Z_{iv}$  of the resistor can be calculated by substituting (6) and (8) into (4)

$$Z_{\rm iv} = \frac{Z_0 Z_{21}}{Z_0 + Z_{22}} = 50 \frac{Z_{21}}{50 + Z_{22}}.$$
 (9)

Similar to those of VNAs, the input impedances of highfrequency oscilloscopes can be set to  $50~\Omega$ , and  $Z_{\rm iv}$  remains almost the same as it is connected to the scope in the practical core loss measurement setup.

#### C. Prototype Implementation and Simulation Validation

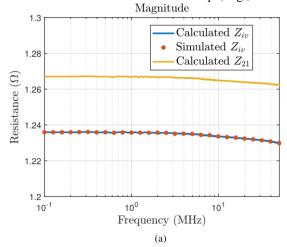
To verify the proposed impedance extraction method, a simulation model is implemented in advanced design system. The simulation setup is shown in Fig. 7(a). The first port is excited by an ac source  $I_{\rm IN}$ , and the second port is terminated with a 50  $\Omega$  resistor, which represents the input impedance of an oscilloscope. The "S2P" block represents the two-port S-

parameters of the prototype that are measured by a VNA (Model: Agilent E5071 C), which is illustrated in Fig. 7(b).

Fig. 8 compares the impedance magnitudes and phases with different definitions. The simulated and calculated  $Z_{\rm iv}$  values represent the results obtained from the simulation according to (9). The magnitudes and phases are well matched, which validates the  $Z_{\rm iv}$  calculation method. Additionally, a 2% discrepancy is observed in the magnitudes calculated for  $Z_{\rm iv}$  and  $Z_{21}$ . This disagreement is created by the loading effect of 50  $\Omega$ . More importantly, the 50  $\Omega$  load introduces a ~ 0.5° error in the phase at only 10 MHz. Significant errors are generated at higher frequencies.

# D. Error Due to the Nonideal Input Impedance of an Oscilloscope

The  $Z_{iv}$  of a two-port resistor can be accurately characterized by a VNA; however, the reproducibility of  $Z_{iv}$  is influenced by the nonideal characteristic of the oscilloscope, e.g., ADC



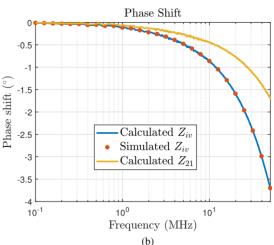


Fig. 8. Simulation verification of  $Z_{iv}$ . (a) Amplitude of  $Z_{iv}$  and  $Z_{21}$ . (b) Phase of  $Z_{iv}$  and  $Z_{21}$ .

TABLE I PORT IMPEDANCE MEASUREMENT SETUP

Equipment	Part No.	Bandwidth
VNA	E5071C	8.5 GHz
Coaxial cable	Teledyne Phase Master 190	26.5 GHz
Cal-kit	Maury Microwave 8050CK10	26.5 GHz
50 Ohm terminator	Rosenberger 32K15R-001E3	12.4 GHz
Oscilloscope	Tektronix DPO 70804	8 GHz
Oscilloscope	Agilent 81204B	12 GHz
Oscilloscope	R&S RTO1024	2 GHz

interleaving,theRFfront-endtransfercharacteristicandvertical rangesetting[19],[20].Onlytheinputportimpedances ofRTOs are discussed in the article. Errors related to other factors are also important for the performance, but they are not treated in this article and are considered as an additional measurement noise.

The port matches of three RTOs are measured with a VNA with one-port approach [21]. The port impedance versus the frequency is shown in Fig. 9, and the components used in the measurement are listed in Table I.

It is clear that the port impedances of oscilloscopes are not exactly 50  $\Omega$  and exhibit stronger frequency dependency compared with the passive terminator. The nonideal port match will introduce extra error into the measurement. To further

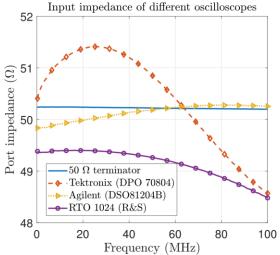


Fig. 9. Port impedance versus frequency for different oscilloscopes (vertical resolution: 100 mV/div). Besides, the impedance of a passive  $50 \Omega$  terminator is shown as the reference.

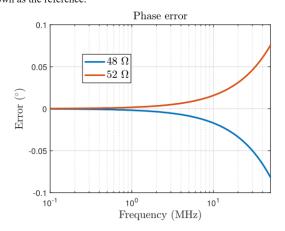
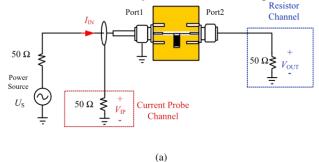


Fig. 10. Phase error induced with different load impedances. The case with a 50  $\Omega$  load is used as the reference.

examine the errors introduced by the input impedance of an oscilloscope,  $Z_{iv}$  of the resistor prototype is evaluated with 48  $\Omega$  and  $50\Omega$  resistiveloads according to (9). Due to the small resistor impedance, i.e.,  $1.2~\Omega$ , the errors are less than  $10~m\Omega$  in terms of magnitude. The errors in phase in comparison with those of the  $50~\Omega$  load case are illustrated in Fig. 10. As observed from the calculation, the error increases with frequency but is limited to  $0.1^{\circ}$  at 50~MHz. However, it should be errors at hundreds of MHz, which is the main limitation of the proposed characterization method for a two-port resistor.

#### III. EXPERIMENTAL VALIDATION FOR THE PROPOSED $Z_{\rm IV}$

In this section, the measurement validation of the proposed  $Z_{iv}$  is demonstrated. We note that the main source of error in the proposed method is the consistency of  $Z_{iv}$  when the resistor is connected to different instruments. To further validate the reproducibility of the proposed resistor characterization method, a current probe is used as a reference, as its transfer impedance  $Z_{ct}$  can also be characterized by a VNA. It should be emphasized



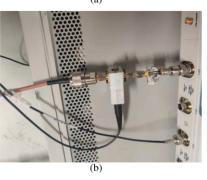


Fig. 11. (a) Diagram of the measurement setup with an oscilloscope for the current probe and resistor comparison. (b) High-power measurement setup for transfer impedance validation.

that the excitation is configured as 1/30 of the rated value of the current probe, and the probe can be treated as a linear component under such a low-level excitation. The small-signal transfer impedance  $Z_{\rm ct}$  of a current probe is well defined and can be characterized according to [22]

$$Z_{\rm ct} = 50 \cdot S_{21}$$
. (10)

#### A. Measurement Validation With a Current Probe

TheexperimentalconfigurationisdepictedinFig.11.Itconsistsofa high-power source, i.e., a signal generator (Agilent N5181 A) and a power amplifier (Amplifier research 100W1000). The power source is terminated by the resistor prototype, and the output port of the prototype is connected to an oscilloscope (R&S RTO1024, 10 GS/s with a 2 GHz bandwidth). A current probe (Tektronix CT-2 with a P6041 probe cable) is inserted between the power sourceandtheresistorforcomparison. Theinputcurrentissetto approximately 0.12 A (peak value). According to the datasheet, thecurrentprobecanmeasurecontinuouscurrentupto4A(peak value) without saturation [23].

 $V_{\rm IP}$  and  $V_{\rm OUT}$  are the outputs of the current probe and the twoport resistor, respectively. To compare the characterization results measured by the VNA and scope, the current ratio  $R_{\rm Scope}$ is defined, which can be expressed as follows:

$$R_{\text{Scope}} = \frac{V_{\text{IP}}(\omega)}{I_{\text{IN}}Z_{\text{ivScope}}}$$

$$V_{\text{OUT}}(\omega) \qquad I_{\text{IN}}Z_{\text{ivScope}}$$

$$= \frac{Z_{\text{ctScope}}}{Z_{\text{ivScope}}}$$
(11)

The time-domain waveforms are transformed into the frequency domain by the FFT. The ratio describes the difference

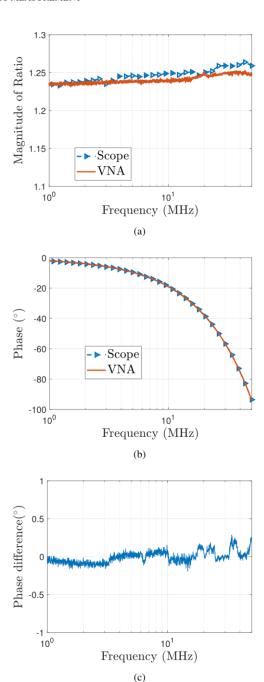


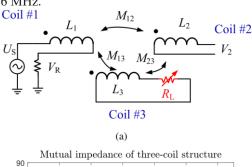
Fig. 12. Comparison of the measured  $R_{\text{Scope}}$  and  $R_{\text{VNA}}$ . (a) Magnitude. (b) Phase. (c) Phase difference.

between the current-to-voltage impedances of the current probe and the two-port resistor. A ratio  $R_{\rm VNA}$  can be calculated according to (9) and (10), which can be measured by a VNA

$$R_{\text{VNA}} = \frac{Z_{\text{ct}}}{Z_{\text{iv}}}$$
 (12)

2) Comparison of the Results: Fig. 12 compares the ratios measured by an oscilloscope and a VNA. The discrepancy in magnitude is 1.5% at most (up to 50 MHz). Additionally, the phase shift differences are smaller than 0.4° among the

frequencies of interest. In particular, the error is limited to 0.1° below 16 MHz.



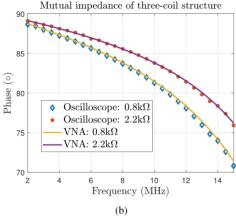


Fig. 13. (a) Equivalent circuit of the three-coil system. The mutual impedance  $Z_{21}$  between coils #1 and #2 can be configured by the load resistance  $R_L$  in coil#3. (b) Comparison of measured mutual impedance  $Z_{21}$ .

### IV. MEASUREMENT CONFIGURATION AND EXPERIMENTAL VALIDATION

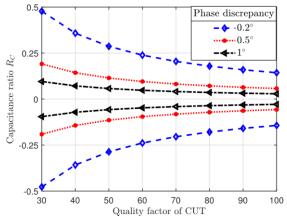
#### A. Considerations in Practical Measurement

1) Phase Discrepancy in I–V Measurements: In addition to thephaseshiftoftheresistor, the propagation delay of the voltage probe is also required in real applications. The voltage induced acrossthesecondarywindingismeasuredbyadifferentialprobe (Tektronix P6251 and Tekprobe power supply 1103). We note that the probe is characterized by a VNA according to [24].

To further evaluate the phase measurement accuracy of the whole system, considering both voltage and current sensors, a three-coil system with an air core is used [25]. The air-core coils provide a linear and controllable mutual impedance that can be measured by different instruments. The circuit configuration and the results comparison are shown in Fig. 13.

Fig. 13(b) compares the phases of  $Z_M$  measured by a VNA and an oscilloscope system. The error measured by the two instruments is limited to 0.2° below 10 MHz, and the maximum value is no more than 0.3° below 15 MHz. We note that the phase resolution of state-of-the-art instruments, e.g., VNAs, can achieve dozens of millidegrees or even better [26], [27]. The extra errors [10] are introduced by the uncertainties of cable connection, calibration process, system noise, etc.

Even though the phase discrepancy cannot be completely removed through characterization, accurate core loss measurement is still achievable. In real practice, direct core loss measurement can be performed below the MHz range and for CUTs with moderate Q-factors (< 40). Besides, the residual error can



5% error boundaries with different phase discrepancies.

be further reduced with proper reactance cancelation, as the discrepancyinI-Vmeasurementscanbelimited to the subdegree level. Therefore, the proposed method offers a higher test speed over the existing methods Fig. 4 shows that the power error is only 5% for a 1° phase discrepancy in the I-V measurement when the phase angle  $\varphi_{V-I}$  is  $\sim 65^{\circ}$ .

2) Selection of the Reactance Cancelation Capacitor: In this article, only the capacitive cancelation method is discussed and demonstrated, whose setup is demonstrated in Fig. 3.

When the turn ratio of the DUT is configured as 1:1 and the leakage inductance can be ignored; the resonant capacitance  $C_0$ can be calculated as

$$C_r = \frac{1}{\omega L_M} \tag{13}$$

where  $L_M$  is the magnetizing inductance of the DUT. The phase angle  $\varphi_{V-1}$  between  $V_3$  and  $V_R$  can be represented by [5]

$$\varphi_{V-I} = \arctan((1 - C_0/C_r) \cdot Q). \tag{14}$$

The core loss measurement error  $\Delta P$  can be formulated by substituting (14) into (2)

$$\Delta P = (1 - C_0/C_r) \cdot Q \cdot \Delta \varphi. \tag{15}$$

Correspondingly, the ratio 
$$R_C$$
 is defined as 
$$R_C = 1 - \frac{C_r}{C_0} = \frac{\Delta P}{Q\Delta\phi} \tag{16}$$

The ratio can be a positive or a negative value, as the phase difference between I-V can also be positive or negative. If we assume the acceptable error is ±5%, the upper and lower limits of the ratios are plotted in Fig. 14. As an example,  $\sim 12\%$  variance in capacitance can be tolerated when the phase discrepancy is 1° and the Q factor of the CUT is 100. Silver mica capacitors or RF porcelain capacitors should be used to minimize the error due to the ESR of the cancelation capacitor [3].

#### B. Measurement Setup and Calculation Flow

The system consists of an RF power amplifier source and a dual-winding transformer. We note that the input impedance of the oscilloscope should be set to  $50~\Omega$ . Similar to the

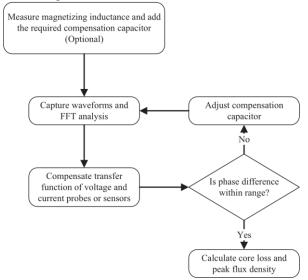


Fig. 15. Calculation flow for current-sensing compensation and core loss measurement.

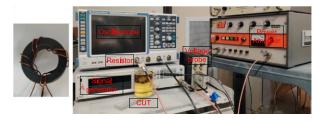


Fig. 16. CUT (Fair-Rite 61) and measurement setup for the magnetic core.

conventional setup, a high impedance voltage probe should be applied for voltage measurement.

Capacitive cancelation is suggested for CUTs with Q-factors higher than 40, and the required resonance capacitance can be calculated by the measured inductance of the secondary winding. Due to the frequency-dependent phase shifts of both voltage and current sensors, frequency-domain analysis and compensation are preferred. Therefore, a fast Fourier transform (FFT) is applied to the measured time-domain voltage and current waveforms. In the practical measurement, a stringent criterion is suggested, which considers the phase error is  $1^{\circ}$  below 15 MHz, and the  $\varphi v$ -t should be controlled within  $\pm 70^{\circ}$ 

after compensation. The calculation process for flux density was

welldiscussedin[28],andthecalculationandmeasurementflow are demonstrated in Fig. 15.

#### C. Experimental Validation With Magnetic Cores

Experiments are performed to demonstrate the benefits created by accurate probe characterization. Two different cores from TDK (R41.8/26.2/12.5-N97) and Fair-Rite (T36/23/13-61) are characterized separately. In addition, the CUTs are immersed in an oil bath, and the temperature is kept reasonably at an ambient level. The configuration of the measurement setup is depicted in Fig. 16.

1) TDKN97: Directmeasurementresults,i.e.,withoutphase cancelationcapacitors,arecompared with those measured by the Loss of TDK N97, 700 kHz

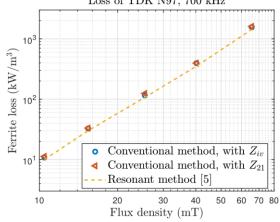


Fig.17. Corelosscomparisonbetweentheproposedmethodandthereference method in [5].

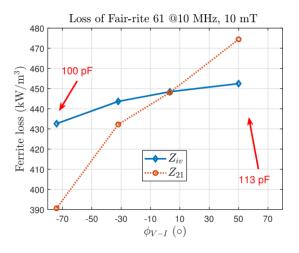


Fig. 18.sponding capacitors are marked in the figure. Core loss measurement results under different  $\varphi_{V}$ -I. The corre-

resonant method in [5], as shown in Fig. 17. In this test case, the

errorduetothedifferentcharacterizationmethodsforthecurrent shuntissmallerthan3%. Inaddition, the resultsmeasured by the proposed method match those measured by the resonant method ( $\Delta$  < 5%). We note that porcelain capacitors (ATC 100 series) areusedtoavoiderrorduetotheESRsoftheresonantcapacitors. 2) Fair-Rite 61: Another comparison is performed at 10 MHz and a 10 mT peak flux density. The CUT samples are madewith4turnsofAWG24copperwires,whichhaveamagnetizin g inductance of 2.44  $\mu$ H. The calculated resonant capacitor is 104 pF at the excitation frequency. Benefiting from the proposed method, perfect reactance cancelation is not required. The measured core losses with different  $\varphi_{V-I}$  are shown in Fig. 18. Compared with the test case with almost perfect resonance, the error created by the nonresonant operation  $(\varphi_{V-I} \approx -74^{\circ})$  is smaller than 3.5%. We note the error is more than 12% if the phase shift is characterized by the conventional  $Z_{21}$  method. In addition, ~15% capacitance variation can be tolerated to limit the error to 5%. The proposed method can effectively improve the accuracy in nonresonant operation conditions and thereby increase the testing speed.

In this article, we focus on eliminating the phase discrepancies among probes. The measurement errors introduced by the temperature, mutual-windingloss, and parasitic capacitances are not within the scope of our study.

#### V. TWO-PORT RESISTOR WITH A COAXIAL RESISTOR ARRAY

The phase shift induced by a two-port resistor has been discussed and validated by the measurements. However, a resistor with a quasi-zero phase shift is still desired to eliminate the characterization and compensation processes. It can also facilitate current measurements for different applications, e.g., in situ loss of an inductor. In this section, the considerations for resistor design are discussed, and the 1  $\Omega$  prototype with a phase shift of  $0.05^{\circ}$  at 10 MHz is demonstrated.

### A. Design Considerations of a Two-Port Coaxial Resistor

1) Parasitic Inductance: According to (9), the phase shift canbeeffectively reduced by eliminating the ESL of the resistor. Coaxial resistor placement is then adopted in the design, which has been used in various current-sensing applications in the RF range [16], [29], [30]. As an add-on advantage, the energy capacity of the resistor can be improved by reducing its ESL [16].

As shown in Fig. 19, surface-mounted resistors are soldered on the top layer of the PCB board. The current flows from the inner conductor of the SMA connector on the top side through the bottom plane of the printed circuit board. The SMA connector at the bottom is pin-to-pin connected to the connector at the top side, and the voltage generated across the resistor array can be directly measured at the port. Due to the 50  $\Omega$  load of the second port, the majority of the current returns to the connector shell through vias, resistors, and the copper plane on

the top layer. In addition to the coaxial placement, another critical parameter in the design is the height difference  $H_D$  between the signal and return planes. The top two layers of a four-layer PCB are used, as  $H_D$  can be configured to 0.1 mm in practical PCB fabrication scenarios.

2) Power Rate and Resistor Selection: The resistor is designed to handle at least 1 Amp of continuous current (RMS value) or 1 W of power; in addition, the uncertainty created by the change in temperature is limited within 0.5%. Such requirements can be fulfilled with commercially available thick film resistors (temperature coefficient: 200 ppm/° C). The temperatureriseshouldthenbecontrolledwithin20° C,considerin g the resistance change in the resistors, PCB and SMA connectors. Correspondingly, the total rated power of the resistor is designed as 4 W according to the temperature rise curve in the datasheet [31].

### B. Resistor Simulation and Measurement Validation

To validate the proposed structure, a prototype is illustrated in Fig. 20. It is built with 20 parallel surface-mounted resistors (resistance:  $22 \Omega$ , package: 0805, rated power: 0.25 W), and two surface-mounted and soldered SMA connectors are used (model: Molex 0732511350). The dimensions of the prototype are presented in Table II.

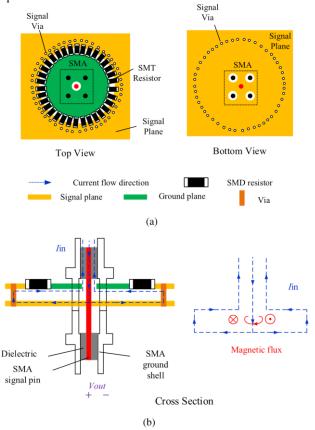


Fig. 19. (a) Top and bottom views of the proposed resistor. (b) Cross section of the proposed resistor and its current flow direction.

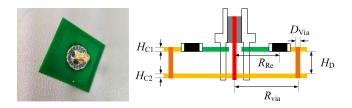
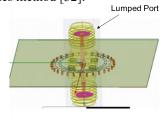


Fig. 20. Photograph of the two-port resistor and its labeled dimensions.

TABLE II
PHYSICAL DIMENSIONS OF THE IMPROVED TWO-PORT RESISTOR

Symbol	Description	Value
$D_{Via}$	Shorting via diameter	0.2 mm
$R_{Via}$	Via circular pattern radius	7.4 mm
$R_{Re}$	SMT resistor circular pattern radius	6.1 mm
$H_{C1}$	Top-layer copper foil thickness	1 oz
$H_{C2}$	Bottom-layer copper foil thickness	0.5 oz
$H_D$	Dielectric between copper layers thickness	0.1 mm

In addition to measurement, a simulation model is also implemented in a full-wave electromagnetic field simulator (Ansys HFSS), which is demonstrated in Fig. 21. In the simulation, the current is injected through lumped ports across the inner conductor and the outer shell of the SMA connector. Resistors are represented by lumped elements with 1.5 nH of series inductance, as measured by a VNA with the two-port series method [32].



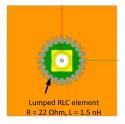


Fig. 21. Full-wave simulation model and its settings.

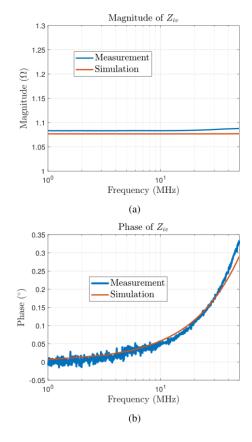


Fig. 22. Comparison of the simulated and measured transfer impedance prototypes. (a) Magnitude. (b) Phase.

As shown in Fig. 22, the simulated and measured magnitudes agree well with an approximately 1% difference. Furthermore, the phase shifts also have a strong correlation, where the maximum discrepancy is less than  $0.1^{\circ}$  below 50 MHz. Additionally, the phase shift of the coaxial prototype is within  $0.05^{\circ}$  below 10 MHz; this can be treated as an ideal resistor below the frequency range.

To validate the power handling rate of the prototype. The temperature rise of the prototype under 1 Amp (RMS value, at 10 MHz) of ac current excitation is tested by an infrared camera (Flir E8), as shown in Fig. 23. The ambient temperature is 26  $^{\circ}$  C and the temperature rise is  $\sim\!17\,^{\circ}$  C, which fulfills the design requirement.

### C. Influence of H<sub>D</sub>

As we have explained, the most critical parameter in the resistor design is the height difference between the top and

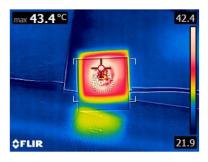


Fig. 23. Temperature monitoring of the current shunt.

# TABLE III EXTRACTED PARASITIC INDUCTANCE VERSUS $H_D$

$H_D$ (mm)	Inductance (pH)	
0.1	38	
0.3	84	
0.5	121	

TABLE IV ESLS OF DIFFERENT COMMERCIAL CURRENT SHUNTS

Product	T&M [29]	Keysight [16]	ESDEMC [30]
Resistance $(\Omega)$	0.1	0.1	2
ESL (nH)	$2.2^{1}$	0.12	N/A
Bandwidth (GHz)	2	2.2	4

<sup>1</sup>The test fixture and measurement results are demonstrated in [33].

bottom planes. The simulation model of the proposed resistor is verified by the above-mentioned measurement process and can be used to investigate the influence of  $H_D$ . The value of  $H_D$  is swept in the simulation, and the parasitic inductances extracted at 10 MHz according to (4) are demonstrated in Table III. It is worth noting that the inductance of our prototype is ~40 pH according to (4), which is 3 times smaller than that of an existing design [16].  $H_D$  is configured as approximately 1 mm, which

results inhundreds of pH parasitic inductances. As thereference, the ESLs of several state-of-the-art coaxial shunts are listed in Table IV.

#### VI. CONCLUSION

This article rigorously illustrates the loading effects of the 50  $\Omega$  detector on the well-known two-port impedance extraction method. Furthermore, an improved method is demonstrated to correctly calculate the current-to-voltage impedance of a two-port resistor. The proposed method is experimentally verified up to 50 MHz with errors limited to  $0.3^{\circ}$ . The partial cancelation concept can be adopted to overcome residual phase error. Accurate core loss measurement can be achieved without finetuning for the compensation component and, thus, accelerates the testing speed.

The design of an improved current shunt with a coaxial resistor array is also exemplified. The parasitic inductance of the prototype presented in this article is 3 times smaller than that of

the state-of-the-art design. As a benchmark, a 3-D simulation model is developed to verify the measurement results. In addition, the main limiting factor in the existing current shunt designs is shown through simulation.

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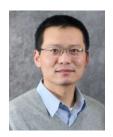
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