Determining the Peak Voltage during TVS switching at the I/O of an IC using Component Measurement Data

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Abstract – A method for calculating the peak voltage at the input of the IC is presented for an I/O port subsystem consisting of a TVS protection device, an IC on-chip protection and a PCB trace. The method is valid for non-snapback on-chip protection where the silicon part can be fully described by a quasistatic (VF)-TLP curve and allows to determine the peak voltage from measurement data of the individual components only.

I. Introduction

To effectively protect an Integrated Circuit (IC) in an application from ESD events coming from a PCB I/O port discrete TVS protection devices are regularly placed on the board to shunt the majority of the current to ground. In addition to the risk of overcurrent there is also the risk that transient overshoot voltages can damage sensitive gate oxides of the IC input [1],[2]. Here, the peak voltage which can occur at the I/O of the IC is of paramount importance. ICs are often processed in advanced IC technologies with small structure sizes and high doping levels which cause their on-chip ESD protections to turn on nearly instantaneously with little or no transient voltage overshoot. For high speed interface applications TVS devices need to balance the requirements of low capacitances and high ESD robustness to maintain signal integrity and offer a high system level protection. For this reason, the TVS devices typically include a low-doped well which, unfortunately, makes switching to the on-state slower. Thus, TVS devices typically possess a notable transient voltage overshoot [3]-[5]. In comparison to an on-chip ESD protection, their turn-on time is long.

To model a PCB I/O port sub-system consisting of a TVS protection device, an IC ESD protection and a PCB trace in between, the System-Efficient ESD Design (SEED) [6] methodology is used. To estimate overshoot voltages at the input of the IC, transient models of the devices used in the I/O port sub-system are required. If these models do not exist, an evaluation of the peak voltage occurring at the IC is tedious.

This work describes a method which allows one to estimate the transient peak voltage for (very fast) transmission line pulses ((VF)-TLP) when no SEED models are available by using only measured data from the individual components. The method is valid for a special but common case. The requirement is that the on-chip ESD protection switch on much faster than the external protection, e.g. when using a non-snapback device which can fully be described with a quasistatic TLP curve, i.e. that the voltage drop over the device is only a function of the current flowing through it and there is no or very little transient voltage overshoot during switching of the on-chip protection. A prominent example is a forward biased diode with high silicon doping levels. However, other IC protections such as RC triggered active MOSFET circuits can be described in this way as well [7],[8]. In principle, the method should also allow a certain small snapback at low currents under the condition that the IC protection is turning on much faster than the external TVS device. The latter can be a snapback device with transient voltage overshoot as used in this paper.

The paper is organized as follows: Section II describes the method. Section III describes measurement which are compared with the results from the model.

II. Method

Figure 1 shows a schematical picture of a transient current into the IC of an I/O interface shown in Figure 2(a) when current starts to be diverted away from the IC into the TVS protection device. Evidently, in steady

state the change of current with time is zero and there is no voltage drop over inductive elements. However, there is another time when $\frac{dI_{IC}}{dt} = 0$, which is when the maximum current is reached. At this point the voltage drop at any inductance in the path towards the IC is also zero. This point is of special interest because at this time the maximum voltage drop at the I/O of the IC is reached if the voltage is a monotonous function of current. This is valid if the voltage of the on-chip protection can be described by a given onset voltage V_0 and a resistive behavior where both parameters are assumed to be time independent. The voltage at the I/O of the IC is only dependent on the current flowing through it and can be described by:

$$V_{I/O} = V_0 + R_{IC} \cdot I_{IC} \quad (1)$$

Figure 2 (a) shows a schematical picture of the I/O Port sub-system. The total current I_t is divided into the current I_{IC} into the on-chip protection via the inductive PCB trace and current I_{TVS} into the TVS protection device. The on-chip protection device is described by a diode with onset voltage V_0 and a resistor which also holds for an active clamp. The on-chip device also may have a parasitic inductance L_{IC} due to its internal metal lines. For the calculation, this inductance is added to the PCB inductance L_{PCB}. The TVS device is modelled as a time dependent resistor $V_{TVS} = R_{TVS}(t) \cdot I_{TVS}$. A voltage drop due to a parasitic inductance L_{TVS} is added to the resistance term, which is possible due to its time dependent nature.

If no current flows through the TVS device, i.e. it has not triggered the determination of the maximum voltage at the I/O is trivial and is given simply by its quasi-static voltage $V_{I/O}^{qs} = V_0 + R_{IC} \cdot I_t^{qs}$, with I_t^{qs} the maximum quasi-static current. To calculate the current I_t means it is necessary to estimate the current when the TVS device turns on.

The quasistatic turn-on current of the TVS device in the application can be estimated by using

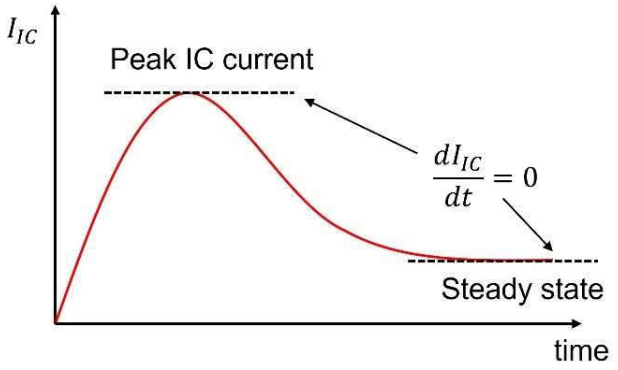

Figure 1: Schematical representation of transient current into an IC.

$$I_t = \frac{V_{tr} - V_0}{R_{IC}} + I_{tr}$$

where V_{tr} and I_{tr} are the trigger voltage and current of the TVS protection device. Once the TVS device triggers the situation changes and the determination of the peak voltage at the I/O is more complicated.

Figure 2 (b) shows the situation when the peak current is reached ($\frac{dI_{IC}(t_p)}{dt} = 0$) at time t_p. As there is no voltage drop across the inductive elements in the IC path they can be omitted and $V_{TVS}(t_p) = V_{I/O}(t_p)$. This is essentially the same situation as for the steady state but with a different resistance $R_{TVS}(t_p)$. Thus, the relation between I_{IC} and total current I_t for the circuit in Figure 2(b) is straightforward and given by

$$I_{IC}(t_p) = \frac{R_{TVS}(t_p) \cdot I_t(t_p) - V_0}{R_{IC} + R_{TVS}(t_p)} \quad (2)$$

The aim of the following calculation is to find the time t_p so that $R_{TVS}(t_p)$ and $I_t(t_p)$ and subsequently $I_{IC}(t_p)$ can be determined. The maximum voltage drop at the I/O is then calculated by using equation (1).

The total voltage drop along the IC path i.e. the sum of the voltage drop of the inductances and of the IC, is equal to the voltage drop V_{TVS} at the TVS device:

$$(L_{PCB} + L_{IC}) \cdot \frac{dI_{IC}}{dt} + V_0 + R_{IC} \cdot I_{IC} = R_{TVS}(t) \cdot I_{TVS} = V_{TVS} \quad (3)$$

Equation (3) is differentiated with respect to time and evaluated at time t_p:

$$(L_{PCB} + L_{IC}) \cdot \ddot{I}_{IC} = \dot{R}_{TVS} \cdot I_{TVS} + R_{TVS} \cdot \dot{I}_{TVS} \quad (4)$$

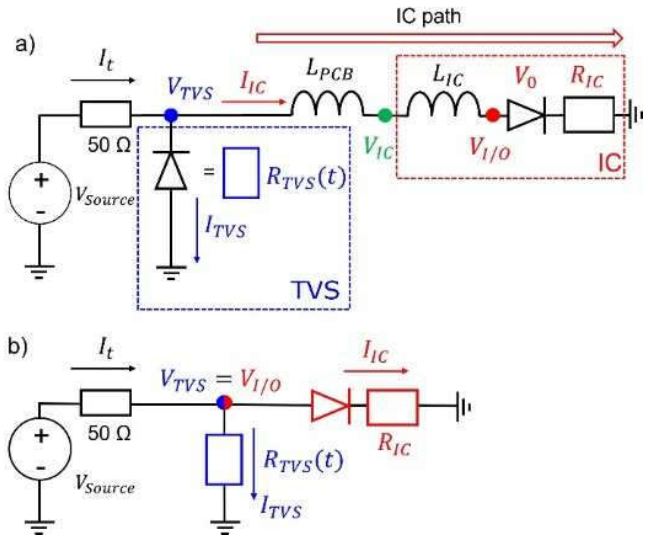

Figure 2: a) Schematical picture of I/O interface. b) effective interface when $\frac{dI_{IC}}{dt} = 0$.

where the number of dots above the symbols represent the order of the derivative in time. $\ddot{I}_{IC}$ can be derived by differentiating Eq. (2) twice with respect to time. The calculation is straightforward but tedious and because of its length the result will not be shown here. By using the relation $I_{TVS} = I_t - I_{IC}$, Eq. (2) and $\dot{I}_{TVS}(t_p) = \dot{I}_t(t_p)$, Eq. (4) becomes at time t_p:

$$(L_{PCB} + L_{IC}) \cdot \frac{d^2}{dt}\left(\frac{R_{TVS}(t)\cdot I_t(t) - V_0}{R_{IC} + R_{TVS}(t)}\right)\Big|_{tp} = \dot{R}_{TVS}(t_p) \cdot \left(I_t(t_p) - \frac{R_{TVS}(t_p)\cdot I_t(t_p) - V_0}{R_{IC} + R_{TVS}(t_p)}\right) + R_{TVS}(t_p) \cdot \dot{I}_t(t_p) \quad (5)$$

Eq. (5) is solved graphically to obtain $R_{TVS}(t_p)$ and $I_t(t_p)$. Please note that the equation is not valid for other times.

From individual measurements, the total current $I_t(t)$, the characteristics of the TVS device, i.e. $R_{TVS}(t)$ and the on-chip ESD protection (see Eq.1) Need to be known. $R_{TVS}(t)$ is measured on a TVS device alone.

The noise on measurement curves can easily mask the true value when calculating the derivative. It is thus advised to fit the VF-TLP current pulse and $R_{TVS}(t)$ by functions. Only the rising edge and the constant part of the VF-TLP current needs to be fitted. For the VF-TLP currents a sum of $atan(t)$ functions yields a very good fit. For the resistance of the TVS mainly the time dependence starting at its peak voltage overshoot is important. Here the following fit function [9]

$$R_{TVS}(t) = \frac{R_0}{1 + \left(c \cdot \int_0^t I_{TVS}(t)dt\right)^d} + R_{qs}$$

is used with R_0, R_{qs} and c and d being fit parameters. Other fit functions can be used because the main objective is to eliminate the measurement noise. The measurement set up can cause that the transient current and voltage measurement are slightly shifted in time to each other which adds a systematic error to the calculation of $R_{TVS}(t)$. To determine the time shift a measurement of an inductance has been performed with the VF-TLP equipment. The noise of the current was reduced by averaging over several measurement points and then the numerical time derivative dI/dt was done. The time of the peak value was compared with the one of the peak voltage. In our set up the time shift between voltage and current was 0.07 ns which was taken into account for the calculation of $R_{TVS}(t)$. Figure 3 shows fitting examples of the current and the TVS device for a VF-TLP current of 10A. An excellent match for both $R_{TVS}(t)$ and $I_t(t)$ can be achieved. It is known that the resistance is dependent on the current flowing through the device.

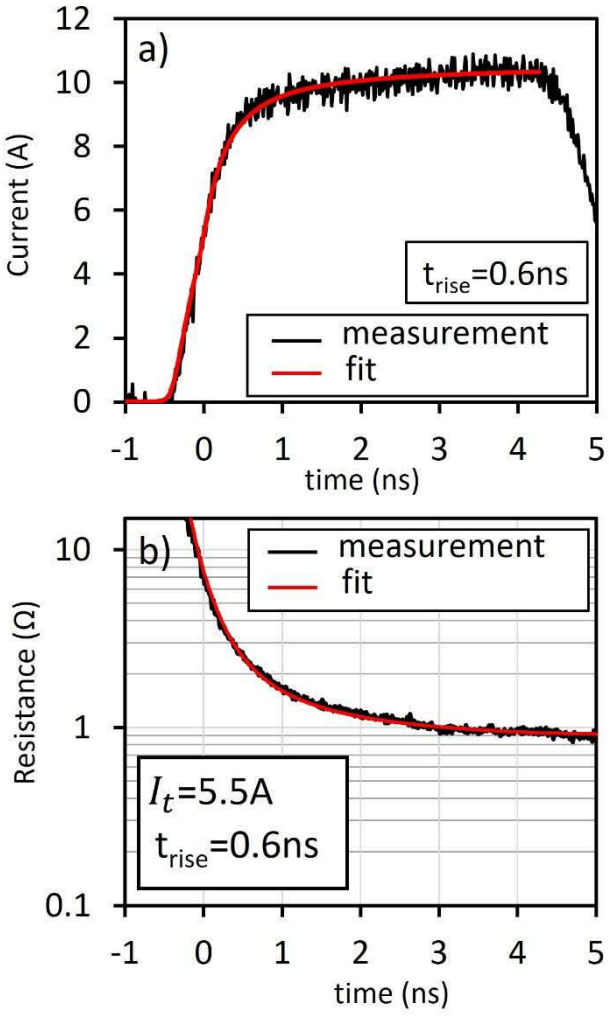

Figure 3: a) VF-TLP current and fit. b) transient resistance of TVS device for a VF-TLP pulse of 5.5A. Measurement data is shown in black, the fitting functions are depicted as red curves.

Thus, to get an accurate result of the peak voltage at the IC, the current into the TVS device at the beginning of the TLP pulse needs to be estimated. The peak voltages of the stand-alone TVS device and the IC path are compared and the current is selected for which both peak voltages are equal. The rationale is that the behavior of the stand-alone TVS device and in the sub-system should be similar if the voltage overshoot is the same. The procedure to define this current is described below.

For a graphical evaluation the TVS device peak voltage is plotted vs the quasistatic current I_{TVS}^{qs}. To be able to plot the peak voltage $V_{Ic} = V_{TVS}$ of the IC path vs I_{TVS}, the left part of Eq. (3) is taken and evaluated at the time when the peak voltage of the TVS device is reached:

$$V_{IC}^{peak} = (L_{PCB} + L_{IC}) \cdot \frac{dI_{IC}^{peak}}{dt} + V_0 + R_{IC} \cdot I_{IC}^{peak} \quad (6)$$

I_{IC}^{peak} is replaced by $I_t^{peak} - I_{TVS}^{peak}$. The same is done for its time derivate. A VF-TLP current pulse keeps its shape independent of the maximum current. Therefore, a relation between the current and the current derivative at the peak voltage can be made: $I_t^{peak} = b \cdot I_t^{qs}$ and $\dot{I}_t^{peak} = a \cdot I_t^{peak}$, with a and b as constant factors and I_t^{qs} being the total current. The same procedure is done for I_{TVS}. However, I_{TVS}^{qs} is regarded as a variable. Thus, the right side of Eq. (6) becomes:

$$V_{IC}^{peak} = ((L_{PCB} + L_{IC}) \cdot a + R_{IC}) \cdot b \cdot I_t^{qs} + V_0 - ((L_{PCB} + L_{IC}) \cdot a + R_{IC}) \cdot b \cdot I_{TVS}^{qs} \quad (7)$$

A resulting graph for a VF-TLP current of 10 A is shown in Figure 4. If the peak voltage of the TVS device would always be reached at the same time, the values of the constants a and b would not vary with the applied current. The current where the two curves intersect could be selected as VF-TLP current to evaluate $R_{TVS}(t)$ for Eq. (6). Clearly, the time when the peak voltage is reached is dependent on the current as shown in Figure 5. For a VF-TLP current of 18A the peak voltage is reached earlier than for 0.5A. This means that a and b change with different total current as they need to be extracted at different times. This changes the red curve of Figure 4 with the total VF-TLP current I_t^{qs}. To find the correct a and b and thus the right VF-TLP current for the evaluation of $R_{TVS}(t)$ it must be made sure that V_{IC}^{peak} also occurs at the *same time* as V_{TVS}^{peak}.

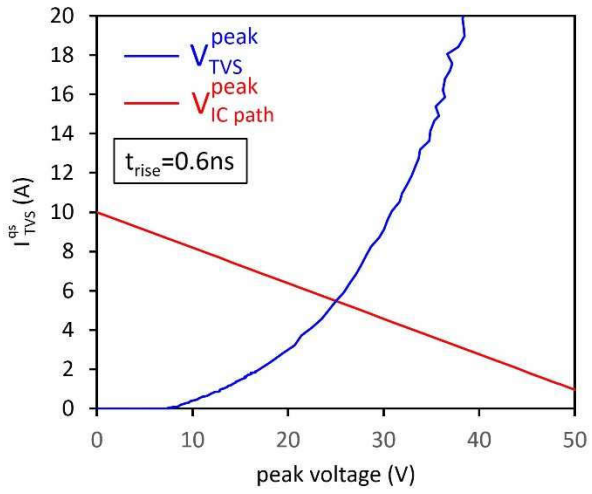

Figure 4: Peak voltage of the stand-alone TVS protection device (blue) and of the IC path (red) by using Eq. 7 for a VF-TLP current of 10A.

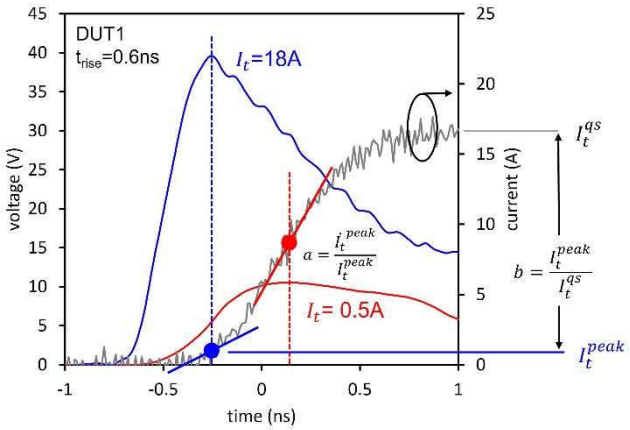

Figure 5: Transient voltage of the stand-alone TVS protection DUT1 for different currents. The grey current curve belongs to the blue voltage curve. The peak voltage occurs at different times which changes the parameters a and b because the current magnitude and the slope changes with time indicated by the slopes and circles in red and blue.

An easy way to achieve this, is by plotting I_{TVS}^{qs} of the stand-alone TVS protection device against the time when the peak voltage is reached for each current. For the IC path for a given VF-TLP current I_t the constants a and b are determined at different times and I_{TVS}^{qs} is recorded where $V_{IC}^{peak} = V_{TVS}^{peak}$ in Figure 4. Both results of I_{TVS}^{qs} are plotted vs time which can be seen in Figure 6. The intersection of both curves indicate the TVS current which needs to be used for the determination of $R_{TVS}(t)$ because the same peak voltage of the TVS protection device and the IC path is reached at the correct time.

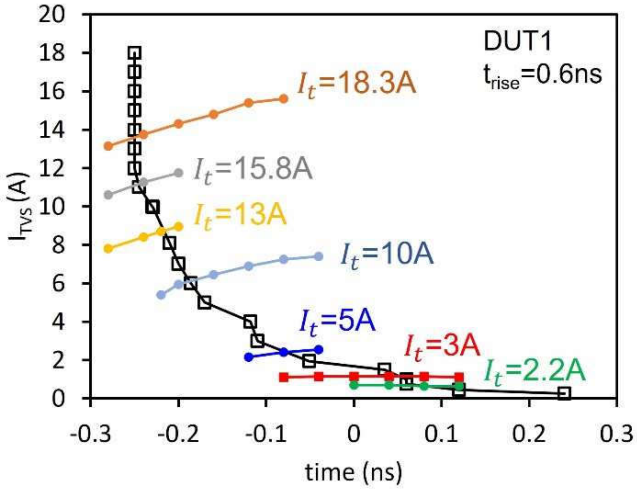

Figure 6: I_{TVS} vs time when the peak voltage is reached. The black open symbols are extracted from the stand-alone TVS protection device. The colored circles are extracted by using Eq. (7) and calculating the constants a and b at different times on the current curve (see Figure 5). The intersection of the black and colored curve indicate the current which is used for determining $R_{TVS}(t)$.

III. Measurement

Measurements were done using a custom PCB board [10] (see Figure 7) which has the same topology as shown in Figure 2. Instead of a real IC, a combination of up to two different discrete devices were used to serve as a replacement. Two combinations were used in this work to emulate an IC: a bipolar diode in forward direction with a 3.1 Ω resistor in series and the 3.3 Ω resistor alone was used in this work. There are voltage pick-ups (using 1 kΩ resistors) at the location of the TVS device and the IC. Between the TVS device and the IC there is an inductive current pick-up which yields the current flowing into the IC. The VF-TLP equipment from a HPPI TLP-8010C [11] is connected via a SMA connector to the input of the board. The signals are recorded by a 33 GHz Tektronix DPO/3304DX oscilloscope with 20 GHz TCA292D adapters. The effective bandwidth is 20 GHz. The rise-time of the VF-TLP pulse was set to 0.6 ns and 1 ns. For the TVS protections three different devices were chosen: two devices with a deep snapback and a high and low trigger voltage and a shallow snapback device with a medium trigger voltage. The devices are chosen so that the peak overshoot voltage has a strong variation. This allows to verify the calculation in a wide parameter range. The quasistatic VF-TLP voltages as well as the peak voltages are shown in Figure 8. The inductance of the PCB trace has been determined by TLP measurements using a rise-time of 5 ns and the value was verified at 10 ns. For this measurement no components were placed on the board and the 1 kΩ resistor at the IC was replaced by a 0 Ω resistor. The transient voltage overshoot was measured with needles at different positions of the PCB to determine the inductance per length. The calculated value of the PCB inductance for the trace section marked in green is $L_{PCB} = 2.7$ nH.

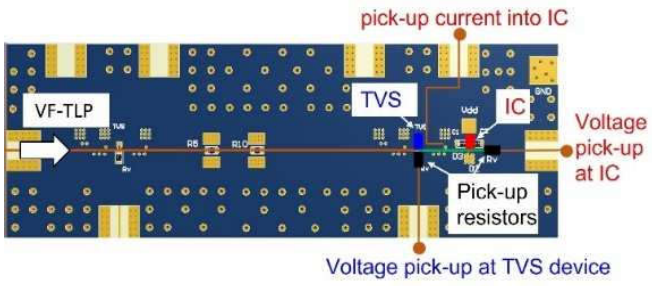

Figure 7: PCB board layout used for the I/O port measurements.

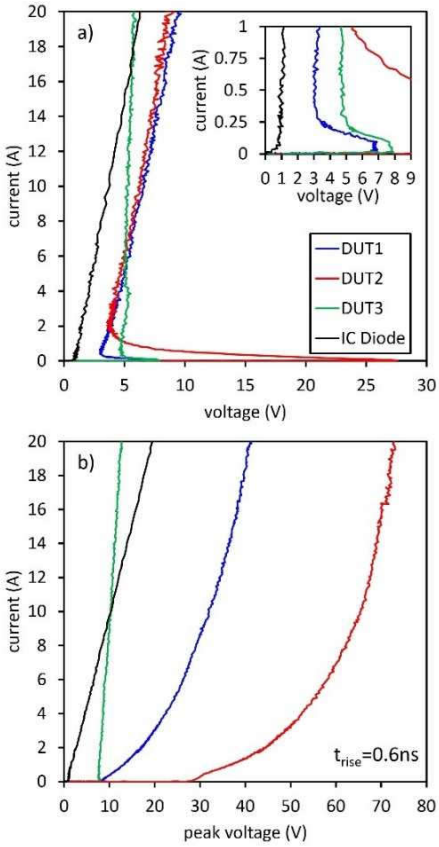

Figure 8: a) quasistatic VF-TLP IV curves of the stand-alone devices. the inset shows a magnification at low currents. b) peak voltages of the stand-alone devices for different VF-TLP currents.

The diode which together with the resistor is used to emulate the IC can be described by a diode which happens to have V_0=1.02 V and a resistance of 0.2 Ω. The device has a parasitic inductance of 0.8 nH. The quasistatic voltage and the peak voltages are shown in Figure 8.

For a first characterization only the 3.3 Ω resistor was placed on the board. Here, a small transient voltage overshoot was detected (shown in Figure 9) which is linear in current and increases with smaller VF-TLP rise-time. This behavior indicates that the overshoot voltage is caused by a parasitic inductance. By fitting the transient voltage using the measured current of the current pick-up and verifying it at different rise-times the value of the parasitic inductance to the 3.3 Ω resistor of $L_{IC} = 1.5$ nH was determined. Please note that without a parasitic inductance also the slope of the rising and falling edge of the voltage cannot be well reproduced as shown by the green dashed curve in Figure 9(b).

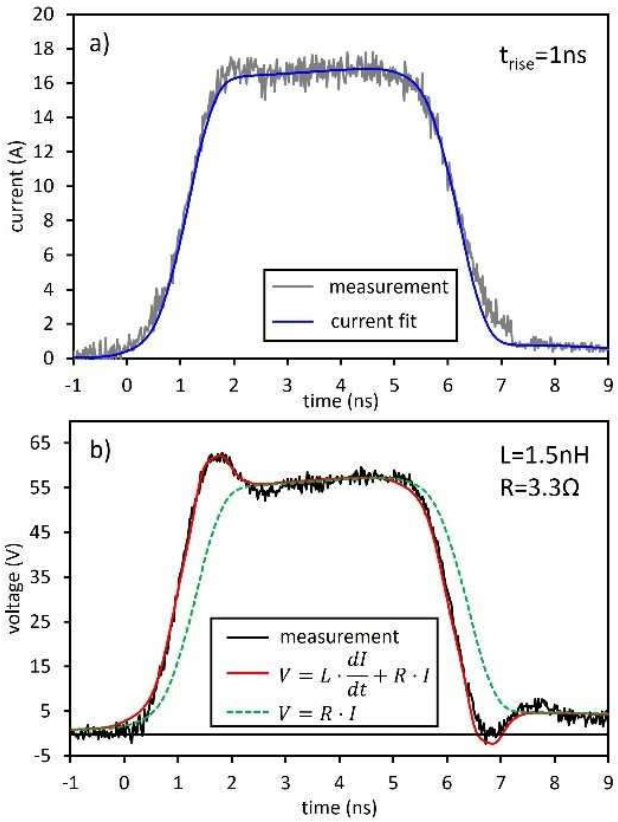

Figure 9: a) measured and current of the 3.3Ω resistor which emulates the IC and a fit with $atan(t)$ functions b) measured voltage and fit of voltage taking only the resistance value into account (greed dashed) and with a parasitic inductance (red). A small linear voltage offset has been added to both curves. One can see that the small voltage overshoot can be well reproduced by the parasitic inductance.

For the final inductance value between TVS device and IC a value of 5 nH for IC diode plus resistor and 4.2 nH for the resistor only has been used.

Figure 10 shows the quasistatic VF-TLP curve of the board at the position of the TVS device DUT1 with (green) and without the TVS device (red) and the stand-alone DUT1 (not mounted on the board) (blue). The IC is emulated by the 3.3 Ω resistor. For the full system (green curve) at low currents the TVS device is turned off and the voltage at the TVS coincides with the voltage when only the resistor is mounted. At a total current of 1.8 A the transient voltage overshoot at the TVS device is sufficiently high to starts its turn-on and is fully turned on at 2.2 A. The trigger voltage of the TVS device also seems to be lower if it is placed on the board instead of being measured alone. This apparent trigger voltage reduction of the TVS device is a direct consequence of the transient voltage overshoot caused by the inductances in the IC path.

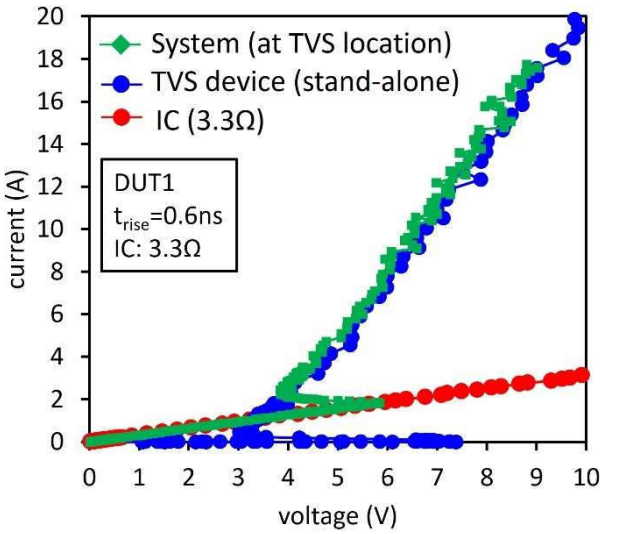

Figure 10: Quasistatic VF-TLP plot of the system at the TVS location (green), the IC (3.3Ω replacement) and the TVS device (alone)

Figure 11(a) shows the transient voltages at DUT1 and the IC location for a VF-TLP current of 10 A. Again the IC emulation consists of the 3.3 Ω resistor. Due to the parasitic inductance in the IC path the measured voltage at the IC is not the voltage at the I/O. After subtracting the voltage drop over the inductance from measurement, the red curve is obtained which is the transient voltage at the IO of the IC. It is observed that the peak voltage is reached at the time when the I/O and the TVS device have the same value, i.e. $V_{TVS} = V_{IC}$, as predicted by Eq. 3 because the voltage drop over any inductance in the IC path vanishes at this time where $\frac{dI_{IC}}{dt} = 0$. This means that the PCB trace and parasitic inductance have no direct impact on the peak voltage at the I/O. Indirectly, the inductances do influence the peak voltage by increasing the voltage on the TVS device to turn it on and thus diverting enough current to the TVS device. In addition, the time when the peak voltage at the I/O of the IC is reached, the overshoot voltage at the TVS is already significantly reduced. This delay is caused by the interplay of the still rising total current and the continuing decrease of the TVS resistance R_{TVS}. This implies that not only the peak voltage of the TVS device is critical for limiting the peak voltage at the IC I/O but also the time needed for the TVS device to reach its quasistatic state as it determines the slope of the falling edge of the voltage overshoot at the TVS location.

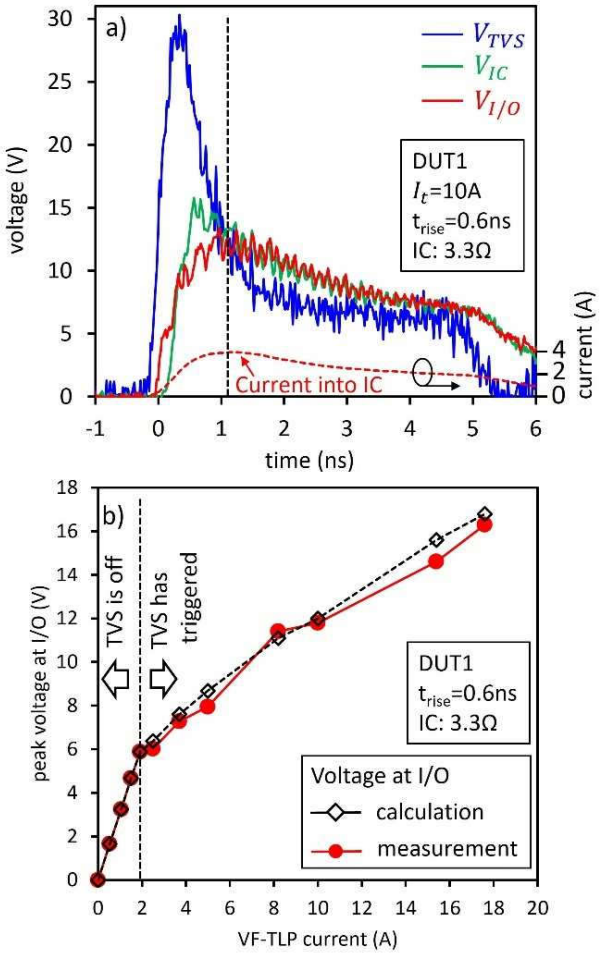

Figure 11: a) Transient voltages V_{TVS}, V_{IC} and $V_{I/O}$. The peak voltage at the I/O is reached when $V_{TVS} = V_{I/O}$ (indicated by the vertical black dashed line). b) Peak voltage at the I/O of the IC for different VF-TLP currents. Black symbols are derived from measurement value, red are calculation results.

Figure 11(b) shows the peak voltage at the I/O of the IC. The resistance of the system, given by the slope of the curve, starts to change once the TVS device turns on, which indicates that a large percentage of the total current is diverted from the IC to the TVS device. The calculated peak voltage obtained by the described method is able to reproduce the peak voltage very well.

Figure 12 shows measurement and calculation results for the three different TVS protection devices presented in Figure 8 for a rise time of 0.6 ns. The IC is emulated by the IC diode and the 3.3 Ω resistor in all cases.

In Figure 13 results of the two deep snapback devices DUT1 and DUT2 are shown for the two different IC emulations. As expected, the peak voltage is about 1V higher if the diode and the resistor is used instead of just the resistor. Figure 14 shows a comparison of measurement and calculation for a rise time of 1 ns.

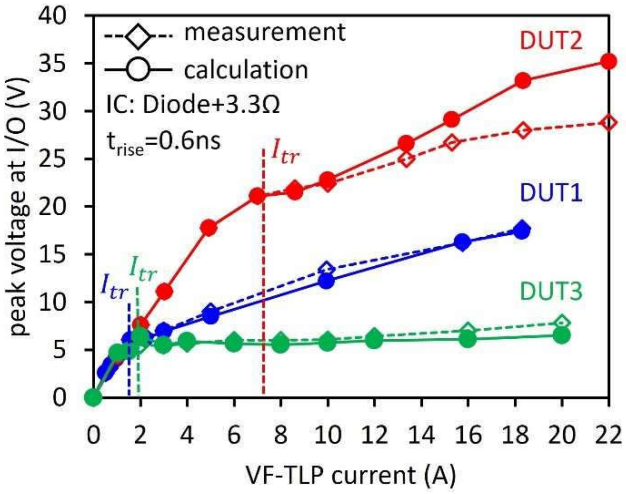

Figure 12: measured and calculated peak voltage for three different TVS protection devices. The calculation shows a good agreement with measurement.

For all variations done in these investigations, i.e. different TVS devices, IC emulation set ups and rise times, there is good agreement between measurement and calculation. The maximum error occurs for DUT2 at high currents (see Figure 12) which is about 20%.

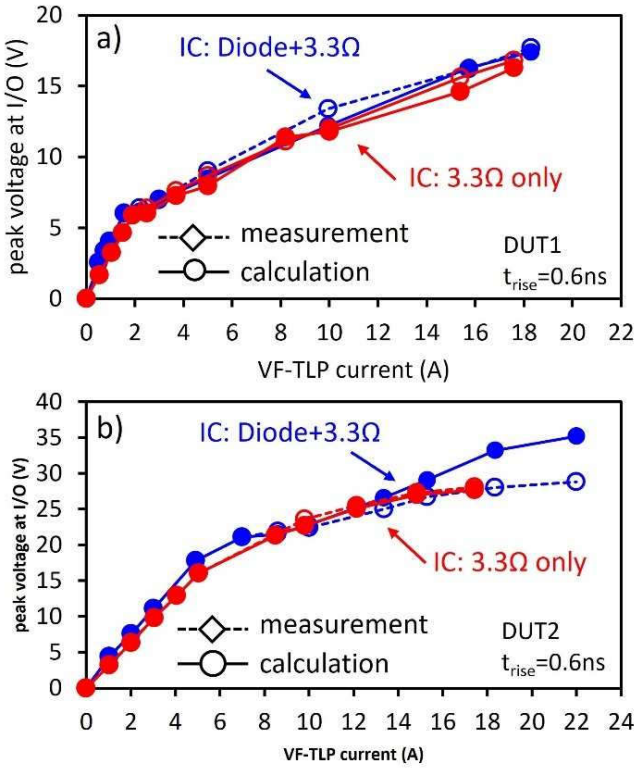

Figure 13: peak voltage measurement and calculation for the two different IC emulations: a) DUT1, b) DUT2.

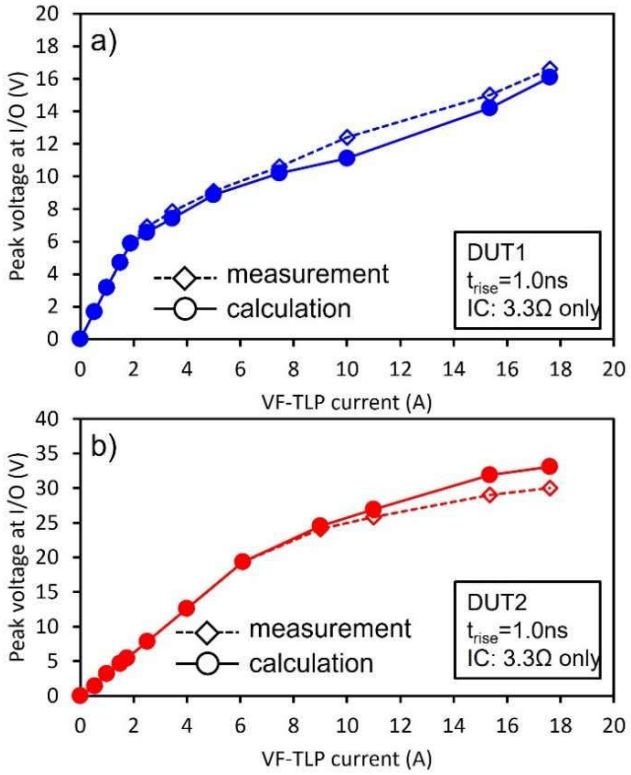

Figure 14: peak voltage measurement and calculation for a VF-TLP rise time of 1ns: a) DUT1, b) DUT2.

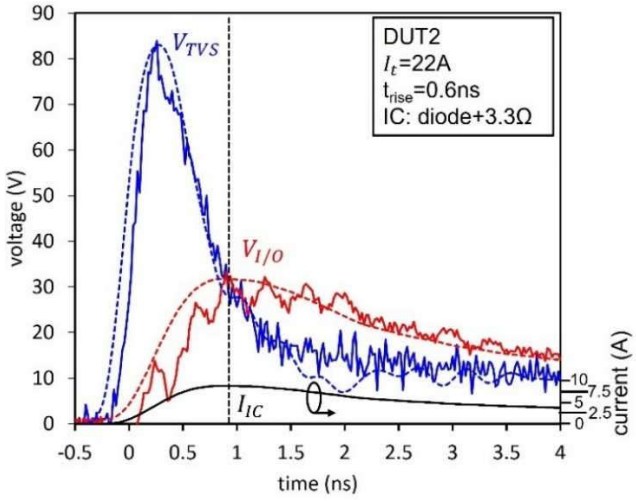

Figure 15: transient voltages at different positions on the board and current into the IC. The dashed curves describe calculated voltages which are obtained by using the deconvoluted current I_{Ic} is inserted into Eq. (1) (red dashed line) and if the voltage drop of the parasitic inductance of 1.5 nH is added to the calculated voltage drop across the IC emulation set up (green dashed line). The blue dashed line is the calculated voltage drop at the TVS protection.

The transient voltage curves are shown in Figure 15 for I_t=22 A. Relatively large oscillations of about 7 V peak-to-peak amplitude can be observed. These are much less pronounced at lower currents. As measurement value the average between the minimum and maximum has been taken. The oscillations might have shifted the readout of the measurement results to lower values and thus causing the larger deviation of measurement and calculation. This is supported by the fact that the calculated voltage drop (red dashed line), which is obtained by inserting the measured current I_{IC} into Eq. (1), gives values which coincide with the maxima of the oscillations. The blue dashed line shows the calculated voltage drop at the TVS location. Here, the total inductance of 5 nH of the IC path is taken into account and added to the calculated voltage drop across the emulated IC. A good fit to the measured peak voltage is observed which indicates that current into the IC is correctly measured.

IV. IC protection devices with snapback

The method described in this work in principle requires that the IC on chip ESD protection either does not have a snapback or that it is instantly turned on, i.e. there is no significant voltage overshoot which originates in the silicon. Parasitic inductances are covered in the described method.

However, it is likely that the methodology also works for devices which have a snapback. If the on-chip protection snaps back quickly so that it has entered its quasi-static state when the TVS protection is still turning on, one could completely neglect it in the on-chip modeling. For a certain quantification one could say that the snapback can, as for the TVS protection can be described by a time dependent resistance. In this paper R_{IC} has been assumed to be constant. Thus, for the method to work the derivative with respect to time of R_{IC} needs to be essentially zero when the peak current into the IC is reached. As a rule of thumb, for a VF-TLP pulse with a rise time of 0.6 ns the on-chip ESD protection should have settled into its quasi-static state after the nominal rise time of the VF-TLP pulse.

V. Conclusion

Knowing the peak voltage at IC I/O is essential as gate oxide breakdowns by a transient overvoltage can affect system level ESD robustness. A method for calculating the peak voltage at the I/O without the need for

simulation software has been presented. It is valid for an important case, namely that the non-snapback IC ESD protection can be described by a quasi-static (VF)-TLP curve, i.e. the IC typically has no or only little transient voltage overshoot which originates from the silicon. Transient voltage overshoots caused by parasitic inductances of the on-chip ESD protection may exist and they are incorporated into the method. The method only needs measurement data, i.e. transient data of the TVS device by itself (which may be obtained from the supplier), the quasi-static (VF)-TLP curve of the IC ESD protection and the inductance of the trace between the TVS device and IC. A full-blown transient SEED model is not required. Indeed, no simulation software is needed to estimate the peak voltage at the IC I/O pin.

Different TVS protection devices with strongly varying trigger voltage have been used to verify the method. The IC has been emulated by different methods and the rise time of the VF-TLP pulse has been set to 0.6 ns and 1 ns. The results of the method with measurements shows a good agreement over the entire range of parameters with an error of typically less than 10%. The measurements also show that the peak voltage at the IC happens at a later time which emphasizes the need to lower TVS device overshoot voltages and a fast device turn on to limit the peak voltage at the I/O of the IC.

The authors would like to thank Thomas Kalscheid for fruitful discussions.

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