

Modular Model Predictive Control with Regulated Third Harmonic Injection for Zero-Sequence Stabilized LCL Inverter

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Abstract—A modular model predictive control method for non-isolated three-phase LCL grid-connected converter is proposed with zero-sequence voltage control and regulated third harmonic injection capabilities. The control method is proposed with the combination of a modified three-phase LCL converter topology to stabilize the common mode voltage. The control mechanism consists of two layers: (1) the central level control of dq sequences output current control cascaded with (2) the local level control of zero-sequence voltage, three-phase inductor current/capacitor voltage model predictive control. No grid side inductance value is needed for the two-layer cascaded control structure which both improves the dynamic performance from inner MPC loop and avoids the MPC parametric error caused by the uncertainty of grid side inductance. With the zero-sequence model predictive control, the common mode voltage and leakage current can be attenuated without bulky isolation transformer. A regulated third harmonic injection (RTHI) method is designed based on the zero-sequence voltage control and the proposed modified converter topology to improve the DC bus utilization and avoid the over-modulation issue. Compared with the conventional third harmonic injection methods, no extra harmonics are injected to the grid and there is no need for specialized grid THD optimization algorithm with the proposed zero-sequence controlled RTHI. The stability and robustness of the proposed regulated third harmonic injection method are also improved with the zero-sequence MPC regulation. Also, the modular concept of local MPC module enables the extensibility for the power converter control with a flexible number of phases. The dynamic performance, leakage current attenuation, DC bus utilization and grid-connection power quality of the proposed model predictive control method with RTHI have been validated experimentally.

Index Terms—Modular Model predictive control, Non-isolated DC/AC converter, LCL filter, zero-sequence voltage control, regulated third harmonic injection, DC voltage utilization.

I. INTRODUCTION

MODEL predictive control is gaining significant research attention with the tremendous development of digital signal processing over the past decades. In the grid-connected power converter applications such as electric vehicle (EV) charger and photovoltaic (PV), leakage current issue and DC bus utilization are two key factors that influence the performance. For the leakage current issue, a bulky line frequency transformer is typically installed to block the leakage path at the point of common coupling (PCC) which increases the cost, volume and weight of the system. For the DC bus utilization, the DC bus voltage needs to be stepped up to be at least twice of the grid voltage amplitude to avoid saturation issue which brings extra switching losses and challenges to the switch

voltage tolerance capability. This paper focuses on the combination of modular MPC with zero-sequence voltage control and regulated third harmonic injection (THI) techniques in a modified non-isolated three-phase LCL converter.

Firstly, MPC is typically designed to solve a constrained finite time optimal control (CFTOC) problem at each of the digital sampling time period which includes continuous control set (CCS) MPC and finite control set (FCS) MPC [1]. CCS-MPC is implemented with space vector modulation (SVM). And FCS-MPC is directly leveraging the duty cycle for pulse width modulation (PWM) of the switching states [2], [3]. For the computation burden of MPC, the normal control algorithms for the simple two-level converters could be achieved by the DSP controllers [4]–[6]. However, other types of MPC implementations, especially the cases with online optimization procedures, constrained variables, longer horizon or multi-level converters, typically require more calculation power. The commonly used micro-controller of DSP may have limits to execute the control algorithms within the certain control period. A more costly FPGA can be leveraged for a faster calculation [7]–[11]. The explicit MPC can be applied to derive the offline control law to simplify the control execution process [12]. This paper developed a modular MPC method in an explicit way by generating an offline-derived piecewise affine function for per phase LC control. This simplified MPC makes it possible to develop the control in a less costly DSP instead of FPGA. Leveraging the TI C2000 control card, the local per phase MPC algorithm can be implemented either in an individual interrupt for per phase switch leg PWM control or in separate local control devices communicated with CAN. The advantages of the proposed modular MPC can be listed as: (1) per phase explicit implementation in local interrupt or device saves computation power for MPC; (2) modular MPC is scalable and flexible for multiple phases in parallel.

Secondly, for a non-isolated three-phase grid-connected LCL converter, the leakage current can be generated by the high voltage, high switching frequency pulse width of the switching phase legs [13]. The leakage path is typically excited through the parasitic capacitance among the chassis of the power module, DC bus terminals and grid neutral point [14]. A bulky line frequency transformer or high frequency transformer with an extra DC/DC power stage is needed to block the leakage current path from flowing into the grid [15]. Transformerless topologies have been studied by adding extra switches and passive components to attenuate

the common mode leakage current which result in more cost and modulation complexity [16], [17], [18]. For the topological contribution of this paper, instead of the conventional topology in Fig. 1(a), a modified non-isolated single-stage DC/AC converter is proposed by connecting the common point of three-phase LCL capacitors to the positive/negative DC bus terminals to bypass the leakage current as is shown in Fig. 1(b). Without introducing extra switches or passive devices, a zero-sequence voltage MPC control method is designed based on the proposed topology to stabilize the common mode voltage and attenuate the leakage current from a control perspective. The cost of high/low frequency transformers for common mode isolation is saved accordingly.

Thirdly, for the DC bus utilization, the THI can be implemented to avoid duty cycle saturation with a relatively low DC voltage [19]. To evaluate the DC bus utilization, a modulation index can be calculated as the ratio of AC output voltage fundamental component (grid voltage) peak value to the modulation waveform fundamental component (DC bus voltage) peak value. Several methods have been studied to improve the DC bus utilization, e.g., third harmonic sinusoidal waveform injection for sinusoidal PWM (SPWM), triangular waveform injection for space vector pulse width modulation (SVPWM) [20]. Among the aforementioned injection methods, the SPWM-based mechanism is simpler to implement in the DSP [21], [22]. However, if the third harmonic or triangular waveforms are directly injected in the duty cycle before the modulation, the control stability and robustness will be affected and even the divergence could occur in the PWM modulation. Also, the conventional THI approaches will inject extra harmonics to the grid which will deteriorate the power quality of the grid voltage and current. Even [21] and [22] have proposed optimized THI algorithms to minimize the grid distortion of THI, the injected grid harmonics cannot be fully eliminated. And the optimization look-up table from the published methods accounts for extra computation resources and brings more control complexity. For the modulation contribution of this paper, a simple MPC-based zero-sequence regulated third harmonic injection method is proposed without the need of introducing optimization algorithm and no extra harmonics are injected to the grid. The power quality and system stability are improved. Combined with the proposed topology and MPC-based regulated THI method, the DC bus utilization is improved in a robust way without injecting harmonics to the grid and the complexity of optimization methods in [21] and [22] are saved.

The paper is organized as follows. Firstly, the circuitry model of the proposed non-isolated three-phase grid-connected converter in Fig. 1(b) is analyzed in detail. The common mode circuit with parasitic path is illustrated. Also the equivalent circuit model in $dq0$ reference frame is analyzed. Secondly, the proposed modular MPC control method is introduced with zero-sequence voltage controller to stabilize the common mode voltage. The control mechanism includes the central level grid current dq control and local level MPC of zero-sequence voltage control and three-phase capacitor voltage/inductor current control. The local MPC module algorithm is designed based on the management of switch side per phase LC filter

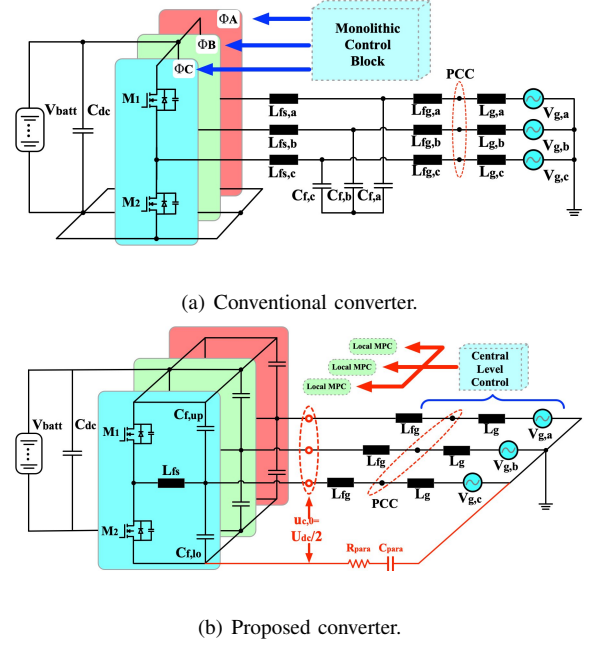


Fig. 1. (a) Conventional LCL converter with monolithic control and (b) proposed non-isolated three-phase LCL converter with modularized MPC.

inductor current and capacitor voltage. Thirdly, the regulated third harmonic injection method is proposed based on the zero-sequence voltage control to improve the DC bus voltage utilization without injecting extra harmonics to the grid. Finally, the experimental results are shown to validate the proposed control methods. The main contributions of this paper include: 1) the connection between the common points of the output capacitors with the positive/negative terminals to bypass the leakage current/third order harmonic and stabilize the common mode voltage; 2) two regulated THI methods based on zero-sequence voltage control for a stable and robust implementation of DC bus utilization improvement without extra harmonics to deteriorate the grid; 3) cascaded outer loop grid current control and inner loop per LC module MPC for transient performance improvement and high accuracy with immunity from grid inductance variations; The main differences from the conference paper of [23] can be concluded as: 1) the control structure is improved with cascaded outer loop grid current control and inner loop per phase module MPC to improve the dynamic performance; 2) the zero-sequence control is implemented by the local MPC instead of PI control; 3) zero-sequence regulated sinusoidal and triangular THI methods are developed to improve the DC bus utilization.

II. SYSTEM MODELING

The proposed non-isolated three-phase DC/AC converter has been shown in Fig. 1(b). Different from the traditional two-level three-phase DC/AC converter, the common point of three-phase capacitors is connected to the DC bus positive/negative terminals to create a bypassing path for zero-sequence voltage model predictive control. By leveraging the topological modification and zero voltage control, the common mode voltage can be stabilized to reduce the leakage current.

A. DC/AC LCL Converter Modeling

The DC/AC converter is directly interfaced with the grid. To maintain a constant common mode voltage, the proposed control method is based on the $dq0$ coordinate system to leverage the zero-sequence voltage component in the proposed topology. Compared with the abc system, the active/reactive power and common mode voltage can be controlled independently with d, q and 0 sequence components in a $dq0$ system. The coordinate system model of the proposed DC/AC converter can be derived from abc reference frame.

1) *abc system*: The state space equations in abc system are expressed as:

$$\dot{i}_{L,abc} = \frac{1}{L_{fs}} \mathbf{I} u_{x,abc} - \frac{1}{L_{fs}} \mathbf{I} u_{c,abc} \quad (1a)$$

$$\dot{u}_{c,abc} = \frac{1}{C_f} \mathbf{I} i_{L,abc} - \frac{1}{C_f} \mathbf{I} i_{g,abc} \quad (1b)$$

$$\dot{i}_{g,abc} = \frac{1}{L_{fg}} \mathbf{I} u_{c,abc} - \frac{1}{L_{fg}} \mathbf{I} u_{g,abc}, \quad (1c)$$

where L_{fs} , C_f and L_{fg} are the switch side inductor, capacitor and grid side inductor, respectively, for the LCL filter. $i_{L,abc}$, $u_{c,abc}$, $i_{g,abc}$ and $u_{x,abc}$ are the switch side inductor current, capacitor voltage, grid side current and grid voltage, respectively. $\mathbf{I} \in \mathbb{R}^{3 \times 3}$ is the identity matrix.

2) *dq0 system*: Since it is difficult to control the time-varying sinusoidal references in abc system while convenient to calculate the active/reactive power and stabilize zero-sequence voltage in $dq0$ system, the state space model is transformed to $dq0$ reference frame for control purpose of the proposed method. Coordinate system transformation has been widely applied in the three-phase AC systems because the dq system can transfer the time-varying sinusoidal waveforms to equivalent constant DC values [24]. For the implementation of control, the DC values are much easier to be controlled than AC values. However, the traditional methods mainly utilize the dq system without considering the zero-sequence. The proposed topology connects the common point of AC three-phase capacitors to the DC bus positive/negative terminals which permits to extract the zero-sequence from abc system to $dq0$ system and control the zero-sequence voltage to be half of DC bus voltage. Thus, the u_{cm} can be stabilized accordingly.

For the reference frame transformation with zero-sequence components, abc system needs to be firstly transformed to $\alpha\beta 0$ and then to $dq0$ system. From abc to $\alpha\beta 0$, the Clarke transform is applied as:

$$x_{\alpha\beta 0} = \mathbf{T} x_{abc} = \frac{2}{3} \begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \\ 1/2 & 1/2 & 1/2 \end{bmatrix} x_{abc}. \quad (2)$$

In $\alpha\beta 0$ system, the signals are composed of two orthogonal sinusoidal AC waveforms in α and β frames and a zero-sequence component. A Park transform is implemented secondly to convert the stationary reference frame of $\alpha\beta 0$ to the rotating $dq0$ system which is calculated as:

$$x_{dq0} = \mathbf{P}(\theta) x_{\alpha\beta 0} = \begin{bmatrix} \cos\theta & \sin\theta & 0 \\ -\sin\theta & \cos\theta & 0 \\ 0 & 0 & 1 \end{bmatrix} x_{\alpha\beta 0}. \quad (3)$$

θ is the phase angle of the grid which is tracked with a phase-locked-loop (PLL) controller by measuring the grid voltage at the point of common coupling (PCC). Thus, the AC sinusoidal signals in abc are converted to DC values in a rotating $dq0$ frame with a time-varying angle of θ . Considering the control requirements to finally implement the duty cycles in abc format for the PWM modulation, the inverse Clarke and Park transformations are needed to convert the output of control signals from $dq0$ to abc :

$$x_{abc} = \mathbf{T}^{-1} x_{\alpha\beta 0} = \mathbf{T}^{-1} \mathbf{P}(\theta)^{-1} x_{dq0}. \quad (4)$$

Based on equations (2) and (3) of the coordinate system transformations, the state space equations of (1) can be transformed from abc to $dq0$:

$$\dot{i}_{L,dq0} = \frac{1}{L_{fs}} \mathbf{I} u_{x,dq0} - \frac{1}{L_{fs}} \mathbf{I} u_{c,dq0} - \omega \mathbf{G} i_{L,dq0} \quad (5a)$$

$$\dot{u}_{c,dq0} = \frac{1}{C_f} \mathbf{I} i_{L,dq0} - \frac{1}{C_f} \mathbf{I} i_{g,dq0} - \omega \mathbf{G} u_{c,dq0} \quad (5b)$$

$$\dot{i}_{g,dq0} = \frac{1}{L_{fg}} \mathbf{I} u_{c,dq0} - \frac{1}{L_{fg}} \mathbf{I} u_{g,dq0} - \omega \mathbf{G} i_{g,dq0} \quad (5c)$$

where ω is the angular velocity of the grid in rad/s. \mathbf{G} is the matrix for the coupling terms resulted from the transformation:

$$\mathbf{G} = \begin{bmatrix} 0 & -1 & 0 \\ 1 & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix}. \quad (6)$$

By leveraging the $dq0$ state space equations and the connection of three-phase capacitors common point with DC bus positive/negative terminals, the zero-sequence voltage can be controlled explicitly to stabilize the u_{cm} .

The equivalent circuits of the $dq0$ system for proposed topology of DC/AC side converter are shown in Fig. 2.

B. Common Mode Analysis of Non-Isolated Inverter

For a conventional transformerless three-phase grid-connected system as is shown in Fig. 1(a), there exist common mode leakage current paths among the grid neutral, chassis of the power module and DC ground due to the high frequency common mode voltage, v_{cm} , fluctuation on the switch side and the equivalent parasitic capacitance, C_p [25]. The leakage current, i_{lkg} , will flow through the common mode path and can be derived as:

$$i_{lkg} = C_p \frac{dv_{cm}}{dt} \quad (7)$$

The level of leakage current is mainly dominated by the fluctuating rate of common mode voltage and equivalent impedance of parasitic capacitance [26], [27]. The fluctuation of common mode voltage is induced by the intrinsic high switching frequency of the circuit and can be expressed as

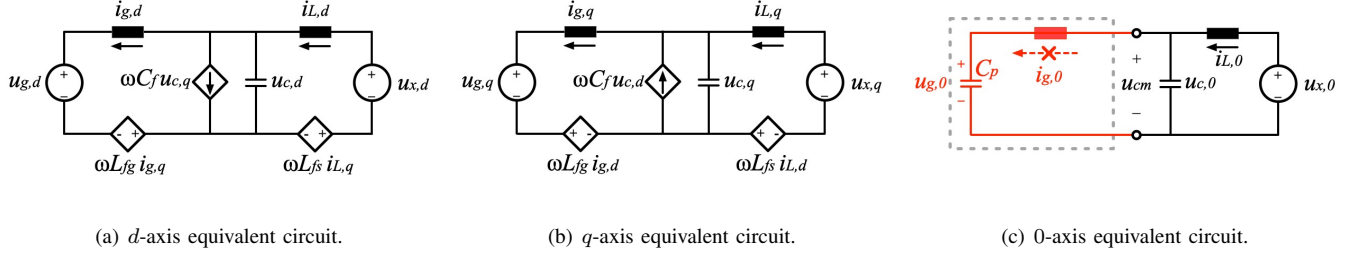


Fig. 2. $dq0$ equivalent circuits of the proposed topology on DC/AC side.

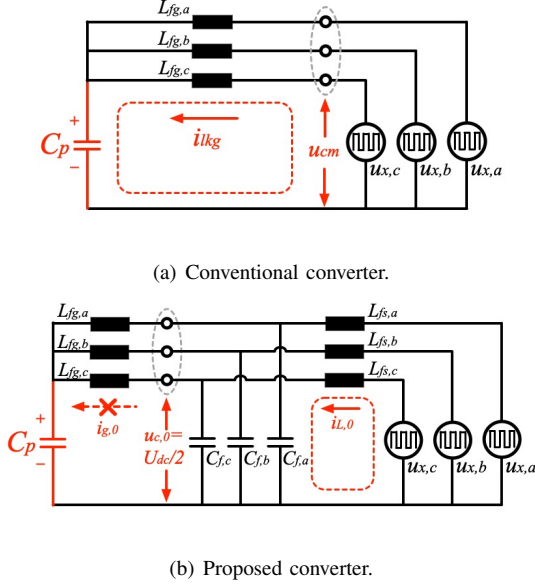


Fig. 3. Equivalent common mode circuit of the (a) conventional and (b) proposed non-isolated DC/AC converter.

the mean value of three-phase switching legs output voltages, $v_{x,a}, v_{x,b}, v_{x,c}$:

$$v_{cm} = \frac{v_{x,a} + v_{x,b} + v_{x,c}}{3}. \quad (8)$$

Fig. 3(a) shows the equivalent common mode circuit in a traditional non-isolated DC/AC converter where the red dotted lines with arrows represent the leakage current. This leakage current is excited by the high frequency fluctuation of common mode voltage in the parasitic path. So, the leakage current is mainly determined by two factors: (1) rate of u_{cm} ; (2) parasitic capacitance. Firstly, according to equation (8), the mean value of three-phase switching legs output voltages is square waveforms with an amplitude of DC bus voltage at switching frequency level. Thus, the rate of change, du_{cm}/dt is high to amplify the leakage current. Secondly, the parasitic capacitance, C_p is another factor to influence the leakage current. The value of C_p varies in the solar and EV charging systems. For a typical photovoltaic system, C_p is ranged between 10nF-100nF. However, in a EV system, C_p is between 1nF-10nF [28]. For the safety consideration of the standard requirements, the leakage current is limited to be no more than 30mA in a EV system by IEC 62955:2018 and

IET Wiring Regulation 18th Edition (BS 7671:2018) Section 722.531.2.101.

Fig. 3(b) presents the equivalent common mode circuit in the proposed non-isolated DC/AC converter where the leakage current to the grid can be bypassed with the connection of three-phase output capacitors common point and DC positive/negative terminals. This leakage current attenuation capability is achieved by the proposed zero-sequence voltage controller which aims at stabilizing the zero-sequence capacitor voltage to be a constant value of half DC bus voltage, $u_{dc}/2$, instead of a high frequency fluctuating square waveform.

III. CONTROL DESIGN

The proposed model predictive control method of non-isolated three-phase LCL converter with zero-sequence voltage stabilization capability is illustrated in this section. Fig. 4 shows the control diagram which consists of the central level control of dq sequences output current PI control cascaded with the local level control of zero-sequence voltage, three-phase inductor current/capacitor voltage model predictive control. The local level modular MPC is implemented for each phase of LC module. The modularized local MPC enables the extensibility for random phase number of power converter control and reduces the computational complexity of multi-phase MPC algorithm as a whole function.

A. Phase-locked-loop

The transformations between abc and $dq0$ needs the real-time phase angle information, θ , of the grid voltage [29]. An effective way can be implemented with a PI controller by controlling the q component of the grid voltage, $v_{g,q}$, to be zero to derive the angular velocity, ω , of the phase angle. Then, the θ can be calculated with a period of 2π . And based on the active/reactive power calculation in

$$\begin{bmatrix} P \\ Q \end{bmatrix} = \frac{3}{2} \begin{bmatrix} u_{g,d} & u_{g,q} \\ u_{g,q} & -u_{g,d} \end{bmatrix} \begin{bmatrix} i_{g,d} \\ i_{g,q} \end{bmatrix} \quad (9)$$

the d -axis and q -axis represent the active and reactive power, respectively.

B. Central Level Output Current Control

The output current is transformed from abc to dq reference frame with Clarke and Park transformations. Then, two PI controllers are configured to regulate the dq sequence output

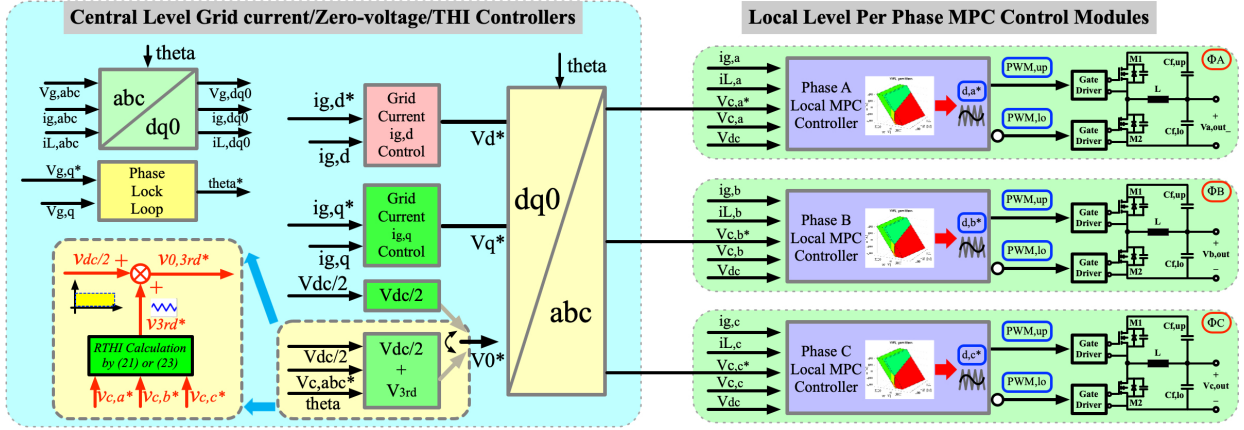


Fig. 4. Proposed modular MPC control diagram of the non-isolated DC/AC converter.

currents, $i_{g,d}$ and $i_{g,q}$, respectively. Based on the configuration of PLL to control the q component of grid voltage, $v_{g,q}$, to be zero and the active/reactive equation in (9), $i_{g,d}$ and $i_{g,q}$ are linked to the active and reactive power control loops, respectively. The outputs of grid current controller, v_d^* and v_q^* , are the dq component references of output capacitor voltages which will be transformed back to abc reference frame and configured as the MPC references of three-phase output capacitor voltages, $v_{c,a}^*$, $v_{c,b}^*$ and $v_{c,c}^*$.

C. Zero-sequence Voltage Control

The zero-sequence voltage of the three-phase capacitors are controlled to be half of DC bus voltage with MPC to block the leakage current from flowing through the grid. As are shown in Fig. 2(c) of the 0-axis equivalent circuit and Fig. 3(b) of the abc frame equivalent common mode circuit, the zero-sequence output current can be attenuated by the stabilization control of zero-sequence capacitor voltage. Specifically, half of DC bus voltage measurement is configured as the reference of zero-sequence voltage controller and transformed from $dq0$ to abc frame for the three-phase LC capacitor voltage model predictive control. A third harmonic component extracted from the central level grid side inductor current controller output after reversed Park transformation can be added to the zero-sequence voltage reference to improve the DC bus voltage utilization which will be analyzed in the fourth section.

The working principle of zero sequence voltage control is based on the three phase output capacitor voltage reference MPC tracking. Specifically, in the central controller, the zero sequence component of the reference is designed as half of DC bus voltage measurement, $V_{dc}/2$. This reference is combined with dq components references from the output of grid side inductor current controllers and then transformed into abc reference frame for tracking references of the local three phase MPC controllers. Each of the reference input for three phase local MPC controller is composed of a sinusoidal AC component and a zero sequence DC component. Thus, the object and cost function of the zero sequence voltage MPC control is integrated into the three separate MPC configurations which is consistent with the illustration in (15). The three phase local

MPC tracking for zero sequence voltage control guarantees a stabilized common mode capacitor voltage and low leakage current.

For the MPC-based zero-sequence regulated THI control diagram in Fig. 4, the proposed third harmonic injection method is implemented on top of the zero-sequence control. Specifically, the desired third order components are extracted from the output of dq components grid current controllers after being transformed from dq to abc reference frame, $v_{c,a}^*$, $v_{c,b}^*$ and $v_{c,c}^*$. Then, the desired referenced third order components, v_{3rd}^* , are added up with the zero-sequence voltage reference, $v_{dc}/2$, to formulate the third harmonic injected zero-sequence reference for the MPC tracking. Thus, the MPC controller of each phase module will regulate the capacitor voltage with the same zero-sequence DC offset and third order harmonic to stabilize the common mode voltage and reduce the peak-to-peak voltage value.

D. Local Level Per Phase LC Filter MPC

An explicit MPC method is designed for the switch side capacitor voltage and inductor current control. As is shown in Fig. 4 of the control diagram, the three-phase capacitor voltages are controlled in abc frame to follow the references from the cascaded grid current controller's outputs. The switch side inductor currents are also regulated with the MPC by adjusting the weighting factor between $i_{L,abc}$ and $u_{c,abc}$. The benefits to configure the MPC per phase in abc frame can be concluded as: (1) the state space matrix of LC per phase is simpler than dq system to implement the offline piecewise affine optimization code in a less costly DSP controller; (2) The time-varying angular speed term, ω , in equation (5) can be omitted in the explicit MPC state space matrix for the offline optimization calculation; (3) Per phase MPC for LC is more flexible for a modular design perspective to extend the paralleled phase number and other topologies, e.g., DC/DC, single-phase DC/AC converters.

For the MPC implementation, in every control period, the MPC controller receives the measured switch side inductor current, $i_{L,abc}$, capacitor voltage, $v_{c,abc}$, grid current, $i_{g,abc}$, from ADC and capacitor voltage reference, $v_{c,abc}^*$ from the

grid current controller. An offline generated piecewise affine search tree is applied to derive the optimal duty cycle for the explicit MPC. The state equations of switch side LC filter can be expressed as

$$\dot{i}_L(t) = -\frac{1}{L_{fs}}u_c(t) + \frac{U_{dc}}{L_{fs}}d(t) \quad (10a)$$

$$\dot{u}_c(t) = \frac{1}{C_f}i_L(t) - \frac{1}{C_f}i_g(t). \quad (10b)$$

For the MPC implementation, the discrete state space equations can be transformed as

$$i_L(k+1) = i_L(k) - \frac{T_s}{L_{fs}}u_c(k) + \frac{U_{dc}T_s}{L_{fs}}d(k) \quad (11a)$$

$$u_c(k+1) = \frac{T_s}{C_f}i_L(k) + u_c(k) - \frac{T_s}{C_f}i_g(k). \quad (11b)$$

For the flexibility of implementing the explicit MPC and the convenience of experimentally adjusting the DC bus voltage during test, the last term of (11), $U_{dc}d(k)$, can be replaced by the phase leg output voltage, $u_x(k)$. The state-space model can be expressed in standard matrix format of

$$X_{k+1} = AX_k + Bu_k + Ee_k \quad (12)$$

where the variables and matrices represent

$$A = \begin{bmatrix} 1 & -\frac{T_s}{L_{fs}} \\ \frac{T_s}{C_f} & 1 \end{bmatrix}, B = \begin{bmatrix} \frac{T_s}{L_{fs}} \\ 0 \end{bmatrix}, E = \begin{bmatrix} 0 \\ -\frac{T_s}{C_f} \end{bmatrix}, \quad (13a)$$

$$X_k = \begin{bmatrix} i_L(k) \\ u_c(k) \end{bmatrix}, u_k = [U_{dc}d(k)], e_k = [i_g(k)]. \quad (13b)$$

In the MPC formulation, the inductor current/capacitor voltage references can be defined as \bar{X} and the tracking errors between the measurement and the references are expressed as \tilde{X} which are composed of

$$\bar{X}_k = \begin{bmatrix} i_{Lr}(k) \\ u_{cr}(k) \end{bmatrix}, \tilde{X}_k = \begin{bmatrix} i_{Lr}(k) - i_L(k) \\ u_{cr}(k) - u_c(k) \end{bmatrix}. \quad (14)$$

Thus, the cost function includes two terms

$$\min \sum_{k=0}^{N_c} \tilde{X}_k^T Q \tilde{X}_k + \sum_{k=0}^{N_p-1} \Delta u_k^T R \Delta u_k. \quad (15)$$

For the penalties of the cost function, Q and R represent the weighting factor matrices that are implemented on the state values and input values, respectively. Specifically, Q is a 2×2 matrix, $[Q_{11}, 0; 0, Q_{22}]$, which is applied for the tracking errors between the state variables and the references. Since the main target of the local MPC is to track the output capacitor voltage references, the corresponding weighting factor, Q_{22} , is configured to be 1000 times larger than the switch side inductor current term, Q_{11} . R is a 1×1 matrix, $[R_{11}]$ which is applied for stabilizing the variation between the adjacent input variables. R_{11} is set to be 100 times smaller than Q_{22} .

The constraints of the MPC controller can be expressed as

$$\tilde{X}_{k+1} = A\tilde{X}_k + Bu_k + Ee_k \in \mathcal{X} \quad (16)$$

$$\Delta u_k = u_k - u_{k-1} \in \mathcal{U} \quad (17)$$

$$\begin{bmatrix} -I_{L,max} \\ 0 \end{bmatrix} \leq X_k \leq \begin{bmatrix} I_{L,max} \\ U_{dc} \end{bmatrix} \quad (18)$$

$$[0] \leq u_k \leq [U_{dc}] \quad (19)$$

$$[-I_{g,max}] \leq e_k \leq [I_{g,max}]. \quad (20)$$

The developed MPC for per phase module LC filter is based on the linear state space model. The state space variables, $i_L(k)$, $u_c(k)$, and input variable, $d(k)$, are all decoupled terms in the modeling to be configured in the cost function of (15) and the constraints of (16) to (20). Thus, the control and stabilization targets can be convenient to achieve.

For the optimization process of the MPC implementation, Fig. 5(a) shows the detailed operating mechanism. The MPC algorithms are implemented in an explicit way. Specifically, the piecewise affine (PWA) feedback law is generated offline based on the pre-selected state space modeling and constraints. Then, the corresponding MPC partitions are configured into the micro-controller memory for online searching. In each of the controlling time period, the active region, s , is searched with the matrices $H_{s,c}$ and $K_{s,c}$. Then, in each of the specific active region, the corresponding feedback law matrices, $F_{s,c}$ and $G_{s,c}$, are applied to calculate the optimal input values with the prediction horizon. The first value of the input matrix is applied to the dynamic system for MPC control. Specifically, in the PWA function offline generation block of Fig. 5(a), the colored areas represent the n regions for MPC to search and optimize according to the feedback law. In the online MPC control block of Fig. 5(a), the matrices $H_{s,c}$ and $K_{s,c}$ will lead to an active region and the matrices $F_{s,c}$ and $G_{s,c}$ will help calculate the optimal input value, $U_{dc}d(k)$, for the PWM modulation based on the updated state values of switch side inductor current/output capacitor voltage. $d(k)$ is the duty cycle ranged from 0 to 1.

The corresponding flow chart of the explicit MPC optimization process has been shown in Fig. 5(b). In each of the control period, when the control is enabled, MPC takes the input measurements of $i_L(k)$, $u_c(k)$, $i_g(k)$ and the reference of $u_{c,ref}(k)$ to find the active region s with the corresponding searching matrices $H_{s,c}$ and $K_{s,c}$. Finally, the optimal duty cycle is derived with the specific control law matrices of $F_{s,c}$ and $G_{s,c}$ for the PWM modulation.

E. Modular MPC Concept

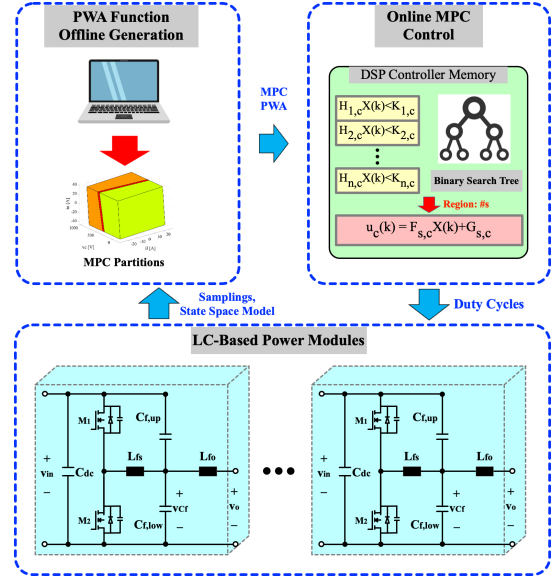
The proposed control structure is designed based on a modularized concept as is shown in Fig. 6. The whole control structure is composed of high level controller and local level MPC control modules. The high level controller is functioned as a central pivot to collect the ADC data from local modules, manage the converged branch power control, redistribute the power flow for local modules and generate voltage/current references for local modules. The local module focuses on the MPC control, ADC sampling and PWM modulation of LC

filtered switch leg. Thus, the reference commands are allocated to the local control modules and the ADC data are collected for the local and central controllers. The modular MPC concept enables a more general power converter control with random number of power modules to satisfy the topological and power rating requirements. For the topological requirement, the local MPC can be applied to single/three phase DC/AC or DC/DC converters. For the power rating requirement, the number of paralleled modules is adjustable with central controller to redistribute the power flow for local modules.

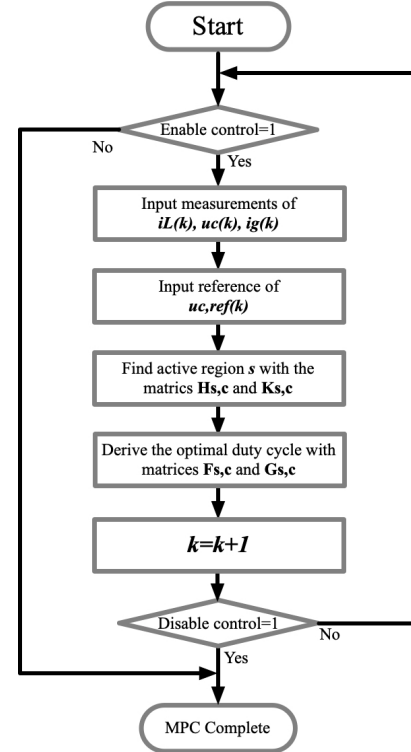
The differences between the proposed modular MPC and the traditional control methods can be summarized in three aspects. (1) Firstly, the accuracy of the proposed control is immune to the parameter uncertainty or mismatch of the grid side inductance. The developed control is a two-layer cascaded structure including the grid side inductor current PI control and the switch side LC filter capacitor voltage MPC control. No equivalent grid side inductance is needed for the parametric modeling which increases the accuracy of control. (2) Secondly, the formulation and code size of the proposed modular MPC is simplified. Since the developed MPC is implemented for each phase module of the switch side LC filter in a modular way, the dimensions of the state space matrices are smaller than the traditional three-phase formulations. The generated C code file for real time DSP experimentation is smaller which saves the required memory. The state space matrix of A is 2×2 which is smaller than 4×4 in [5] and 6×6 in [30]. The generated C code file for MPC implementation is only 5kB which is undemanding for a less costly DSP; (3) Thirdly, all static parameters for the state space matrices enable the offline generated explicit MPC algorithm and save the online execution time. Since the developed MPC is configured for per phase module of switch side LC filter, as is shown in equation (13a), the state space matrices are only composed of the static parameters of switch side inductance, L_{fs} , output capacitance, C_f , and control period, T_s . Different from the formulations of state space matrices in [5] and [30], no dynamic parameter, such as the grid angular velocity ω , is included in the state space matrices. A PLL controller is designed to provide the accurate grid angular velocity. Thus, leveraging the static LC parameters, the MPC can be implemented in an explicit way to derive the code offline and implement the optimal searching procedures online. The execution time can be saved for control with higher bandwidth.

IV. REGULATED THIRD HARMONIC INJECTION

A regulated third harmonic voltage injection (RTHI) method is proposed in this paper based on the zero voltage MPC to improve the DC bus voltage utilization [23]. Different from the conventional THI (Con-THI) in Fig. 7(a) to directly apply the third order sinusoidal waveform or triangular space vector component to the duty cycle for modulation, the proposed RTHI in Fig. 7(c) extracts the third order/triangular components from the central level grid side inductor current controller output after reversed Park transformation and add them to the zero-sequence voltage reference, $v_{dc}/2$, to formulate a new third-harmonic-based zero-sequence reference for the



(a) MPC optimization process.



(b) MPC flow chart.

Fig. 5. (a) MPC optimization process and the corresponding flow chart.

MPC. The main advantages of the proposed RTHI include: (1) As is shown in Fig. 4, the injection of third order/triangular components will be regulated by the MPC constraints before applying to the duty cycle of PWM. Thus, compared to the traditional direct duty cycle side injection methods, the stability and robustness of the system are improved. (2) By leveraging the proposed modified LCL converter to connect the capacitors common point to positive/negative DC bus

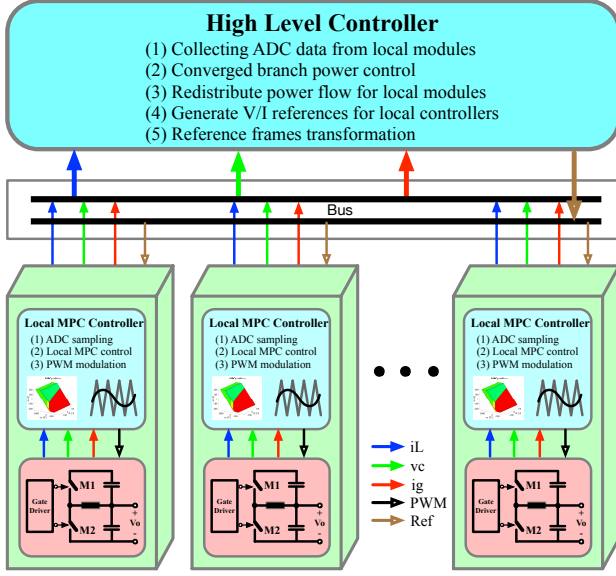


Fig. 6. Modular MPC concept structure.

in Fig. 1(b), the injected third harmonic components will be bypassed by the modified paths without flowing into the grid. Thus, the grid-connected power quality will be improved compared to the conventional THI methods. The third order sinusoidal (Sin-RTHI) and triangular space vector (Tri-RTHI) components injection methods are analyzed in this section.

A. Third Harmonic Sinusoidal Injection (Sin-RTHI)

The sinusoidal injection method is implemented by deriving the third order of grid fundamental frequency component to be superimposed to the zero-sequence voltage reference of MPC. The Sin-RTHI zero-sequence voltage reference for MPC can be expressed as:

$$v_{0,3rd}^* = v_{dc}/2 + V_m D_{3rd} \sin(3\omega t). \quad (21)$$

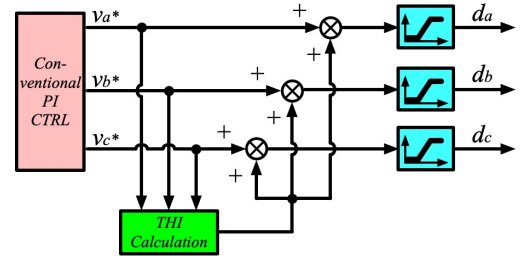
Thus, the abc frame Sin-RTHI three-phase capacitor voltage references, $v_{c,abc}^*$, distributed to the local MPC controllers can be expressed as

$$v_{c,a}^* = v_{c,a}^* + V_m D_{3rd} \sin(3\omega t) \quad (22a)$$

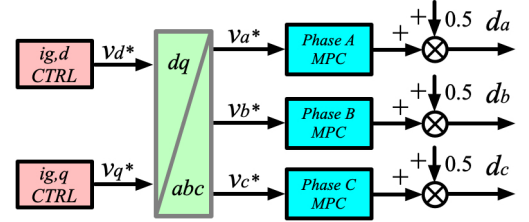
$$v_{c,b}^* = v_{c,b}^* + V_m D_{3rd} \sin(3(\omega t - \frac{2\pi}{3})) \quad (22b)$$

$$v_{c,c}^* = v_{c,c}^* + V_m D_{3rd} \sin(3(\omega t + \frac{2\pi}{3})). \quad (22c)$$

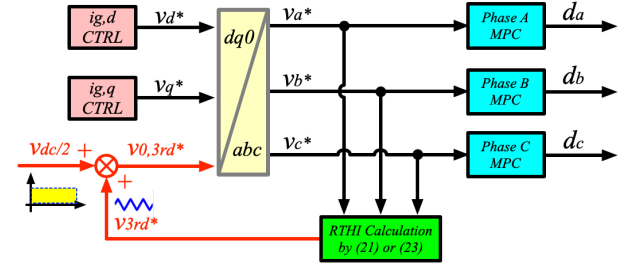
where V_m and D_{3rd} are the amplitude of fundamental component and third harmonic injection depth, respectively. The angular speed, ω , and phase shift can be derived based on the PLL controller. By leveraging the THI to the proposed zero-sequence voltage MPC as is shown in Fig. 7(c), the peak to peak capacitor voltage can be reduced to improve the DC bus utilization and avoid the duty cycle saturation in lower DC bus voltage. Fig. 8(a) shows the simulation waveforms of third order, fundamental frequency and injected capacitor voltages in one grid period.



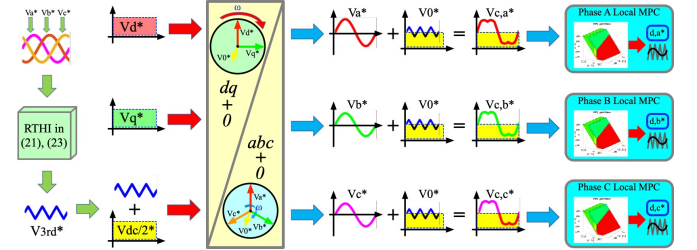
(a) Conventional THI.



(b) MPC without Zero-Sequence CTRL.



(c) Proposed RTHI.



(d) Detailed control diagram of zero sequence stabilized RTHI.

Fig. 7. (a) Conventional THI (b) MPC without zero-sequence control (c) proposed MPC-based regulated third harmonic injection methods and (d) the detailed control diagram of the MPC-based zero-sequence stabilized RTHI.

B. Triangular Space Vector Injection (Tri-RTHI)

The triangular space vector injection method is implemented by deriving the mean value of maximum and minimum grid fundamental frequency component capacitor voltage to be superimposed to the zero-sequence voltage reference of MPC. The Tri-RTHI zero-sequence voltage reference for MPC can be expressed as:

$$v_{0,3rd}^* = v_{dc}/2 - D_{3rd} [\max(v_{c,abc}^*) + \min(v_{c,abc}^*)]. \quad (23)$$

Thus, the abc frame Tri-RTHI three-phase capacitor voltage

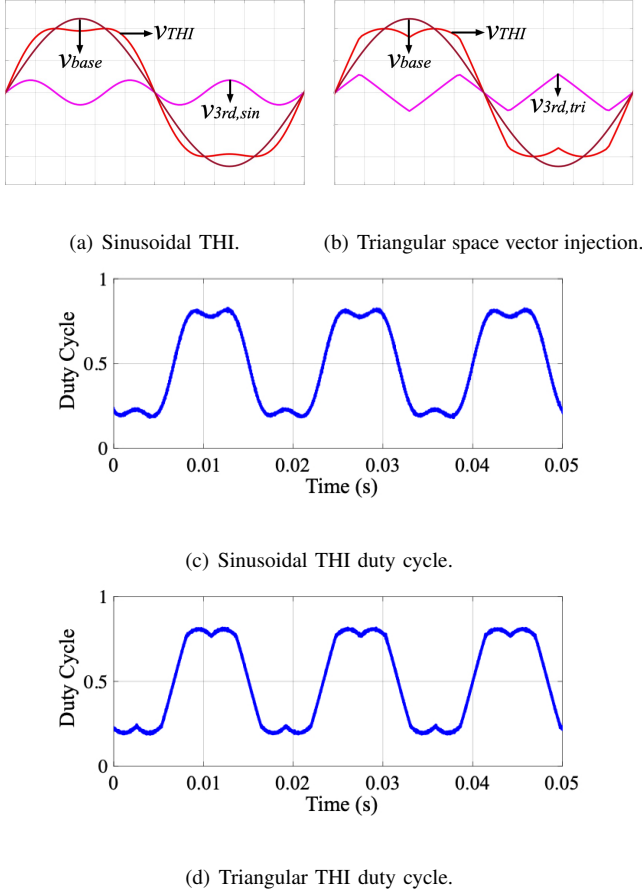


Fig. 8. (a) Sinusoidal THI (b) triangular space vector injection (c) sinusoidal THI duty cycle and (d) triangular THI duty cycle.

references, $v_{c,abc}^*$, distributed to the local MPC controllers can be expressed as

$$v_{c,a}^* = v_{c,a}^* - D_{3rd}[\max(v_{c,abc}^*) + \min(v_{c,abc}^*)] \quad (24a)$$

$$v_{c,b}^* = v_{c,b}^* - D_{3rd}[\max(v_{c,abc}^*) + \min(v_{c,abc}^*)] \quad (24b)$$

$$v_{c,c}^* = v_{c,c}^* - D_{3rd}[\max(v_{c,abc}^*) + \min(v_{c,abc}^*)]. \quad (24c)$$

As is shown in Fig. 8(b) of the triangular component injection, the DC bus utilization can also be improved to avoid the duty cycle saturation issue.

To evaluate the effectiveness of the THI in Fig. 7, a voltage gain can be defined as the ratio of the fundamental component capacitor voltage peak value, v_{base} , to the reference modulation waveform peak value, v_{THI} ,

$$G_v = \frac{v_{base}}{v_{THI}}. \quad (25)$$

The maximum voltage gain of the continuous THI methods can be derived at the $\pi/3$ when the third harmonic is at zero crossing point. Thus,

$$G_{v,max} = \frac{1}{\sin(\pi/3)} \approx 1.155. \quad (26)$$

By leveraging the proposed THI methods, the DC bus voltage can be reduced by a factor of 1.15 and the voltage stress,

switching losses on the power switches can be decreased, accordingly.

C. Advantages of Zero-sequence Controlled RTHI

The advantages of the zero-sequence controlled RTHI are addressed in this subsection. The comparison among the conventional THI, MPC without zero-sequence control, proposed MPC-based regulated THI and the corresponding detailed working mechanism is shown in Fig. 7. Compared with the conventional THI in Fig. 7(a), the developed method combines the references from zero-sequence control and the extracted third harmonics as the new reference for the per phase module MPC regulation. The regulated third harmonic injection provides more robust performance. Compared with the MPC method without zero-sequence control in Fig. 7(b) of the open loop DC offset, the proposed method stabilizes the zero-sequence voltage with desired reference based on the MPC feedback control loop instead of directly stepping up the duty cycle by 0.5. Thus, the zero-sequence control loop can operate in real time to regulate the measured zero-sequence value as the reference and attenuate the leakage current. The detailed working principle of the zero-sequence controlled RTHI is shown in Fig. 7(d). Different from the conventional THI in Fig. 7(a), the proposed RTHI methods extract the third order/triangular components from the central level grid side inductor current controller output after reversed Park transformation and superpose the third order/triangular components, v_{3rd}^* , with the zero sequence voltage reference, $v_{dc}/2$, as the new zero sequence reference for the local MPC to track. However, the conventional THI methods directly add the third order components onto the duty cycle for PWM modulation which brings two drawbacks: (1) The directly added third order components are from the output of PI controllers. No constraints and regulations are implemented before the third order components are pushed to the PWM modulation. Thus, compared to conventional THI, the proposed zero sequence stabilized RTHI is more robust and stable from the control perspective; (2) The conventional THI induces extra third harmonics to the grid with the traditional inverter topology which could deteriorate the power quality at PCC. The proposed zero sequence controlled RTHI combined with the proposed topology can bypass the third harmonics without injecting harmonics to the grid. The power quality will be improved automatically without extra optimization methods in [21] and [22] to reduce the THD at PCC. The zero-sequence and third harmonic components are demonstrated in the modified non-isolated three-phase converter systems with the corresponding flowing paths in Fig. 9. The injected third harmonics reduces the peak-to-peak output capacitor voltages without inducing harmonic distortions into the grid side.

V. RESULTS

The proposed method is validated experimentally on the non-isolated three-phase converter with grid simulator. The testing parameters are 450Vdc to 208Vac with switching frequency of 100kHz. The LCL filter parameters are $45\mu H$ for switch side inductor, L_{fs} , $12\mu F$ for upper/lower output

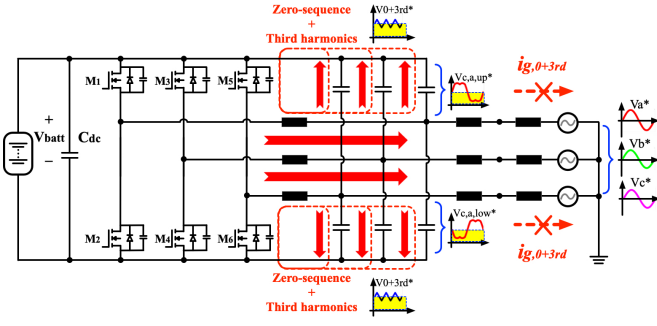


Fig. 9. The zero-sequence and third harmonics flowing paths in the non-isolated system.

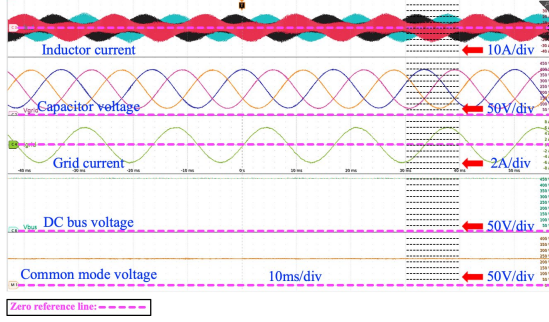
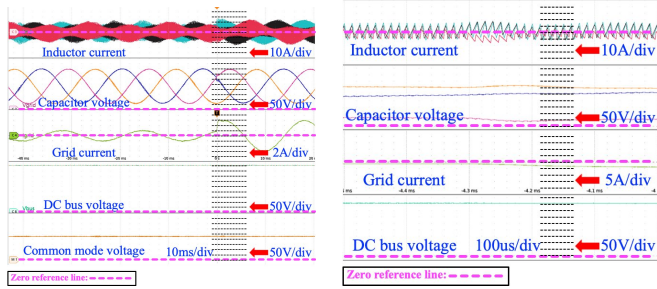


Fig. 10. The steady state waveforms.



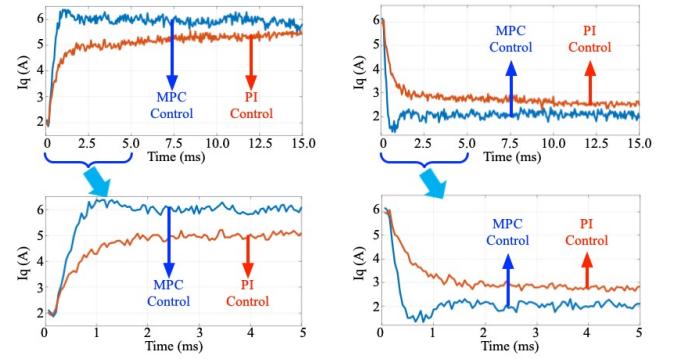
(a) Transient waveforms. (b) Zoomed transient waveforms.

Fig. 11. (a) Transient waveforms and zoomed transient waveforms.

capacitor, $C_{f,upper/lower}$, and $450\mu\text{H}$ for grid side inductor, L_{fg} . The power switches are C2M0025120D SiC from Cree with the gate driver of CRD-001. TMS320F28379D from TI is leveraged for the micro-controller. CKSR 25-NP and LV 25-P from LEM are utilized as the current and voltage sensors, respectively.

A. Steady State and Dynamic Performance Test

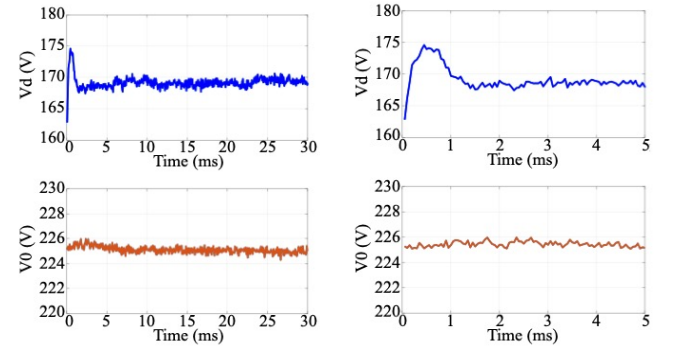
The steady state switch side inductor current, capacitor voltage, grid current and DC bus voltage with I_q of 6A are shown in Fig. 10. For the transient and zoomed waveforms of I_q step from 2A to 6A are shown in Fig. 11. The proposed modular MPC method captured ADC readings and the zoomed waveforms of I_q with a step from 2A to 6A and 6A to 2A are shown in Fig. 12(a) and Fig. 12(b), respectively. For the transient comparison, the 2A to 6A and 6A to 2A current steps with the conventional PI control method are also shown



(a) Transient from 2A to 6A.

(b) Transient from 6A to 2A.

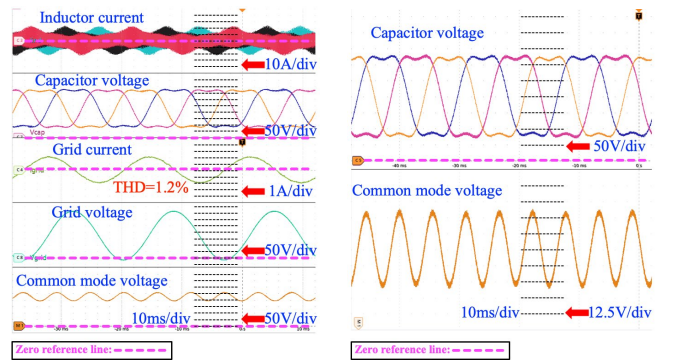
Fig. 12. Transient and zoomed waveforms comparison between the proposed modular MPC and conventional PI control methods with current steps of I_q from (a) 2A to 6A and (b) 6A to 2A.



(a) Transient of V_d and V_0 .

(b) Zoomed waveforms.

Fig. 13. (a) Transient and (b) zoomed waveforms of V_d and V_0 with V_d step from 160V to 170V.



(a) Sinusoidal RTHI waveforms.

(b) Zoomed waveforms.

Fig. 14. (a) Sinusoidal RTHI and (b) zoomed waveforms.

in the Fig. 12(a) and Fig. 12(b). The response time of modular MPC is 1ms and the conventional PI method is 15ms. Also, a grid voltage step performance of V_d from 160V to 170V is captured in Fig. 13.

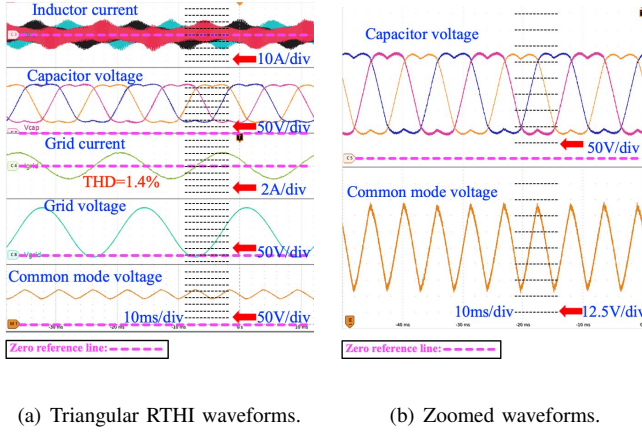


Fig. 15. (a) Triangular RTHI and (b) zoomed waveforms.

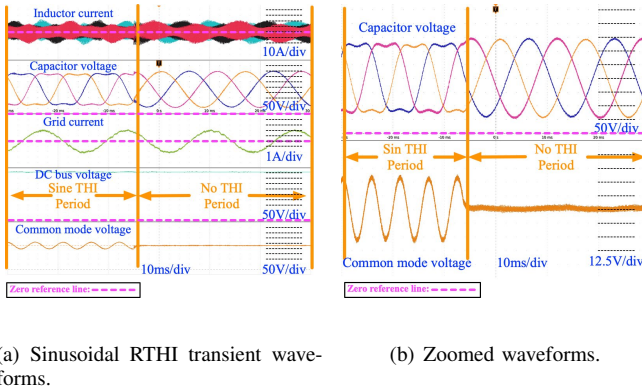


Fig. 16. (a) The transients from sinusoidal RTHI to constant zero-sequence voltage control and (b) zoomed waveforms.

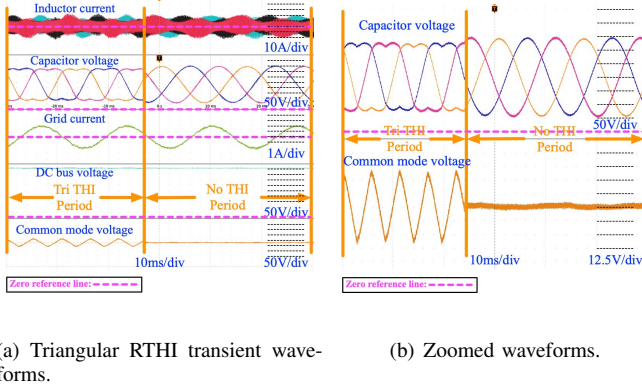


Fig. 17. (a) The transients from triangular RTHI to constant zero-sequence voltage control and (b) zoomed waveforms.

B. Third Harmonic Injection Test

The regulated third harmonic injection methods are validated in Fig. 14 and Fig. 15. Specifically, the sinusoidal RTHI in Fig. 14 achieves a voltage gain of 1.13 and the triangular RTHI in Fig. 15 achieves a voltage gain of 1.12, respectively. Also, the transient waveforms from Sin-RTHI and Tri-RTHI modes to constant zero-sequence voltage (Const- v_0) mode are shown in Fig. 16 and Fig. 17, respectively. The voltage gain, THD, third harmonic percentage of capacitor voltage, grid current/voltage and leakage current performance of the pro-

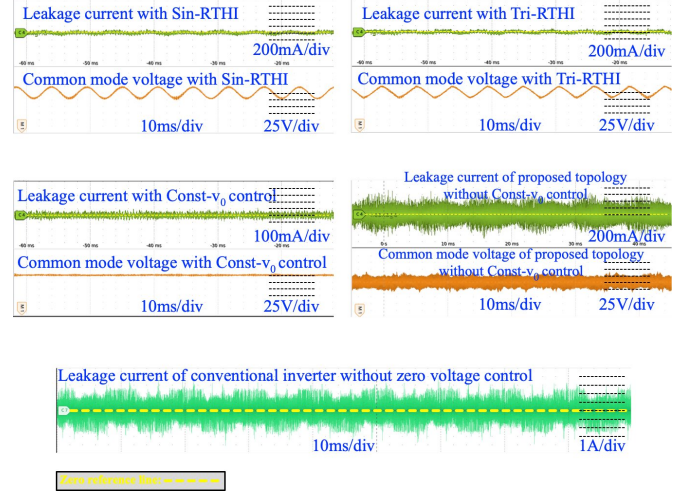


Fig. 18. The leakage currents and common mode voltages in Sin-RTHI, Tri-RTHI, Constant- v_0 , proposed topology without Constant- v_0 control and conventional modes.

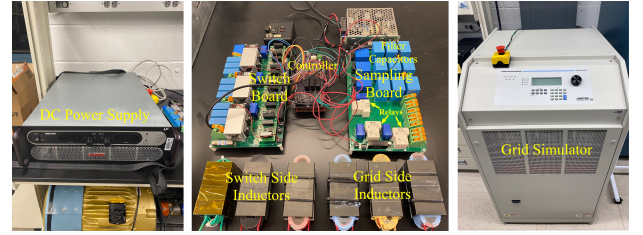


Fig. 19. The experimental prototype.

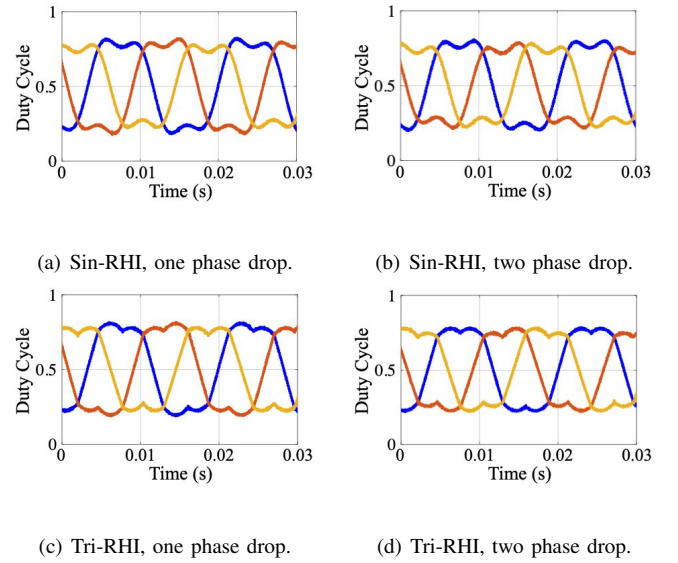


Fig. 20. (a) Sin-RHI, one phase voltage drops (b) Sin-RHI, two phases voltage drop (c) Tri-RHI, one phase voltage drops and (d) Tri-RHI, two phases voltage drop with the voltage drop of 20%.

posed Sin-THI, Tri-THI and Const- v_0 methods are compared with conventional THI (Con-THI) and no THI cases which are shown in table I. The proposed RTHI methods can improve the DC bus utilization by 12% to 13%. The grid current/voltage THD are maintained within 1.5% with the proposed RTHI with less than 3% of third harmonics to be injected to the

grid. However, the conventional THI method deteriorates the grid THD to be larger than 15% with more than 15% of third harmonics to be injected to the grid. Thus, compared with the Con-THI, the proposed RTHI methods can achieve maximum voltage gain with lowest grid current/voltage THD and minimum third harmonic components which means the RTHI can avoid the harmonics to be injected to the grid.

C. Leakage Current Test

The common mode voltage and leakage current waveforms of the Sin-RTHI, Tri-RTHI, Const- v_0 and non-THI are shown in Fig. 18. For the measurement of leakage current, as is shown in Fig. 1(b), the parasitic circuit of resistor and capacitor, R_{para} and C_{para} , are pre-designed to be connected between the DC bus terminal and neutral point of grid simulator. The typical values of the R_{para} and C_{para} are selected based on typical parasitic range between the automotive and photovoltaic systems [31], [32]. The prototype is shown in Fig. 19 with the converter, DC power supply and grid simulator. Also, the leakage current values are summarized in Table I. The zero-sequence voltage is controlled by the MPC to be half of DC bus voltage in Const- v_0 mode and with the injected third harmonic components in Sin-RTHI and Tri-THI modes. The leakage current are all limited to be within 15mA for the three modes which are 30 times lower than the conventional method. Thus, both the common mode voltage and current are compliant with the UL and IEC standard requirements. Also, to further study the independent effects of zero sequence voltage control and the modified topology on the reduction of leakage current, the leakage current and common mode voltage of the modified topology without zero sequence voltage control have been shown in Fig. 18 where the leakage current is 80mA. Thus, both the zero sequence voltage control and modified topology contribute to the leakage current reduction. The modified topology attenuates 5 times of the leakage current compared with the conventional topology. Furthermore, the zero sequence voltage control reduces another 5 times of the leakage current compared to the modified topology without zero sequence control case. The sinusoidal and triangular third harmonic injection methods only cause 0.6mA and 1.8mA more leakage current than the pure zero-sequence voltage control case. The two regulated THI methods both reduce 30 times of leakage current compared to the conventional THI and no THI cases.

TABLE I
THE COMPARISON OF PROPOSED AND CONVENTIONAL METHODS.

	Sin-RTHI	Tri-RTHI	Const- v_0	Con-THI	No THI
Topology	Proposed	Proposed	Proposed	Convent.	Convent.
G_v	1.13	1.12	1	1.11	1
THD_{vc}	15.3%	17.6%	2.3%	18.5%	2.5%
THD_{ig}	1.2%	1.4%	1.3%	17.4%	1.6%
THD_{vg}	0.93%	1.1%	0.91%	15.3%	1.2%
$vc_{3rd}\%$	10.2%	13.5%	1.5%	17.6%	1.8%
$ig_{3rd}\%$	2.1%	2.9%	2.7%	16.3%	2.6%
$vg_{3rd}\%$	1.6%	1.7%	1.5%	16.7%	1.2%
i_{lkg}	13.3mA	14.5mA	12.7mA	416mA	392mA

Besides the negligible influence on the leakage current, the impact of the regulated THI methods on the grid voltage and current is also small. According to the results shown in Table I, the grid voltage and current THD of Sin-RTHI and Tri-RTHI are all below 1.5% which are more than 10 times lower than the conventional THI method. For the high frequency noise in the proposed methods, it is caused by the switching frequency level fluctuation of 100kHz. The same frequency of noise also occurs in the conventional method testing cases but with higher peak-to-peak and RMS values compared with the proposed methods. The control algorithms of the proposed methods can be executed within $7\mu s$ which is enough to handle the switching frequency noise.

D. Parameters Mismatch and Variation Test

There exist a trade-off between offline explicit MPC with less computation burden and the corresponding possible tracking error caused by the parameter variations. To explore the influences of LC filter parameters variations on the control behavior, the mismatch between the MPC state space parameters and the physical LC parameters is manually adjusted in Table II. Three sets of cases have been tested including: (1) varying only the switch side inductance, L_{fs} , mismatch; (2) varying only the output capacitance, C_f , mismatch; (3) varying both the switch side inductance, L_{fs} , and the output capacitance, C_f , mismatch. Based on the testing results, the variations of offline pre-selected L_{fs} and C_f can affect the accuracy of MPC tracking. Applying the variations on both L_{fs} and C_f can cause more error than only applying variations on either L_{fs} or C_f . The largest possible error is 1.03% which occurs at a large mismatch of 60% on both L_{fs} and C_f .

For the influence of grid side inductance parameter on the control performance, since the local MPC is not leveraging this grid side inductance as the state space modeling, the per phase module of output capacitor voltage MPC tracking will not be affected by the variation of grid side inductance. The corresponding validation has been shown in Table III by manually adjusting the grid side inductance to check the influence on control performance. The tracking error is verified to be free from the variation of grid side inductance.

TABLE II
THE INFLUENCES OF SWITCH SIDE LC VARIATIONS ON MPC TRACKING.

L_{fs} Variation	Tracking Error	C_f Variation	Tracking Error	L_{fs}, C_f Variation	Tracking Error
60%	0.7%	60%	0.8%	60%	1.03%
40%	0.58%	40%	0.59%	40%	0.9%
20%	0.45%	20%	0.47%	20%	0.63%
0%	0.1%	0%	0.75%	0%	0.12%
-20%	-0.25%	-20%	-0.33%	-20%	-0.53%
-40%	-0.53	-40%	-0.63	-40%	-0.83%
-60%	N/A	-60%	N/A	-60%	N/A

TABLE III
THE INFLUENCES OF GRID SIDE L VARIATIONS ON MPC TRACKING.

Grid Side Inductance (μH)	4.5	18	45	180	450
Tracking Error (%)	0.25	0.21	0.18	0.14	0.12

E. Selective Design of Inductor and Capacitor

For the switch side inductor, the minimum inductance, $L_{f,min}$, can be determined by the maximum required current ripple, $\Delta i_{L,max}$, with the duty cycle of 0.5, d , switching frequency, f_{sw} , and DC bus voltage, V_{dc}

$$L_{f,min} = \frac{d(1-d)V_{dc}}{f_{sw}\Delta i_L}. \quad (27)$$

With the desired grid/switch side inductance determined, the capacitance can be designed by the minimum output voltage ripple, u_{ripple} and the resonant frequency of the LCL filter, ω_{res} . Specifically, the minimum capacitance is determined by the output voltage ripple which is expressed as

$$C_{f,up,min} + C_{f,lo,min} = \frac{1 - d_{min}}{8L_f u_{ripple}[\%] f_{sw}^2}. \quad (28)$$

Then, from the minimum available $C_{f,up,min}$ and $C_{f,lo,min}$, the value of capacitance can be adjusted to determine the resonant frequency of LCL filter system as is shown in

$$\omega_{res} = \sqrt{\frac{L_f + L_g}{L_f L_g (C_{f,up} + C_{f,lo})}}. \quad (29)$$

Based on (29), the capacitor values can be finally determined to choose a specific resonant frequency of the LCL filter. Then, with the help of ω_{res} and LCL parameters, the control bandwidth, ω_c , can be further designed to avoid the excitation.

F. Unbalanced or Weak Grid Analysis

Firstly, for the unbalanced grid conditions, the PLL will be affected to have more oscillation which could be reflected on the extraction of third order components as is shown in equations (21) and (22). Thus, the derived duty cycles can be influenced accordingly with the shifting of peak/valley points. The unbalanced conditions have been analyzed in Fig. 20 with four cases. Fig. 20(a) and 20(b) show Sin-RTHI with one and two phases voltage drop of 20%. Fig. 20(c) and 20(d) show Tri-RTHI with one and two phases voltage drop of 20%. The RTHI can still maintain stable operation with reduced peak-to-peak output capacitor voltage. Secondly, for the weak grid conditions, i.e. in a low short-circuit ratio (SCR), high impedance or low inertia constant microgrid, the robustness of the proposed regulated THI could contribute to the stable operation of the interfaced converter. As is shown in Fig. 7, different from the conventional THI method, the proposed RTHI utilizes the MPC to regulate the extracted third order component through zero-sequence controller before injecting into the PWM modulation. Thus, the robustness of operation, even in weak grid condition, can be improved.

VI. CONCLUSION

This paper proposes a modular model predictive control method for a novel non-isolated three-phase DC/AC converter with the capabilities of zero-sequence voltage stabilization and regulated third harmonic injection. The proposed non-isolated

topology is designed to connect the common point of three-phase LCL capacitors and positive/negative DC bus terminals to bypass the zero-sequence leakage current. The zero-sequence voltage MPC controller stabilizes the zero-sequence capacitor voltage to be a constant of half DC bus. Thus, the leakage current flowing through the grid is attenuated. The proposed regulated third harmonic voltage injection methods improve the DC bus utilization. By adding the third harmonic to the zero-sequence voltage MPC reference, the stability and robustness are improved. And compared to the traditional THI methods in the aspect of grid THD, the grid power quality is improved since no extra harmonics are injected to the grid and there is no need for optimization algorithm to reduce the grid THD. Per phase explicit modular MPC simplifies the execution complexity on DSP and does not need to update the angular speed in the state space matrix which makes it possible to implement the MPC optimization offline. Compared with the traditional PI controller, the proposed MPC improves the dynamic performance and control bandwidth with faster response. Compared with the traditional MPC controller, no grid side inductance value is needed for the two-layer cascaded control structure which both improves the dynamic performance from inner MPC loop and avoids the MPC parametric error caused by the uncertainty of grid side inductance.

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