Inductor Design for Non-Isolated Critical Soft Switching Converters Using Solid and Litz PCB and Wire Windings Leveraging Neural Network Model

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***Abstract*—High frequency (300kHz-1MHz) and high efficiency ($\geq 99.7\%$) inductor design method is proposed for the application of critical soft switching with large current ripple ($\triangle i_L \geq 200\%$) to improve the power density and efficiency of electrified energy conversion systems. Firstly for the theoretical design section, the core/coil size, number of turns, airgap, inductance are optimized using analytical model to minimize the inductor losses. Secondly for the structural design section of coil, a 3D routing method of litz PCB winding is developed to reduce the high frequency copper losses. The strand number, trace width, thickness and layout of litz PCB are analyzed in detail. Different types of coil, including solid/litz types of PCB/wire windings, are compared and analyzed based on the high frequency copper loss reduction and space utilization. For the structural design section of core, E and I cores are optimized to reduce the volume and core losses. Specifically, E-E, E-I, I-I and E-Air types of core structures are designed and compared considering the core loss, volume reduction and airgap limitation for the stack of turns. Two 4-layer neural network models are designed to analyze the AC losses of the proposed solid/litz PCB winding. The parameters of PCB winding can be optimized to reduce the inductor losses. Ten derived prototypes are built to benchmark between the proposed design and the commercial inductors. Power losses, temperature rise and cost are reduced by factors of 10, 2.5 and 3, respectively, with the proposed core and coil structures for the high frequency high current ripple critical soft switching applications.**

***Index Terms*—Inductor design, loss optimization, critical soft switching, litz PCB winding design, core structure design, neural network model.**

I. Introduction

ELECTRIFIED energy conversion systems especially for the electric vehicle and more electric airplane systems are developing towards the directions of higher power density, higher efficiency and lower cost. The key components of DC/DC and DC/AC power converters need to be carefully designed to achieve the goals. A promising method to increase the power density while reducing the losses is by leveraging the critical soft switching technique. It permits to increase switching frequency by a factor of 5 and reduce the required inductance by a factor of 20. Thus, the volume of filtering components can be decreased. However, a large current ripple is required for achieving critical soft switching operation with high frequency. Thus, the inductor needs to be carefully designed to handle large current ripple for the critical soft switching.

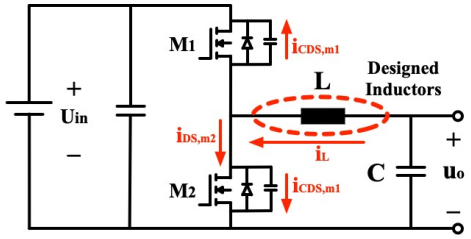
Inductor has been playing an essential role in the energy conversion system of DC/DC and DC/AC power converters to filter out the switching-frequency ripple. In a power converter circuit, the inductor accounts for a significant part of the total power losses. Especially for the application of high power, high frequency power converters with critical soft switching operation of large current ripple, the system efficiency is highly related to the electromagnetic performance of the inductor. Also, the volume of the inductor is crucial to the power density of the energy conversion system. Thus, the design and optimization of inductor for critical soft switching contributes to the efficiency and power density of the power converter.

Many references have studied and summarized the magnetic design procedures for power converters [1], [2], [3]. Also some advanced methods such as the Artificial Neural Network (ANN) [4], [5] or Fuzzy Logic [6] algorithms have been developed. However, there exist deviations between the theoretical analysis and assembled prototypes, especially in the high frequency/high power applications. The deviations are mainly caused by two factors. First is the structure and spatial layout differences of the core/coil. The topology of the core, winding method of the coil and even the distance among the conductors will bring differences on the performance of the inductor, such as inductance, flux density, copper/core losses, etc [7], [8]. Second is the high frequency electromagnetic behaviors of the coil excited by a high current ripple in the conductor. A high frequency current excitation will result in significant AC losses which may dominate the whole copper losses. This AC losses are caused by the skin and proximity effects of the conductors and are difficult to analyze theoretically [9]. This paper focuses on the structural optimization of core and coil to reduce the volume, cost and total losses especially considering the high frequency copper losses which is barely mentioned in many of the inductor design references.

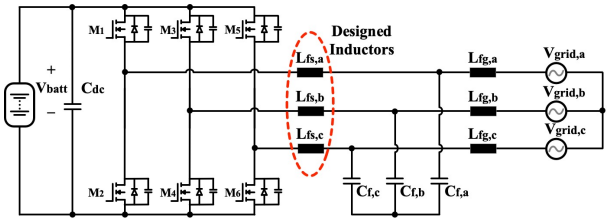
For the evaluation of inductor design, some key aspects need to be carefully considered such as the efficiency, volume, fabrication and cost. Firstly, for the efficiency, the inductor losses are mainly composed of core and copper losses. The core losses are caused by the alternating magnetization in a magnetic core which include hysteresis loss and eddy current loss [10]. The selection of core material influences the core losses. Ferrite core is a desired option for high frequency inductor design considering its low power loss density. Due to the large permeability, the air-gap is commonly added for a ferrite core to avoid saturation. Based on the targeted frequency range of 100kHz to 1MHz, ferrite core is selected for the core structure design of this paper. The copper losses are induced by the equivalent resistance of the winding. Using

thicker winding could reduce the resistivity of the conductor. Thus the DC copper losses will be reduced. However for the high frequency current excitations, the skin and proximity effects will result in significant AC losses. The litz type of conductor could be adopted for reducing the AC losses by winding multiple strands of conductors in parallel [11]–[16]. Specifically, [11] and [12] analyze the litz and solid types of round wire for the inductor thermal behavior. A preliminary litz PCB winding model was designed in [13] to reduce the AC resistance. [14] and [15] designed two-layer litz PCB inductors for domestic induction heating and wireless charging coil, respectively. However, multi-layer (>2) litz PCB winding has not been studied in depth which is addressed in this paper for a better AC resistance reduction. Secondly, for the consideration of volume and fabrication, different structures of the core are suitable for various winding method. Considering the PCB winding's convenience for manufacturing, fabrication and high space utilization, E cores with PCB windings can combine dense designs that can be mass-produced. Thirdly, for the cost, the litz wire cost more than the normal solid wire. However, if PCB is applied for the winding fabrication, the cost will be largely reduced when demanding a mass-production. So, this paper developed a litz type of PCB 3D layout to apply the litz conductor in PCB winding.

This paper is arranged as following. First part is the theoretical design procedures of inductor optimization. High current ripple/switching frequency requirements of critical soft switching are illustrated to specify the targeted application of the design. An iterative optimization method is developed to find the optimal number of turns, air-gap with the desired operating range of frequency for the reduction of total losses. The theoretical analysis will provide the guideline of structural inductor design. Second part is the structural design of core and coil. Based on the analysis in first part, the specific structures of core and coil are further optimized. For the coil, the high frequency AC losses are analyzed with the skin and proximity effects. A 3D litz PCB routing method is developed to emulate the twisted litz wire for the reduction of AC resistance. The ratio of AC to DC resistance, space utilization between multi-layer litz PCB and solid PCB are analyzed in detail. For the core, four types of core structure, E-E, E-I, I-I, E-Air (E-A) are developed based on the window/air-gap space and PCB winding parallelization. The trade-off of different core structures is illustrated with the combination of litz/solid PCB winding. Two 4-layer neural-network models are designed to analyze the AC resistance factor of the proposed solid/litz PCB winding. A generalized PCB-based inductor design method is developed leveraging the neural network model to reduce the losses. Finally, depending on the theoretical and structural design of core and coil, ten prototypes are finalized with different combination of E-E/E-I/I-I/E-Air cores and litz/solid PCB windings. The finalized prototypes are emphasized on different merits of the key factors for inductor design, such as losses, volume and cost, which could provide practical references for industrial inductor design with various trade off requirements. The experimental results verify the theoretical and structural analysis.



(a) DC/DC application



(b) Three-phase DC/AC application

Fig. 1. The inductor design for non-isolated (1) DC/DC and (2) three-phase DC/AC applications.

II. Theoretical Design

The designed inductor is targeted for critical soft switching converter operating at a high current ripple. The main purpose of the critical soft switching technique is to reduce the total switching losses by replacing the large turn-on loss of upper switch with small turn-off loss of lower switch. Critical soft switching permits to increase switching frequency by a factor of 5, and reduce the required inductance by a factor of 20. For the total losses of a non-isolated power converter, as is shown in Fig. 1(a) of a DC/DC converter or Fig. 1(b) of a three-phase DC/AC converter, the high current ripple inductor losses on the switch side account for a significant part of the power conversion losses. The critical soft switching method could be applied by adjusting the current ripple to certain values which requires the inductance to be designed within a certain range [17], [18], [19]. So the critical soft switching parameters and loss optimization for inductor design are performed in this section theoretically.

A. Critical Soft Switching Parameters

In a buck module of Fig. 1(a), the turn-on losses are much higher than the turn-off losses. A critical soft switching technique could be implemented to replace the large turn-on losses of the upper switch with small turn-off losses of the lower switch. The principle is to enlarge the current ripple on the inductor and make sure the peak/valley points of the inductor current is beyond certain threshold. Thus the current direction of the inductor is bidirectional and the soft switching turn-on of both switches will be guaranteed [20]. The soft switching waveforms during switching transient are illustrated in Fig. 2. Also, the soft switching turn-on transient of upper switch is shown in Fig. 1(a).

A negative current from the inductor is expected to fully discharge the output capacitor of upper switch before it is

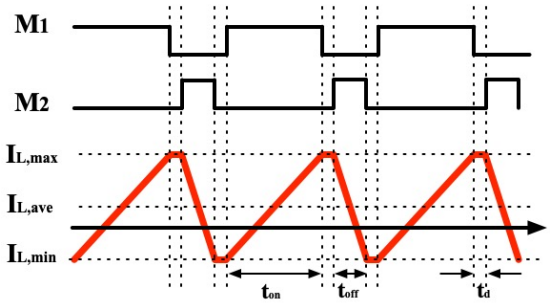


Fig. 2. Gate signals and inductor current for critical soft switching.

turned on [20]. Thus the large turn-on losses will be minimized by soft switching. So, the critical soft switching requirements of inductor current are

$$I_{L,peak} \geq I_{threshold} \tag{1}$$

$$I_{L,valley} \leq -I_{threshold}. \tag{2}$$

In the inductor design perspective of soft switching, the current ripple is the key parameter that will influence the inductance. And the soft switching requirements of peak/valley inductor currents limit the range of current ripple. For a general design application, both AC (60Hz) and DC currents are taken into consideration for the peak/valley inductor currents requirements of soft switching. The current ripple is the function of switching frequency, inductance and DC voltage

$$\Delta i_L = \frac{d(1-d)U_{in}}{f_s L}. \tag{3}$$

For DC current, the maximum inductance for soft switching can be derived accordingly as

$$L_{max,DC} = \min_{d_{min} \leq d \leq d_{max}} \frac{d(1-d)U_{in}}{2(|I_{L,ave}| + I_{threshold})f_s}. \tag{4}$$

For AC current, the most critical soft switching operating points of sinusoidal waveforms are the peak/valley points. The maximum inductance requirement is

$$L_{max,AC} = \min_{d_{min} \leq d \leq d_{max}} \frac{d(1-d)U_{in}}{2(\sqrt{2}|I_{L,rms}| + I_{threshold})f_s}. \tag{5}$$

According to equation (3), the switch side inductor current ripple is largely determined by the DC bus voltage. For the DC/DC converters in Fig. 1(a), the input and output voltage levels can be selected arbitrarily with the desired power and voltage requirements. However, for the three-phase DC/AC converter in Fig. 1(b), the DC bus voltage is generally depending on the grid voltage. The typical three-phase grid voltage for the US is line-to-line $480V_{L-L}$ which is line-to-neutral $277V_{L-N}$. And the DC side voltage should be at least twice higher than the AC grid voltage amplitude which is 783V. Since it is common to configure the DC voltage 10% higher than the AC voltage limit to avoid duty cycle saturation issue, we designed the DC bus voltage as 850V. For the current rating of switch side inductor design, a high power DC/AC converter power module with rated power of 11-13kW requires $16A_{RMS}$. And based on equation (5), the required maximum ripple current for the designed inductor to handle is 50A. And for the selection of winding gauge under soft switching operation, the equivalent RMS of current ripple is lower than 30A based on the the relationship of triangular current ripple peak-to-peak value, $I_{rms,triangle}$, and RMS value, $I_{rms,triangle}$: $I_{rms,triangle} = I_{p-p,triangle}/\sqrt{3}$. Thus, a gauge 8 wire is capable of handling 40A at 60 °C according to the AWG Table.

B. Iterative Optimization

The iterative optimization is based on the soft switching parameters of current ripple, minimum requirement of inductance, voltage level and power ratings for specific switching frequency. An inductor design optimization method is developed in this section to iteratively sweep the switching frequency and number of turns for finding the optimal inductor parameters. The theoretical analysis of the design procedure includes the core selection, coil design, air-gap adjustment and iterative searching for switching frequency and turn number.

1) Core selection: The core of the inductor is an essential part that is functioned for magnetization at specific frequency. The performance of the inductor is largely influenced by the core size and structure. Some key factors need to be considered for the selection of core: the core losses (including the hysteresis losses and the eddy current losses), the flux density saturation issues, the area product (AP) power capability checking.

The core size could be designed based on the AP power capability checking method [2]. The AP checking method has been developed to evaluate the power capability of the core based on the comparison of two values: electrical requirements of current and flux density, geometrical capability of the core, respectively. The electrical requirement, AP_e is related to the inductance, L, peak current, I_{pk}, peak flux density, B_{pk}, current density, J_{rms}, window utilization factor, K_u and can be expressed as

$$AP_e = \frac{LI_{pk}^2 10^4}{B_{pk} J_{rms} K_u}. \tag{6}$$

The geometrical capability of the core, AP_g is defined as the product of window area, W_a, and effective cross section area, A_c,

$$AP_g = W_a A_c. \tag{7}$$

In the iterative optimization procedure of inductor design, the AP checking is implemented in each round to check the power handling capability of the core for specific peak current, peak flux density and inductance. If the calculated AP_e is equal or less than the AP_g, the design parameters are regarded as effective. Otherwise, bigger core or combining more cores in parallel should be implemented to increase the core volume, V_{core}, and AP_g for the satisfaction of AP checking.

2) Coil and air-gap design: For the coil design of the inductor, the number of turns, N, combined with the air-gap, l_g, determines the inductance. The cross section area and the length of the coil conductor influences the copper losses. Thus, the number of turns, air-gap and cross section area are the three key factors that need to be considered in coil design [21], [22].

In an air-gaped inductor, the inductance could be derived as

$$L = \frac{4\pi N^2 A_c 10^{-4}}{l_g + (L_{MPL}/\mu_r)} F_{fringe} \tag{8}$$

where L_{MPL}, μ_r are the magnetic path length, relevant permeability and F_{fringe} represents the fringing effect that can be expressed as

$$F_{fringe} = \frac{l_g}{\sqrt{A_c}} ln(2W_h/l_g) + 1 \tag{9}$$

where W_h is the window height.

The total losses of the inductor, P_{total}, are composed of core losses, P_{core}, and copper losses, P_{copper}. And the copper losses are the sum of DC losses, P_{DC}, and AC losses, P_{AC} [23]

$$P_{total} = P_{core} + P_{copper} = P_{core} + P_{DC} + P_{AC}. \tag{10}$$

The core losses are calculated by the Steinmetz's equation with frequency, f_{sw}, peak flux density, B_{pk}, and the coefficients, a, b and k

$$P_{core} = k \cdot f_{sw}^a \cdot B_{pk}^b. \tag{11}$$

The peak flux density, B_{pk}, is expressed with the turn number, N, peak inductor current, I_{pk}, magnetic path length, L_{MLT}, and permeability, μ_r,

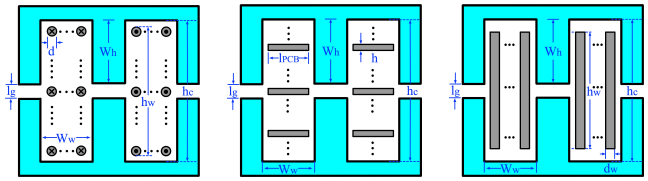
$$B_{pk} = \frac{4\pi N I_{pk} 10^{-2}}{l_g + (L_{MPL}/\mu_r)}. \tag{12}$$

The copper losses can be derived in detail as

$$P_{copper} = (I_{DC}^2 + I_{AC,rms}^2) R_{DC} RF \tag{13}$$

where $I_{DC,rms}$ and $I_{DC,rms}$ are the DC and AC components of RMS currents. R_{DC} is the DC resistance which is relevant to the mean length per turn, L_{MLT}, number of turns, N, cross section area, A, and resistivity, ρ, of the coil conductor in (14). RF is the ratio of AC and DC resistance called resistance factor. However, the AC resistance, $R_{AC} = R_{DC}RF$, is a much more complex variable that depends on the frequency, coil structure and routing method and will be analyzed in next section.

$$R_{DC} = \frac{\rho N L_{MLT}}{A} \tag{14}$$



(a) Wire coil (b) PCB coil (c) Foil coil

Fig. 3. The distribution of wire, PCB and foil coils in E core window.

3) Turn number and air-gap adjustment: The adjustments of turn number and air-gap mainly aim at avoiding saturation and tuning the inductance as is shown in (8) and (12). In the optimization procedure of inductor design, the number of turns are swept from the maximum allowable value to find the minimum inductor losses. In the mean time, the air-gap is adjusted accordingly to maintain a desired inductance. The maximum allowable turn number, N_{max}, is restricted by the window area, W_a, and the cross section area of the coil conductor. The derivation of N_{max} is different for the wired coil and PCB coil in Fig. 3. For the wired coil with diameter of d

$$N_{wire,max} = \frac{W_w}{d} \frac{(2W_h + l_g)}{d}. \tag{15}$$

For the PCB coil with thickness of h and length of l_{PCB}

$$N_{PCB,max} = \frac{W_w}{l_{PCB}} \frac{(2W_h + l_g)}{h}. \tag{16}$$

For both wired and PCB coil inductors in (15) and (16), W_w and W_h are the window width and height, respectively.

4) Iterative Searching: For the iterative searching of the inductor optimization, the number of turns is swept to find the minimum inductor losses at each operating point of desired switching frequency. Specifically, at each frequency point, the turn number is swept from the largest allowable value to find the optimal turn number for minimum inductor losses while checking the saturation issue of the flux density. Thus, at each frequency value, the optimal values of turn number, airgap, core/copper losses, inductance and peak flux density are derived for the following sections of structural design. The theoretical design algorithm of flow chart is shown in Fig. 4. The theoretical inductor optimization is calculated based on the high frequency high power critical soft switching converter with the parameters in table I where the switching frequency is swept from 100kHz to 1MHz. At each switching

TABLE I
HIGH FREQUENCY HIGH POWER INDUCTOR DESIGN PARAMETERS

Parameter	Values
DC bus voltage	850V
AC RMS current	16A
AC current ripple	50A
Switching frequency range	100kHz-1MHz
Core volume	0.011L
Winding gauge	AWG8

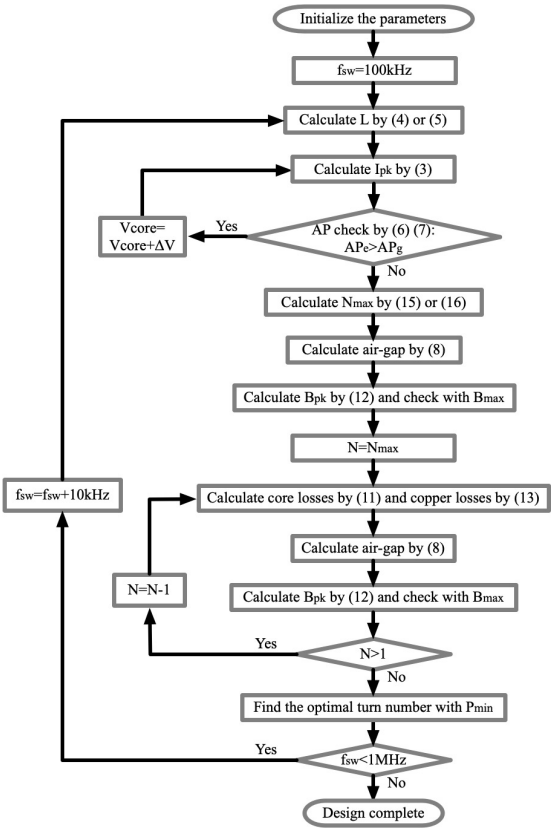


Fig. 4. Round wire winding inductor design flowchart.

frequency point, the optimal turn number, airgap, inductor losses, inductance and peak flux density are derived to achieve the minimum inductor losses. The E42/21/20-3F36 from Ferroxcube is chosen as the core cell which is a kind of ferrite material. It is a medium to high frequency power material suitable for a frequency ranged from 500kHz to 1MHz. And it has low power loss density at a wide temperature range from 25 to 100 °C. The design algorithm is aimed at optimizing the inductor parameters at every specific frequency point. And the maximum frequency point (1MHz) could be chosen as the most strict condition which will be feasible to be applied to any of the lower frequency range without violating the B_{max} and AP checking. Specifically, the turn number, air-gap, inductance at 1MHz could be picked as the optimal parameters to operate in the lower frequency ranges. The optimization results of inductor design parameters at 1MHz are shown in table II.

TABLE II
THEORETICAL INDUCTOR DESIGN RESULTS AT 1MHZ

Parameter	Values
Frequency	1MHz
Turn number	10
Air gap	1.38 cm
Core loss	15.3 W
Copper loss	24.1 W
Inductance	4.1 μH
Peak flux density	0.2 T

III. STRUCTURAL OPTIMIZATION

The geometrical structure of the inductor is an essential part that will influence the electrical and magnetic performances. This section covers both the coil structure and core geometrical topology. Specifically, for the coil structure design, different types of coil including litz PCB, solid PCB, litz wire, solid wire are taken into account for the considerations of high frequency AC losses, space utilization. A 3D litz PCB routing method is developed for PCB application of litz wire. For the core geometrical topology design, three types of core structures, E-E, E-I and I-I cores are analyzed and compared based on the window area and air-gap for the coil space utilization. Finally, considering different merits of trade off, three optimal prototypes are derived, fabricated and validated.

A. Coil Structure Design

The high frequency AC losses are analyzed in a solid coil conductor. For the reduction of AC losses, a 3D litz PCB routing method is developed with n layers of PCB board to emulate the litz wire. The comparison of litz and solid PCB coil is derived with high resolution FEA simulation.

1) High frequency AC loss analysis: The copper losses are generated by the coil conductor which include DC losses and AC losses as is shown in (13). The DC, AC rms currents and DC resistance, $I_{DC,rms}$, $I_{AC,rms}$ and R_{DC}, could be directly derived mathematically. However, the AC resistance, R_{AC}, is complicate to derive theoretically, especially in the high frequency applications. The Dowell's equation could be applied to estimate the AC resistance [9], [23], [24], [25]. To analyze the AC losses of the conductor geometrically, the traditional coil structure could be mainly divided into rectangular foil solid conductor, round wire solid conductor and round wire litz conductor. The complexity of estimating the AC resistance results from the factors of skin effect and proximity effect.

The skin effect is induced by the internal current of the conductor which generates a magnetic field that makes the current density lower in the center and higher in the surface. On the other hand, the proximity effect is induced by the adjacent conductors that produce magnetic fields and influence the current density distribution: higher in the outer wire and lower in the inner wire. Thus, both the skin and proximity effects will distort the current density distribution of the conductor and the AC resistance will be increased by the rise of frequency.

In PCB solid winding conductor, the AC resistance can be derived in (17) as

$$\begin{aligned} R_{AC,PCB} &= R_{skin} + R_{prox} \\ &= \frac{L_{PCB}}{2\sigma W h}\left(\frac{h}{\delta}\right)\frac{sinh(h/\delta)+sin(h/\delta)}{cosh(h/\delta)-cos(h/\delta)} + \frac{1}{12}hw^2\sigma B_n^2 W^3 \end{aligned} \tag{17}$$

where $L_{PCB}, h, W, \delta, \sigma, w, B_n$ are the length, thickness, width, skin depth, conductivity, angular frequency, average external magnetic field of the PCB winding.

In rectangular foil solid conductor, the AC resistance can be derived in (18)

$$R_{AC,foil} = \frac{l_w m}{\delta \sigma h_w}[\zeta_1^{'} + \frac{2}{3}\eta_w^2(m^2-1)\zeta_2^{'}] \quad (18)$$

where $\zeta_1^{'}$ is the skin effect factor

$$\zeta_1^{'} = \frac{sinh(2\Delta^{'}) + sin(2\Delta^{'})}{cosh(2\Delta^{'}) - cos(2\Delta^{'})} \quad (19)$$

and $\zeta_2^{'}$ represents the proximity effect factor

$$\zeta_1^{'} = \frac{sinh(\Delta^{'}) - sin(\Delta^{'})}{cosh(\Delta^{'}) + cos(\Delta^{'})}. \quad (20)$$

$\Delta^{'}$ is the revised penetration ratio and is expressed as

$$\Delta^{'} = \sqrt{\frac{h_w}{h_c}}\frac{d_w}{\delta}. \quad (21)$$

$m, \delta, l_w, \sigma, h_w, h_c, d_w$ are the layer number, skin depth, layer mean length, material conductivity, layer width, core window size and foil conductor thickness, respectively.

In round wire solid conductor, the AC resistance can be derived based on the Dowell's equation in (22)

$$R_{AC,wire} = \frac{l_w m N}{\delta\sqrt{\pi/4}d}[\zeta_1^{'} + \frac{2}{3}(\frac{\sqrt{\pi/4}dN}{h_w})^2(m^2-1)\zeta_2^{'}] \quad (22)$$

where d, N are the diameter and turn number of the round wire solid coil.

The mathematical calculation for PCB, foil and round conductor AC resistance are based on the parameters in Fig. 3.

The AC resistance is highly relevant to the frequency of the current excitation and a higher frequency will result in a thinner skin depth, δ, which is derived by resistivity, ρ, switching frequency, f_{sw}, and permeability, μ

$$\delta = \sqrt{\frac{\rho}{f_{sw}\pi\mu}}. \quad (23)$$

This skin depth, δ, will affect the revised penetration ratio, $\Delta^{'}$, in (21) and thus influence the skin and proximity effect factors, $\zeta_1^{'}, \zeta_2^{'}$, in (19) and (20). Finally, the AC resistance will be increased with the rise of frequency as is shown in (18) for foil conductor and (22) for round conductor, respectively.

Due to high AC resistance of solid conductor, the AC copper losses could be increased significantly in high switching frequency power converter filtering system. The resistance factor RF, defined as the ratio of AC and DC resistance, can be applied to describe the performance of copper losses for specific coil.

$$RF = \frac{R_{AC}}{R_{DC}} \quad (24)$$

According to (18) and (22), the penetration ratio, switching frequency and number of turns/layers are the dominating factors that affect the resistance factor. A typical option to eliminate the AC resistance is by replacing the round solid wire with litz wire. Litz wire is fabricated by twisting multiple stranded wires to reduce the skin and proximity effects. For the skin effect, because each strand has much smaller cross section area, the influence of skin depth turns to be negligible compared to the current conducting diameter. For the proximity effect, the evenly distributed spiral strands could counteract the magnetic fields in adjacent strands. So, the proximity effect will be largely reduced. Thus, in strand level of each bundle, both skin and proximity effects are decreased effectively with litz structure. For stacked layers or multiple turns of the coil, the bundle level skin and proximity effects could also result in extra AC losses due to the adjacent bundles of wire. Despite of the bundle level effect, the litz wire is superior than solid wire in the aspect of AC losses.

In litz winding conductor, the AC resistance can be derived as [26]

$$R_{AC,litz} = \frac{4l_w m N\zeta}{\sqrt{2}n_s\sigma\pi d_s^2}[\psi_1(\zeta) - \frac{\pi^2 n_s p_f}{24}(16m^2 - 1 + \frac{24}{\pi^2})\psi_2(\zeta)] \quad (25)$$

where $m, N, l_w, n_s, d_s, \zeta$ are the layer number of the winding, turn number of litz wire per layer, number of strands per bundle and strand diameter, respectively. The variables of $\psi_1(\zeta)$ and $\psi_2(\zeta)$ are the skin effect and proximity effect losses which are expressed as Bessel functions and can be derived by a Talyor-series expansion [26]

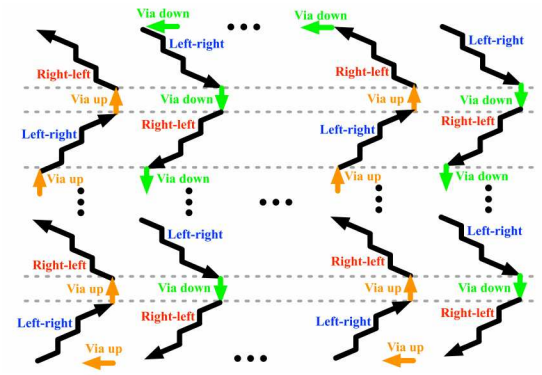
$$\psi_1(\zeta) = 2\sqrt{2}(\zeta + \frac{1}{32^8}\zeta^3 - \frac{1}{32^{14}}\zeta^5 + ...) \quad (26a)$$

$$\psi_2(\zeta) = 0.5\sqrt{2}(-\frac{1}{2^5}\zeta^3 + \frac{1}{2^{12}}\zeta^7 + ...). \quad (26b)$$

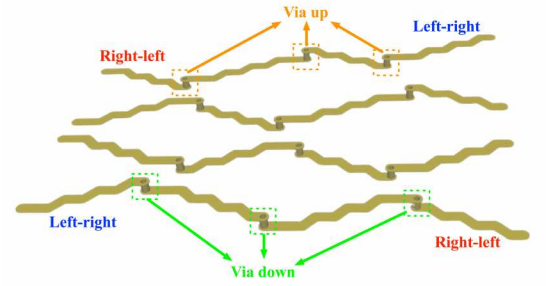
2) 3D litz PCB routing method for AC losses reduction: Although litz wire could reduce the AC losses significantly, the cost and insulation restrict the litz wire from wide application because each strand of the bundle inside the litz wire needs to be insulated. On the other hand, the PCB winding has the merits of inherent insulation capability, convenience of assembly and high window space utilization. This paper develops a 3D litz PCB routing method to combine the advantages of both litz wire and PCB winding. The method is designed by applying the litz structure of round twisted wire to PCB routing for multiple layers.

The 3D routing method is aimed at emulating the twisted litz wire by following two principles: (a) Each of the strand in the PCB board should go through all the layers evenly and spirally to counteract the adjacent magnetic field; (b) The length of each strand should be equivalent to avoid uneven magnetic field among different strands.

Thus, a routing method is implemented in Fig. 5 which could be extended and applied to arbitrary number of strands and layers for a better emulation of round litz wire. Specifically, starting from the top-right corner of the figure, each strand will be spirally and evenly routed through all layers of the PCB board. To achieve this goal, the litz PCB is composed of six types of routing modes: left-right, right-left, external-via-up, external-via-down, internal-via-up, internal-via-down. The left-right and righ-left modes are the wires that are routing directly from side to side of certain copper layer. The external-via-up and external-via-down are the vias that are distributed



(a) 3D litz PCB coil routing method.



(b) 3D example of the separated litz PCB routing.

(c) 3D example of the integrated litz PCB routing.

Fig. 5. (a) 3D litz PCB routing method, 3D view of (b) separated and (c) integrated routing example.

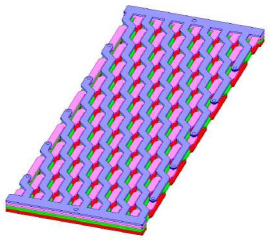
on both sides of PCB edges to connect between adjacent copper layers. If more than 4 layers are designed for the PCB, the internal-via-up and internal-via-down will be added which are the vias distributed inside the PCB away from the edges to connect between adjacent copper layers.

3) Litz PCB design procedure: Based on the 3D litz PCB routing method, a specific litz PCB winding design procedure is shown in this subsection which includes the routing method, copper thickness, strand number, trace width and layer number.

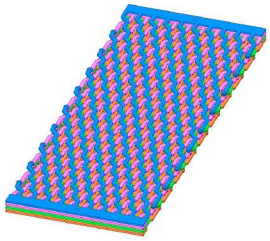
Firstly, the thickness of the PCB copper layer, t_{PCB}, is designed according to the skin depth equation in (23). To avoid the conductor being influenced by the skin effect from both top and bottom surfaces of the PCB winding, the thickness of copper trace should be less than twice of the skin depth

$$t_{PCB} \leq 2\delta. \tag{27}$$

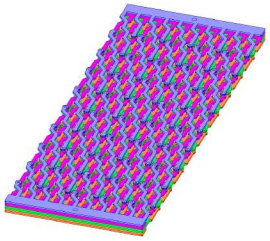
The targeted maximum switching frequency is 1MHz. Given the resistivity of copper and the targeted maximum switching frequency, the skin depth is calculated as 0.0652mm. So, the thickness of the PCB copper layer should be less than twice of the skin depth which is 0.1304mm. Because the



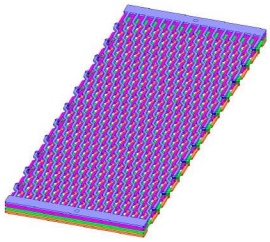
(a) Litz PCB 4×7 Strands, 16mils trace width.



(b) Litz PCB 4×10 Strands, 8mils trace width.

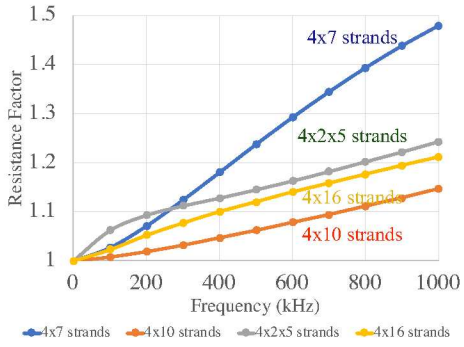


(c) Litz PCB 4×2×5 Strands, 8mils trace width.

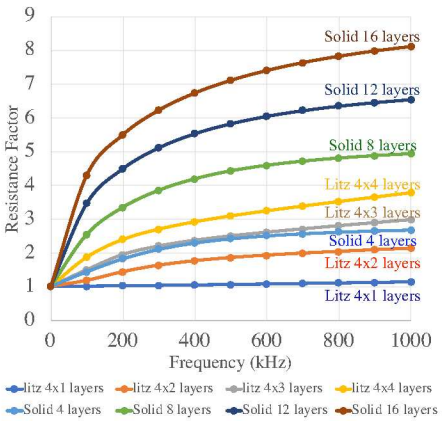


(d) Litz PCB 4×16 Strands, 5mils trace width.

Fig. 6. Four types of litz PCB routing structures with different strand number and trace width.



(a) Four types of designed litz PCB structures.



(b) Stacked litz and solid PCB.

Fig. 7. Comparison of resistance factor with different frequencies (a) for a single PCB with different combinations of strand number and trace width (b) for different stacked number of the desired 4x10 strand type of litz PCB and solid PCB structures.

fabrication of PCB copper thickness is measured with ounce, 3oz (0.1067mm) is the most satisfied thickness option.

Secondly, the number of strand, N_s, and trace width per strand, W_s, are the two key parameters that need to be designed. These two parameters influence the proximity effect and window space utilization. A suitable combination of strand number and trace width could result in lower resistance factor thus lower AC losses, especially, when multiple layers of PCB need to be stacked for the coil fabrication. Theoretically, the more number of strand and the thinner trace width, the less AC resistance will be induced. However, there exist the restriction of PCB minimum trace width and window space utilization. The minimum trace width per strand is restricted by the minimum diameter of the via hole, $d_{h,min}$. The minimum spacing between adjacent strands in the same layer is restricted by the minimum outer diameter of the via, $d_{v,min}$. And the number of strands per layer will be defined by the core window width, W_w, strand trace width, W_s, and trace spacing, S_t. The combination of (N_s, W_s) could be designed iteratively starting from the minimum requirement of via size and window width to find the optimal resistance factor

$$(N_s, W_s)_{optimal} = \underset{(N_s,W_s)}{\operatorname{argmin}} RF(N_s, W_s, S_t) \tag{28}$$

where N_s ranges from 0 to $W_w/(d_{h,min}+d_{v,min})$. The strand number could be swept with a certain step to iteratively find the optimal resistance factor with reasonably tuned values of strand width and trace spacing.

The core E42/21/20 with a window width of 9mm from Ferroxcube is taken as an example for the design of litz PCB winding. Four types of routing structures with different strand number and trace width are designed and simulated with high resolution FEA analysis in ANSYS. The PCB is set to be four layers with different combinations of (strand number, trace width) as is shown in Fig. 6: (4×7 Strands, 16 mils), (4×10 Strands, 8 mils), (4×2×5 Strands, 8 mils), (4×16 Strands, 5 mils). In each of the subfigure, a small length of four-layer litz PCB routing structure is shown and the current is expected to flow from left-bottom of the input terminal to the right-top of the output terminal.

From Fig. 6(a) to 6(d), the strand number is increased from 28 to 64. Accordingly, due to the core window width limitation, the trace width per strand is reduced from 16 mils to 5 mils. Specifically, in Fig. 6(a), 6(b) and 6(d), the single bundle types of spirally twisted litz PCB are designed with different strand numbers. Also, in Fig. 6(c), 5 bundles of strands are twisted respectively and connected in parallel as a whole in which each bundle has 8 strands. The AC losses and resistance factors of the four structures are listed in Table III and Fig. 7(a) to analyze the skin/proximity effects on the proposed litz PCB. From the illustrated results, the (4×10 Strands, 8 mils) litz routing structure has the smallest resistance factor which is more suitable for the high frequency application especially when stacking multiple PCB boards to form a specific number of turns for inductor winding.

TABLE III
HIGH FREQUENCY BEHAVIOR COMPARISON OF LITZ PCB

Parameter	4×7	4×10	4×2×5	4×16
AC loss (mW) @60Hz	108.4	154.1	154.9	149.4
AC loss (mW) @500kHz	134.1	163.4	177.5	167.4
AC loss (mW) @1MHz	160.4	176.5	192.5	181
RF=Rac/Rdc (pu) @500kHz	1.24	1.06	1.15	1.12
RF=Rac/Rdc (pu) @1MHz	1.48	1.14	1.24	1.21

The via to be applied in the litz PCB winding design is hollow type with outer and inner diameters of 12mil and 6mil, respectively. The high frequency loss model of the via is also built with ANSYS to analyze the impact of via on losses. The loss per via at 500kHz, 25A current is 25.63μW. For a piece of litz winding, there are totally 54 vias including 10, 8 on the two shorter sides, 18 on both longer sides. They are connected in parallel within each side and in series among the four sides. Thus, the total losses induced by the via is 8.61μW which is 0.005% of the litz PCB AC losses and can be neglected.

4) Litz PCB vs. solid PCB: Considering the final inductor prototype, multiple turns of coil requires the litz PCB to be stacked for multiple layers. Thus the proximity effect will dominate the copper losses and the resistance factor will be increased with the stacked layer number. In this subsection, the litz PCB is compared with solid PCB coil in the aspects of copper losses and resistance factor at different frequency. Also, the number of stacked PCB layers are taken into account for the AC resistance analysis. Based on the results in Fig. 7(a), (4×10 Strands, 8 mils) litz routing structure is chosen as the optimal litz winding solution for the core of E42/21/20 due to the least resistance factor. Also, a solid PCB winding layer with the same 3D sizes as the litz PCB layer is selected for comparison. To analyze the resistance factor performance of different number of stacked solid or litz PCB layers, 4, 8, 12 and 16 layers of litz and solid PCB windings are simulated with the same current excitation under different frequencies. The resistance factors of the 8 types of PCB winding cases are plotted in Fig. 7(b) with frequency ranged from 100 kHz to 1 MHz. The results show that the designed litz PCB winding structure has 2 to 3 times lower resistance factor than the solid PCB at the same number of stacked layers. Thus, the AC copper losses of the litz PCB is lower than the solid PCB proportionally. For the E core setup, the 3D view of the proposed 4 layer litz PCB winding and the top views of each layer are shown in Fig. 8 and 9, respectively. What is noteworthy is that the four right angle corners of the litz PCB layout are designed as solid structure because the principle of litz routing requires the length of each strand to be equivalent to avoid uneven magnetic field. The solid design of winding corners guarantees that all the traces between two solid corners have the same length despite the diagonal lines may reach the edges. Since whenever a trace reaches the edge, the via will help the trace switch the layer and go towards another symmetric diagonal direction. For the terminal of the traces in Fig. 8 and Fig. 9, solid terminal pads and castellated holes are designed to connect among PCB winding boards. These castellated holes help to mount one PCB windng board on top of another during assembly. Such holes provide proper alignment between the winding boards while soldering. Thus, the terminal pads and castellated holes contribute to the

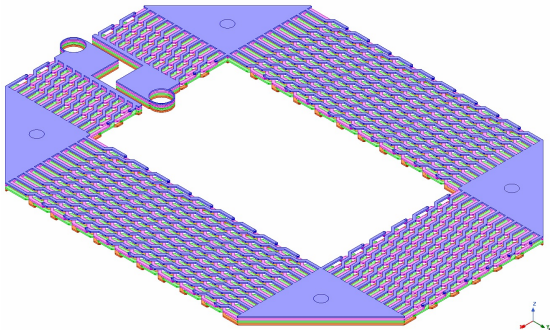
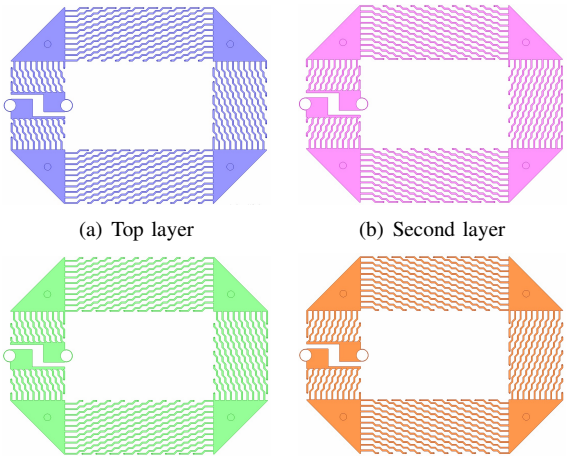


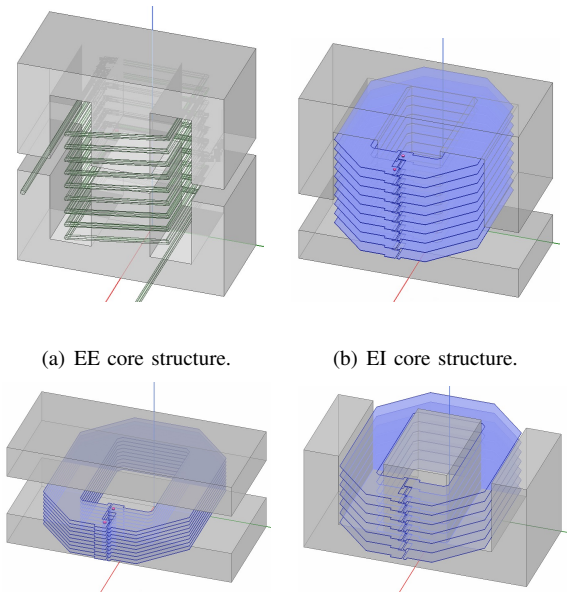
Fig. 8. 3D view of a four layer, 40 strand litz PCB design.



(a) Top layer (b) Second layer

(c) Third layer (d) Bottom layer

Fig. 9. Four layers of litz PCB design in top view.



(a) EE core structure. (b) EI core structure.

(c) II core structure. (d) EA core structure.

Fig. 10. Four types of core structures.

balancing of winding length for every turn.

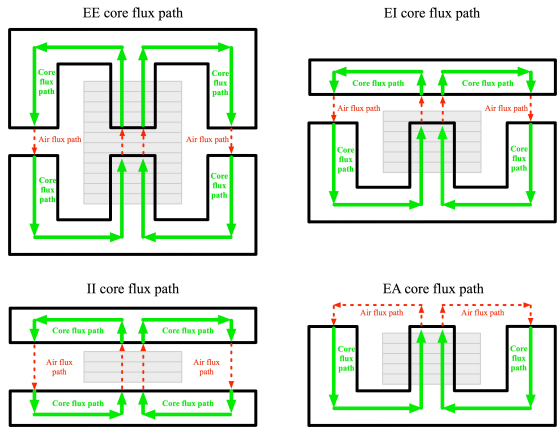


Fig. 11. The analysis of magnetic flux paths for different core structures.

B. Core Structure Design

This section discusses the core structure design based on the E core topology which is convenient for combined fabrication with PCB winding. A commercially available E core cell of E42/21/20 is used for the core structure design which is consistent with the theoretical design of core selection. Four types of core structures are developed based on the emphasis of different merits among the trade-offs of volume, cost and losses. The four core structures are: EE, EI, II and EA cores which have been shown in Fig. 10. Specifically, EE, EI, II are composed of two E cores, one E core and one I core, two I cores, respectively. The air gap of these three core structures could be adjusted by inserting different height of resin in the middle of the three legs. For the EA (E-Air) core, the airgap is not flexible and is mainly determined by the window width since the structure is open on top side without close loop flux path of magnetic material above the E core.

1) Core structure design based on window/airgap space and winding parallelization: The high resolution design is implemented in ANSYS for validating the proposed four core structures. For each structure, different airgap values or winding heights are simulated with different number of turns to derive the suitable inductance for critical soft switching with optimal core losses and peak flux density. Based on the soft switching requirements of inductance and current ripple in equations (4) and (5), the targeted inductance is 4μH. The simulated results of the four types of cores are shown in table IV. In each type of the EE, EI and II core structure, different turn numbers are constructed and swept with different airgap values to derive the optimal inductance, core losses and peak flux density. For the EA core, since the airgap is not adjustable, the total winding height is tuned for the adjustment of inductance. Specifically, table IV shows the derived optimal setup parameters of four core structures and the flux density distributions after simulating different airgaps/winding heights and turn numbers for each type of the core based on the same current excitation of 50A peak-peak and frequency of 500kHz and 1MHz.

2) Core structure trade off analysis: The four types of core structures are designed considering different emphasis of merit trade-offs. The EE core costs more on the core material and

has the largest volume. But the window height is the biggest which means more winding could be stacked in parallel to decrease the coil resistance and copper losses. II core has the smallest volume but the airgap is limited by the height of the winding coil which means the airgap needs to be no less than the coil height. Thus, the number of turns and airgap need to be carefully designed to support the desired inductance especially when considering to parallel winding coil for the reduction of copper losses. The EI core is a trade-off between the EE and II cores in the aspect of volume cost and copper losses. Lastly, for the EA core, the airgap is restricted by the open area on top of the E core. Specifically, the flux path can only go through the window width on top to finish the flux loop. Thus, the winding coil could not exceed the window upper side and the airgap is not as flexible as the other three structures. However, EA core saves half of the magnetic material which means the cost is the least. To better illustrate the flux paths of the four core structures with different airgap formations, the magnetic flux paths are shown in Fig. 11. The green solid arrows are the flux paths in the core and the red dotted arrows represent the flux paths in the airgap. Thus, the flexibility of adjusting airgap between EE, EI, II and EA could be seen perceptually in which the EA core has an approximately constant airgap of the window width.

For the influences of different core structures and the fringing effect on the inductor performance, three cases of inductor structure are simulated in ANSYS (under same turn number, airgap, current excitation) for validation: (1) EE core; (2) EI core with winding evenly distributed in the window; (3) EI core with winding distributed away from the airgap. The flux density and current density distributions of the three inductor cases are plotted in Fig. 12. The inductance, core losses are simulated as follows: case (1) Core Loss@500kHz: 4.6W, Core Loss@1MHz: 14W, L=4.4uH; case (2) Core Loss@500kHz: 4.7W, Core Loss@1MHz: 17W, L=4.6uH case (3) Core Loss@500kHz: 5.3W, Core Loss@1MHz: 19W, L=4.9uH. Thus, from the ANSYS comparison of cases (1) and (2), the EE or EI core difference does not influence too much of the inductor configuration. From the ANSYS comparison of cases (2) and (3), the fringing effect caused by the distance between the winding and airgap does not have obvious effect on the inductor behavior.

C. Neural Network Modeling of Litz/Solid PCB Structure

1) Neural network design: For the analytical modeling of AC losses in the litz/solid PCB winding, two 4-layer neural

TABLE IV
FOUR CORE STRUCTURES DESIGN RESULTS BY SWEEPING THE AIR GAP OR WINDING HEIGHT AND TURN NUMBER

Core type	EE	EE	EE	EI	EA	II
Turn number	10	6	4	4	5	8
Air gap (mm)	14	3	1	1.2	-	8
Winding height (mm)	-	-	-	-	5.8	-
P_{core}(W) @0.5MHz	1.9	4.6	11.6	7.2	2.7	0.4
P_{core}(W) @1MHz	9.7	23.6	49.4	28.5	13.8	2
Inductance(μH)	4.3	4.2	4.1	4.1	4.2	4.1
B_{pk}(T)	0.37	0.36	0.38	0.34	0.48	0.08

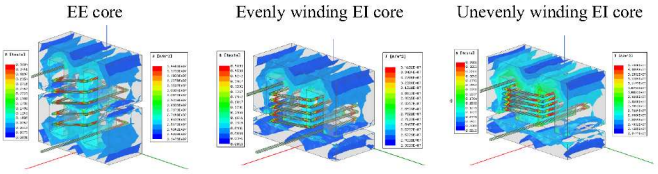
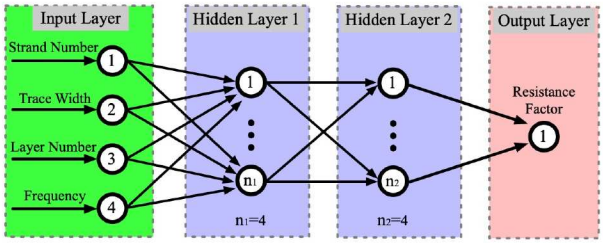


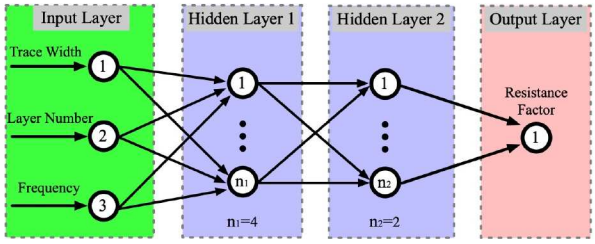
Fig. 12. Analysis of EE/EI core inductor performances with different winding distributions.

network models are built to analyze the resistance factors of the proposed litz/solid PCB winding under different design parameters. For the structure of the neural network, the 4-layer model consists of input layer, two hidden layers and output layer as is shown in Fig. 13.

Firstly, for the input layer, the key factors that could affect the resistance factor of litz PCB winding are strand number, N_s, trace width, W_s, trace thickness, t_{PCB}, layer number, N_l, and frequency, f_{sw}. The trace thickness could be determined by equation (27) to minimize the skin effect. Thus, 4 variables are configured as the input of the litz PCB neural network model including strand number, trace width, layer number and

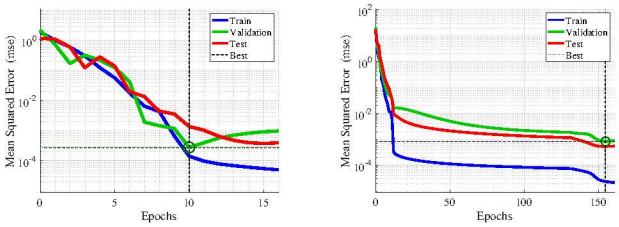


(a) Litz PCB neural network model.



(b) Solid PCB neural network model.

Fig. 13. Four-layer neural network model for resistance factor of the proposed (a) litz and (b) solid PCB winding.



(a) Litz PCB neural network model. (b) Solid PCB neural network model.

Fig. 14. Training and testing losses of the (a) litz and (b) solid PCB winding neural network model.

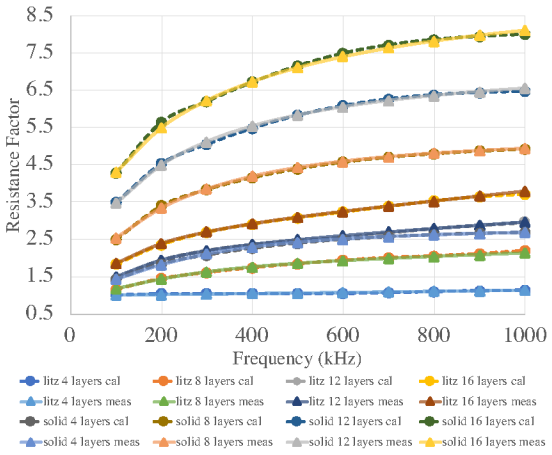


Fig. 15. Resistance factor comparison of the proposed litz PCB winding between the neural network model and measured values.

frequency. For the solid PCB winding, only trace width, layer number and frequency are needed for the input variables. Secondly, two hidden layers are designed to approximate smooth mapping for high accuracy. Different number of neurons are configured to optimize the training and testing losses. Table V shows the testing losses of the 4-layer neural network with different combinations of neuron number from 2 to 6 in the two hidden layers where the losses are defined by Mean Squared Error (MSE) to assess the performance of the model. Based on the size of training data and input/output variables, (4, 4) and (4, 2) of neuron number combinations in the two hidden layers can achieve minimum losses of 1.2e-4 and 4.6e-4 for litz PCB and solid PCB models, respectively. Lastly, for the output layer, the resistance factor is the output of the neural network model for the analysis of litz/solid PCB winding AC losses.

The formulation of the neural network consists of the following five parts: (1) input values, $x(k)$ (k=1,...,N_1, N_1=3 for three input variables of solid PCB model, N_1=4 for 4 input variables of litz PCB model); (2) hidden layer values, $h_1(k)$ (hidden layer 1 neurons, k=1,...,N_2, k denotes k-th hidden layer 1 neuron), $h_2(k)$ (hidden layer 2 neurons, k=1,...,N_3, k denotes k-th hidden layer 2 neuron); (3) output value, $y(k)$ (k=1,...,N_4, k denotes k-th output layer neuron); (4) weight, $W2_{mn}$ (weight from m-th input neuron to n-th hidden layer 1 neuron), $W3_{mn}$ (weight from m-th hidden layer 1 neuron to n-th hidden layer 2 neuron), $W4_{mn}$ (weight from m-th hidden layer 2 neuron to n-th output layer neuron); (5) bias, $B2_k$ (bias of k-th hidden layer 1 neuron), $B3_k$ (bias of k-th hidden layer 2 neuron), $B4_k$ (bias of k-th output layer neuron).

The input values, $x(k)$, can be imported as [N_s; W_s; N_l; f_{sw}] for litz PCB model and [W_s; N_l; f_{sw}] for solid PCB model.

The hidden layer values, $h_1(k)$ and $h_2(k)$, can be expressed as

$$h_1(k) = \sum_{k=1}^{N_2} W2_{mn}x(k) + B2_k, m = 1, ..., N_1, n = 1, ..., N_2 \tag{29a}$$

$$h_2(k) = \sum_{k=1}^{N_3} W3_{mn}x(k) + B3_k, m = 1, ..., N_2, n = 1, ..., N_3. \tag{29b}$$

The output layer values, $y(k)$, can be expressed as

$$y(k) = \sum_{k=1}^{N_2} W4_{mn}x(k) + B4_k, m = 1, ..., N_3, n = 1, ..., N_4. \tag{30}$$

2) Data training and testing: High resolution and accuracy ANSYS models for different litz PCB parameter combinations of (N_s, W_s, N_l, f_{sw}) and solid PCB parameter combinations of (W_s, N_l, f_{sw}) are imported for the training data. The Levenberg-Marquardt feed-forward backpropagation algorithm is applied for the training function to achieve a fast and accurate converging process. Fig. 14(a) and Fig. 14(b) show that the minimum testing losses of 1.2e-4 and 4.6e-4 are achieved with certain epochs of iteration for the litz PCB (4, 4) and solid PCB (4, 2) hidden layers neuron number combinations, respectively. More specifically, the validation of neural network model calculation and measured values of resistance factor are plotted in Fig. 15 where the solid lines with trigonal markers are the measured values and the dotted lines with round markers are the neural network model calculated values. It can be seen that the designed neural network models for litz/solid PCB winding highly emulate the resistance factors under different parameters.

3) Inductor loss optimization leveraging neural network: The inductor loss optimization can be implemented leveraging the analytical neural network models of AC resistance factor for the proposed litz/solid PCB winding. The main difference between the neural network-based PCB-type inductor loss optimization and the normal inductor design process of Fig. 4 is that number of turns, n_t, the number of paralleled PCB per turn, n_p, the strand number, N_s, and the trace width, W_s, for litz/solid PCB winding need to be swept and optimized.

The constraints for the optimization are:
(1) the multiplication of $n_t n_p$ should be less than the maximum allowable number of stacked PCB, $N_{max,PCB}$ (in a core window height of w_h):

$$n_t n_p \leq N_{max,PCB} = \frac{w_h}{t_{PCB}}. \tag{31}$$

(2) the multiplication of $N_s W_s$ should be less than the core window width, w_w:

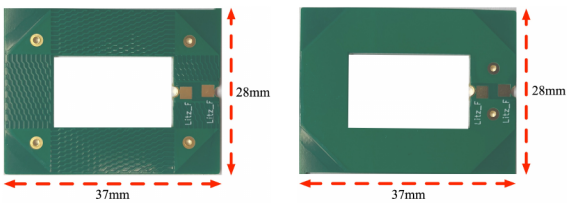
$$N_s W_s \leq w_w. \tag{32}$$

Thus, the neural network-based litz/solid PCB inductor design process can be illustrated in algorithm 1. By importing the required parameters of voltage, RMS current and ripple current, the optimal number of turns, n_t, number of paralleled

PCB per turn, n_p, strand number, N_s, trace width, W_s, and air-gap, l_g for litz/solid PCB inductor can be derived with minimum power losses at desired switching frequency. A preliminary neural network-based litz/solid PCB winding design results have been shown in table VI where the EE/EI solid/litz PCB winding inductors are analyzed to derive the low loss inductor winding parameters at the switching frequency of 500kHz. Since the air-gap of EA core is fixed and the winding height of II core is restricted by the air-gap, these two types of inductors are only designed by manually sweeping the turn number and number of PCB per turn in ANSYS and shown in the next section of prototyping results.

Algorithm 1 PCB Winding Intuctor Design Optimization

Initialize the parameters for V_{dc}, I_{rms}, Δi_L;
for f_{sw}=100kHz:10kHz:1MHz **do**
  calculate L by (4) or (5);
  check AP by solving (12);
  calculate $N_{max,PCB}$ by (31);
  calculate air-gap by (8);
  calculate peak flux density by (12);
  check if $B_{pk} \leq B_{max}$;
  $n_t \leftarrow 1, n_p \leftarrow 1, N_s \leftarrow 1, W_s \leftarrow 4mil$;
  while $n_t \leq N_{max,PCB}$ **do**
    while $n_t n_p \leq N_{max,PCB}$ **do**
      for N_s=1:4:80 **do**
        while $N_s W_s \leq w_w$ **do**
          calculate core losses by (11);
          calculate copper losses by (29), (30);
          calculate air-gap by (8);
          calculate peak flux density by (12);
          check if $B_{pk} \leq B_{max}$;
          $W_s = W_s + 4mil$;
        end while
        $W_s \leftarrow 4mil$;
      end for
      $n_p = n_p + 1$;
    end while
    $n_p \leftarrow 1$;
    $n_t = n_t + 1$;
  end while
  find optimal n_t, n_p, N_s, W_s, l_g with minimum losses;
end for



(a) Litz PCB winding. (b) Solid PCB winding.

Fig. 16. Litz and solid PCB winding prototypes.

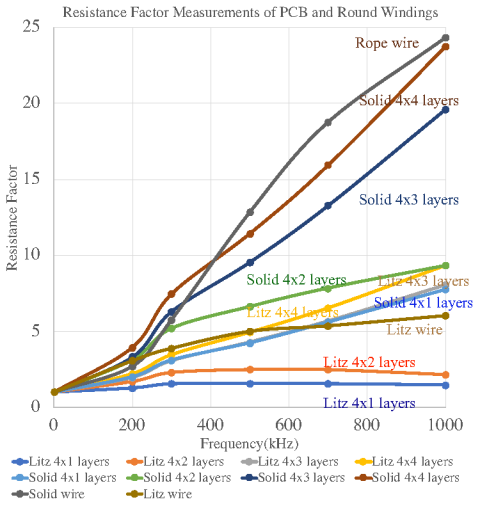


Fig. 17. Resistance factor measurements of different layers of litz/solid PCB windings and round normal/litz wires with different frequencies.

IV. Prototyping Results

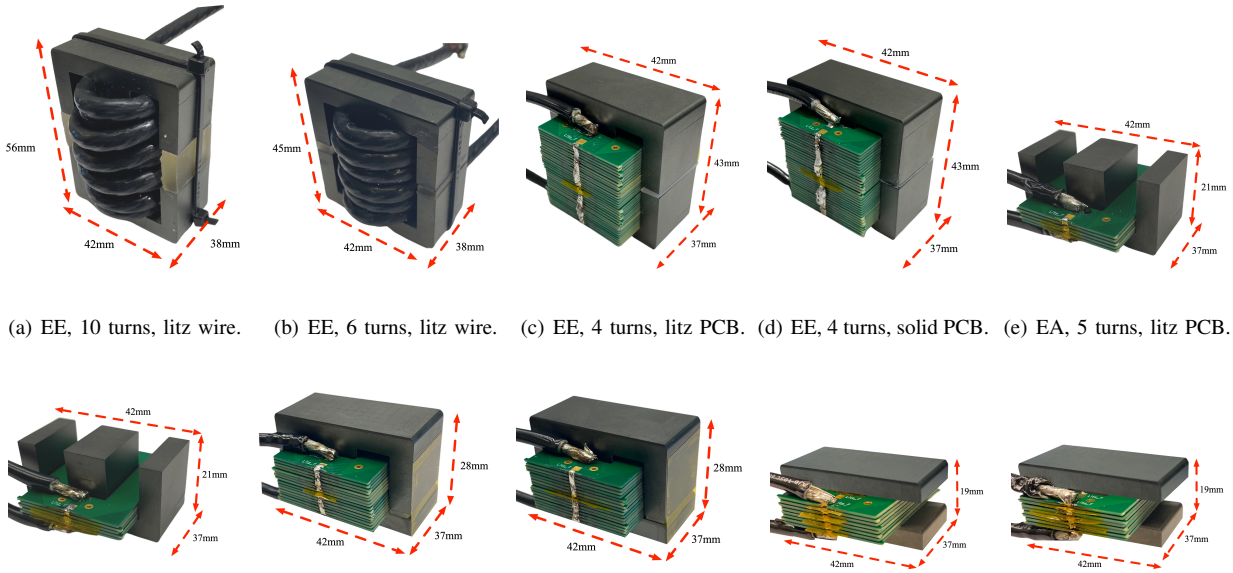
The designed inductors are prototyped in this section for the loss, volume and cost comparison. Based on the theoretical and practical core/winding design, 10 prototypes of EE/EI/EA/II core structures combined with litz wire/litz PCB/solid PCB windings are built for a comprehensive analysis.

A. Prototype Finalization

Firstly, the litz and solid PCB windings are fabricated as is shown in Fig. 16. Based on the resistance factor comparison in Fig. 7(a), the (4×10 Strands, 8 mils) litz routing structure has the smallest resistance factor and is selected as the litz PCB winding prototype. The resistance factor of the prototyped litz/solid PCB winding is measured with LCR meter by stacking different layers as is shown in Fig. 17. The measured RF is consistent with the ANSYS analysis in Fig. 7(b). Litz PCB has smaller RF than solid PCB and the advantage of RF is more remarkable with increased stacked number of layers. Also, a type of AWG 8 litz wire is applied for the litz wire winding. 10 prototypes are built and shown in Fig. 18. From Fig. 18(a) to 18(j), the inductor prototypes are designed as: EE core, 10 turns litz wire; EE core, 6 turns litz wire; EE core, 4 turns litz PCB; EE core, 4 turns solid PCB; EA core, 5 turns litz PCB; EA core, 5 turns solid PCB; EI core, 4 turns litz PCB; EI core, 4 turns solid PCB; II core, 8 turns litz PCB; II core, 8 turns solid PCB, respectively. The prototypes are designed and fabricated based on the parameters in table I. Considering the high frequency ranged from 100kHz to 1MHz and high current ripple of 50A for critical soft switching operation, the desired inductance, turn number and air-gap are following the theoretical design and core structure design with ANSYS validation in section II and III, respectively. Because the thickness of litz wire is higher than PCB winding, litz wire is only suitable for EE core with more window height as is shown in Fig. 18(a) and 18(b). On the other hand, the PCB winding is thin enough to be flexibly fit into any of the core structure's window area. To fully utilize the window area of

TABLE V
LOSS COMPARISON OF THE FOUR-LAYER NEURAL NETWORK WITH DIFFERENT NEURON NUMBER COMBINATIONS IN TWO HIDDEN LAYERS.

Neuron number in (hidden layer1, hidden layer2)	(2, 2)	(2, 4)	**(4, 2)**	(2, 6)	(6, 2)	**(4, 4)**	(4, 6)	(6, 4)	(6, 6)
Losses of litz PCB neural network model	1.5e-3	2.2e-3	5.2e-3	6.8e-3	7.2e-3	**1.2e-4**	3.9e-4	5.7e-4	6.2e-3
Losses of solid PCB neural network model	1.6e-2	7.7e-2	**4.6e-4**	9.1e-3	2.5e-2	2.8e-3	1.4e-3	9.9e-4	4.9e-3



(a) EE, 10 turns, litz wire. (b) EE, 6 turns, litz wire. (c) EE, 4 turns, litz PCB. (d) EE, 4 turns, solid PCB. (e) EA, 5 turns, litz PCB.

(f) EA, 5 turns, solid PCB. (g) EI, 4 turns, litz PCB. (h) EI, 4 turns, Solid PCB. (i) II, 8 turns, Litz PCB. (j) II, 8 turns, Solid PCB.

Fig. 18. Proposed inductor prototypes.

the cores for reducing the winding resistance, the PCB winding are stacked 8 and 4 layers in parallel per turn in EE of Fig. 18(c), 18(d) and EI core of Fig. 18(g), 18(h), respectively. Due to the limited window area of EA and II cores, the number of stacked PCB per turn is one for the EA prototypes of Fig. 18(e), 18(f) and II prototypes of Fig. 18(i), 18(j), respectively. For the EA core, the airgap is nonadjustable and determined by the width of the window area. For the II core, the airgap is limited by the total thickness of the PCB winding. Thus, EA/II inductors are designed by sweeping turn number in ANSYS to derive the desired configurations which are shown in the following section.

B. Experimental Validation

The inductor prototypes are tested with a buck converter at fixed duty cycle of 0.5 to deliver 50A current ripple at different switching frequency ranged from 100kHz to 1MHz.

TABLE VI
NEURAL NETWORK-BASED INDUCTOR DESIGN RESULTS

Parameters	n_t	n_p	N_s	W_s	Loss@500kHz
EE solid	4	7	-	-	22.32W
EE litz	4	6	44	8mil	20.04W
EI solid	4	4	-	-	26.24W
EI litz	4	3	36	12mil	32.28W

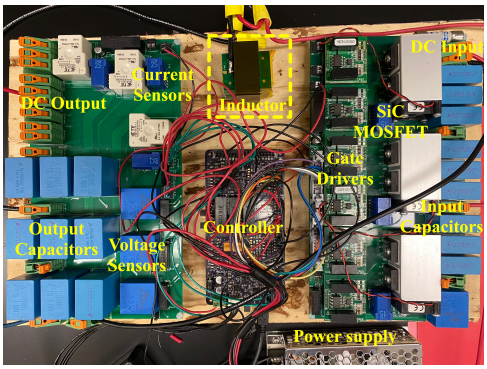
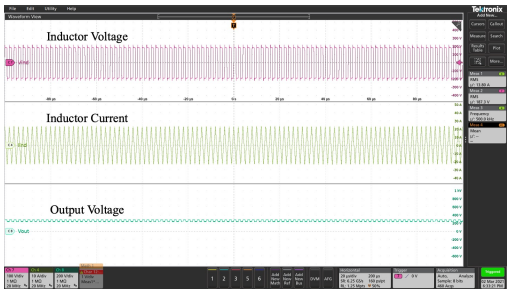


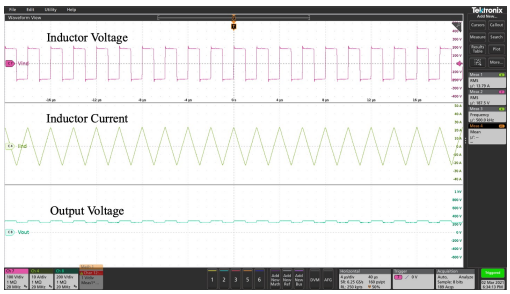
Fig. 19. Testbench for inductor loss measurement.

The testbench is shown in Fig. 19 including three-phase type of switch board on the right, controller board in the middle and sensing board on the left. The switch board is composed of SiC MOSFET (C2M0025120D)×6, gate driver (CRD-001)×6, DC bus capacitors (B32774D8505K, 5μF)×9 and DC voltage sensor (RP1215D). The sensing board includes three phase capacitors (B32774D8126K000, 12μF)×9, voltage sensor (RP1215D)×3, current sensor (CKSR 25-NP)×3, power relay (T9SV1K15-12)×3. Typical inductor voltage, inductor current and output voltage waveforms at 500kHz are shown in Fig. 20 with zoomed views. The PCB winding width and thickness are designed for a temperature rise of less than 40

°C under the desired current rating. The thermal behaviors of designed inductors are compared with the commercial ones in Fig. 21. The proposed inductors have temperature rise only up to 50-60°C which are 60-70°C lower than the commercial ones. For a solid winding, the AC resistance will be increased by a factor of more than 10 when the switching frequency is reaching 500kHz as is shown in Fig. 17. If the winding of commercial inductors are not specially designed, the AC losses will be increased proportionally. Thus, high temperature rise will occur if no active cooling system is added.

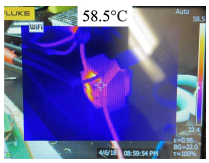


(a) Experimental waveforms.

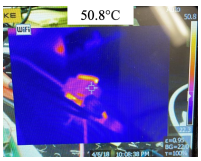


(b) Zoomed experimental waveforms.

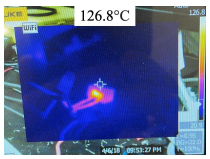
Fig. 20. Inductor voltage, inductor current and output voltage waveforms at 500kHz switching frequency, 500V input voltage and 0.5 duty cycle.



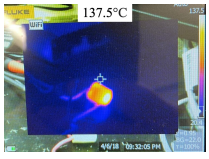
(a) EE core, litz PCB



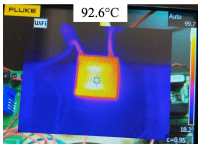
(b) EA core, solid PCB



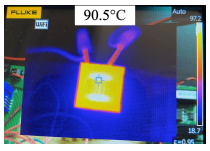
(c) SER inductor



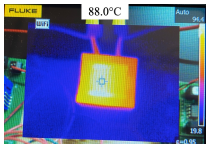
(d) AGM inductor



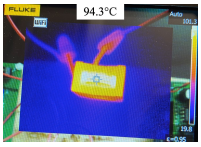
(e) AGP-332 inductor



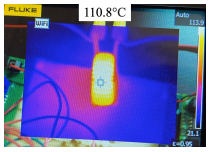
(f) AGP-562 inductor



(g) WE-0068 inductor



(h) WE-1022 inductor



(i) DMT2-20 inductor

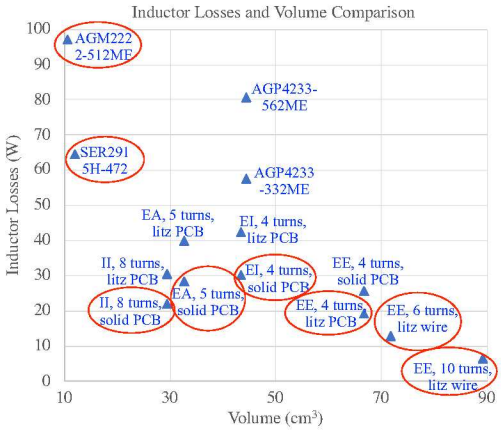
Fig. 21. Thermal behaviors of the designed and commercial inductors at 500kHz, 50A peak current.

The loss, volume and cost of the 10 proposed prototypes and two typical commercial inductors are compared in Fig. 22 and Fig. 23. Specifically, Fig. 22(a) shows the comparison of volume and loss at 500kHz. It can be derived that the EE core litz wire inductors have the lowest losses but higher volume. II and EA core PCB inductors have the smallest volume and higher losses. EE core PCB inductors have the medium volume and losses. The miminum losses are achieved with EE core 6 and 10 turns litz wire inductors which are 13.1W and 6.5W, respectively. The least volumes are achieved with II core 8 turns and EA core 5 turns PCB inductors which are 29.5 cm^3 and 32.6 cm^3, respectively. The commercial inductor of AGM and SER have significant losses compared with the proposed inductors despite of their small volumes. Also, the loss and cost among the inductors are compared in Fig. 22(b). For a mass production, the cost of the PCB winding inductor is less than the litz wire inductor and the commercial ones. The EA core inductor has the least cost since it needs only one core for fabrication. The circled points in the two figures are the desired solutions for the prototype if putting different weighing factors on the loss, volume or cost. Finally, the break down of core and copper losses for the 10 designed inductors and 2 commercial inductors are listed in Fig. 23 with frequencies of 100kHz, 500kHz and 1MHz. The caption of each prototype from (a) to (j) are consistent in Fig. 18 and Fig. 23. Compared with the commercial ones, the designed inductors reduced the core and copper losses significantly by a factor of 5-10.

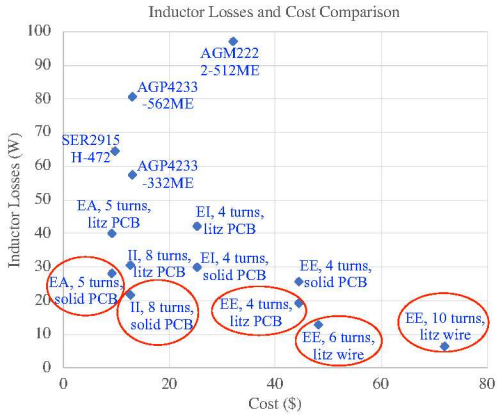
C. Observations

The following observations are derived from the conducted research:

1) The critical soft switching power converter at high power ($\geq 11kW$) and high frequency (100kHz-1MHz) requires a large current ripple ($\geq 50A$). The commercial inductors could not handle this high ripple high frequency current due to the high power losses and temperature rise ($\geq 125°C$).
2) The conducted research provides the specially designed critical soft switching inductors to handle high frequency large current ripple working conditions by reducing the overall losses by a factor of 5-10 and temperature rise by a factor of 2-3.
3) The AC winding losses can be reduced by introducing litz wire with large number of strand. But the cost and volume of litz wire are high due to the thick outer insulation jacket and manufacturing process.
4) Careful design of PCB litz/solid windings can be a substitute for the litz wire in the reduction of high frequency AC copper losses. On one hand, the thickness of PCB copper could be flexibly adjusted to reduce the high frequency AC losses caused by the skin effect. On the other hand, multiple pieces of PCB could be stacked in parallel per turn to fit into the core area for the reduction of the equivalent DC resistance.



(a) Losses and volume comparison.



(b) Losses and cost comparison.

Fig. 22. Comparisons of Power losses with volume and cost among the proposed prototypes and commercial products.

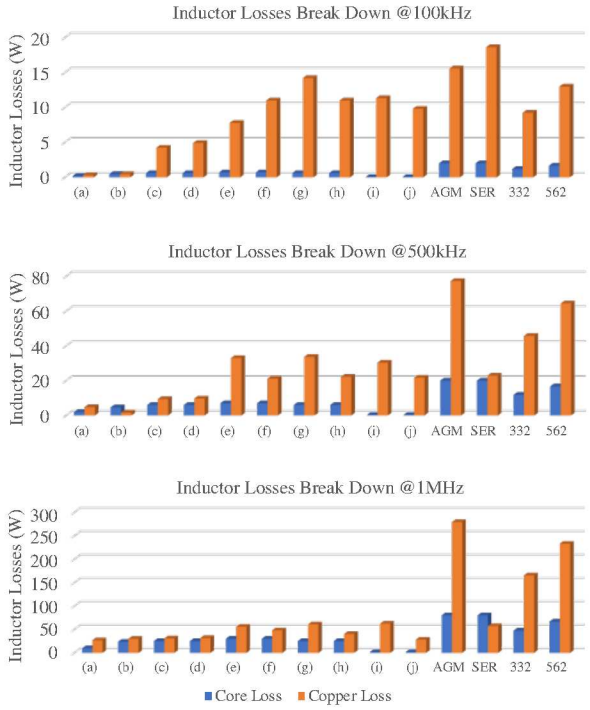


Fig. 23. Comparison of inductor core and copper losses break down at 100kHz, 500kHz and 1MHz.

5) The litz PCB 3D layout method could largely emulate the litz wire capability for attenuating the AC losses of skin and proximity effects by performing a small resistance factor.
6) The four core structures have advantages in different aspects. EE and EI core have more window area for paralleling more PCB to reduce the DC resistance. EA and II cores have less volume and cost. The flexibility of adjusting the stacked number of PCB for EE and EI cores are better than EA and II cores.
7) For the selection of inductor among the designed prototypes, if volume and cost are the two primary considerations, II 8 turns inductor and EA 5 turns inductor can be the preferences which reduce 50% of the volume and 75% of the cost compared to EE inductors. On the other hand, if the losses are the primary considerations, EE 10 turns litz wire inductor and EE 4 turn litz PCB inductor can be the preferences which reduce 40-60% of the losses compared to the II or EA inductors. Specifically for the core structure selection, the EE core has more window area for winding and is suitable for round litz wire (high diameter) and high inductance applications (more turn number). II core window area is restricted by the air-gap. Thus it is suitable for PCB winding (low thickness) and low inductance applications (less turn number).
8) For the selection of litz or solid PCB windings, the AC resistance can be calculated to guide for selection which are based on the DC resistance of two PCB windings, $R_{DC,litz}$ and $R_{DC,solid}$, in Fig. 16, number of turns, n_t, and number of paralleled PCB per turn, n_p, resistance factor at a stacked PCB number of $n_p \times n_t$, $RF_{n_p \times n_t}$. The total AC resistance of an inductor, $R_{AC,litz}$ or $R_{AC,solid}$, can be expressed as

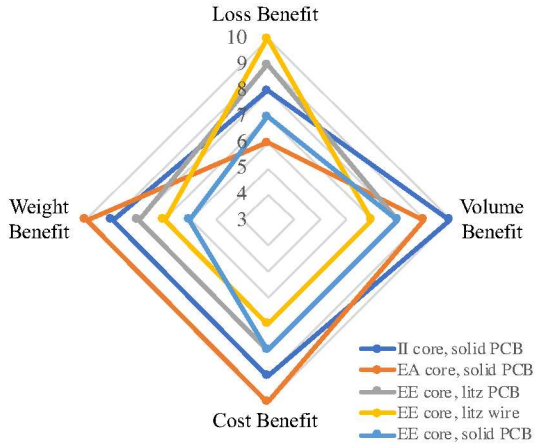


Fig. 24. Ratings of performance for four of the desired inductor prototypes.

$$R_{AC,litz} = \frac{R_{DC,litz} n_t}{n_p} RF_{litz,n_p \times n_t} \tag{33}$$

$$R_{AC,solid} = \frac{R_{DC,solid} n_t}{n_p} RF_{solid,n_p \times n_t}. \tag{34}$$

Thus, at a certain stacked PCB number of $n_p \times n_t$ inductor prototype, if $R_{AC,litz}$ is less than $R_{AC,solid}$ which means litz PCB has less copper losses, litz PCB winding can be chosen as preference. On the other hand, solid PCB can be the option. Based on the calculation in (33) and (34) and data in Fig. 7 and 17, in less stacked PCB number of $n_p \times n_t$ prototypes of EA and II core inductors, the solid PCB has less copper losses than litz PCB because the DC resistance dominates the copper losses more than the resistance factor. However, when the total stacked number of PCB is larger than 20 layers in EE core inductor, the litz PCB will prevail due to the litz layout's more capability than solid PCB at reducing the resistance factor at higher stacked number of PCB setups.

9) For the inductor optimization design methods that are developed in this paper, the round wire type of litz winding inductors are designed based on the analytical litz wire AC loss equations. The PCB type of litz/solid winding inductors are designed based on the proposed neural network model for the derivation of optimal PCB winding structures.

To summarize for the prototyping designs, the desired inductor setups are labeled with red circles in Fig. 22(a) and Fig. 22(b), respectively by considering different weighing factors on loss, volume or cost. EE litz wire inductor has low losses, higher cost and volume. EE litz PCB inductor has lower volume, higher losses and lower cost. II and EA core inductors have low volume, low cost and higher losses. All the designs are based on the critical soft switching conditions of high frequency (100kHz-1MHz), high current ripple (50A) which could not be handled by the benchmarked commercial inductors due to the high loss and temperature rise. Also a performance rating comparison radar chart of five desired prototypes scored from 6 to 10 is shown in Fig. 24 to address the advantages of different designs in the aspects of losses, volume, cost and weight. For each comparative item, the five prototypes are ordered and scored from 6 to 10 to show their strength in a unified radar chart system.

V. Conclusion

This paper develops a theoretical design method for high frequency and high efficiency inductor especially for critical soft switching in high current ripple application. The optimal design parameters are derived with the minimization of inductor losses. Also, the topological design of core and coil structures are proposed. Specifically, for the coil, a 3D litz PCB routing method and designing procedures are developed to reduce the AC losses. For the core, four types of core structures, EE, EI, II, EA, are developed for different merits of trade-off including core losses, volume and cost. A neural network-based litz/solid PCB winding AC loss modeling method is developed to analytically optimize the losses of the PCB inductor design. Finally, a comprehensive analysis and comparison of the proposed designs with typical commercial inductors shows the advantages of the proposed inductors in the aspect of high frequency high ripple losses and cost. Power losses, temperature rise and cost are reduced by factors of 10, 2.5 and 3, respectively, with the proposed core and coil structures for the high frequency high current ripple critical soft switching applications

VI. Acknowledgement

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TABLE VII
OVERALL COMPARISONS OF THE PROPOSED PROTOTYPES, COMMERCIAL INDUCTORS AND THEORETICAL DESIGN

	(a)	(b)	(c)	(d)	(e)	(f)	(g)	(h)	(i)	(j)	SER	AGM	332	562	Calculation
Loss (W) @100kHz	0.9	0.5	4.8	5.5	8.4	11.7	14.8	11.6	11.4	9.8	17.6	20.6	10.4	14.7	6.3
Loss (W) @500kHz	6.2	6.5	15.3	15.6	39.9	28.1	39.6	28.1	30.5	21.9	97.2	42.8	57.5	81	19.2
Loss (W) @1MHz	53.2	36.4	55.6	56.4	85.6	77.8	85.7	65.1	63.7	29.4	359.4	137	212.6	299.5	39.5
Volume (cm^3)	89.3	71.8	66.8	66.8	32.6	32.6	43.5	43.5	29.5	29.5	10.7	12	44.5	44.5	75
Cost ($)	72	48	44.4	44.4	9	9	25.2	25.2	12.6	12.6	32	9.6	13	13	32
Weight (g)	142	130	144	176	61	66	95	111	54	62	51	35.7	135	135	122

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