The Manhattan Configuration: a Differential Power Converter with Linear Scaling to N-levels

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***Abstract*—This paper proposes a multilevel power converter topology that processes less power than it outputs. It can be scaled to N-levels with linear component quantity and stress scaling and voltage balance is maintained for any voltage conversion ratio. It is composed of a set of series stacked capacitors where each additional capacitor defines an additional voltage level. Input voltage is applied across the entirety of the capacitor stack and the output can be taken at any node between capacitors. Capacitor voltage balance is maintained through any method of energy sharing between capacitors. The amount of power that needs to be transferred between capacitors to maintain voltage balance is less than the output power of the converter. Equations that describe this required power transfer are derived. An example implementation of a capacitive power transfer mechanism is shown. Functionality of the proposed topological framework is proven through high-fidelity simulation of an 8-level converter consisting of 8 series capacitors in both DC/DC and DC/AC modes of operation.**

I. Introduction

To increase space in urban developments, if one cannot build horizontally, one must build vertically. A parallel can be drawn with electrical engineering, and specifically, the field of power electronics. If more power is desired and it becomes infeasible to increase the current, then one must increase the voltage. And as cities have grown vertically with the passage of time, so too have the voltages present in society. High voltage DC transmission is approaching the GV range [1]. Modern electric vehicle (EV) batteries are, at present, in the range of 800V and steadily increasing [2] to the kV range. Even the ubiquitous USB standard, formerly at a static value of 5V, has increased to be configurable up to 20V, a decision largely driven by the power delivery benefits associated with the higher voltages [3].

These increases in voltages require an equal increase in the voltage ratings of their associated power electronics. For low voltages, such as those used in conjunction with USB standards, increasing the voltage for the power electronics is straightforward as there are many discrete components with sufficient voltage ratings. When voltages increase to a level that is beyond the rating of common discrete components, this process becomes less straightforward as simple power converter topologies can no longer be used. Instead, multilevel topologies must be implemented.

Multilevel power converter topologies serve to bridge the gap between higher voltage requirements and lower voltage discrete components. They allow for the control and conversion of voltages higher than the rating of any individual component. The component that is typically the bottleneck in increasing voltage is the switching device. Modern Silicon Carbide (SiC) devices can withstand >1200V [4], [5], allowing for the safe control and conversion of voltages in the range of 900V with typical single-level topologies. Using SiC devices for voltages higher than this will require a multilevel topology.

A variety of multilevel designs exist and there have been many reviews that balance the tradeoffs between different multilevel topologies [6]–[10]. However, no existing multilevel topology offers the combination of characteristics (linear component quantity/stress scaling with number of levels, modularity, inherent capacitor voltage balance, and simplistic control, and differential power conversion) that the topology this paper proposes has.

This paper proposes a new class of multilevel power converter topologies that are characterized by a set of series stacked capacitors with dynamic level voltages. Level voltages are defined by the voltage of each individual capacitor and all level voltages change with the output voltage. It is linearly scalable to N-levels, which is a valuable attribute as it allows for both increased voltage handling capabilities and reduced filtering requirements. Voltage balance is maintained through energy sharing between these capacitors, with energy sharing and connectivity techniques not critical to the functionality of this topology. It is a generalization of the topology found in [11]–[13], which is a derivation of the high conversation ratio converters of [14], [15].

Basic operating principles for a 2-capacitor 2-level converter upon which the topological framework is built are first derived. This 2-capacitor implementation is then expanded to a 4-capacitor 4-level converter to demonstrate the feasibility and trends of expansion to N-levels. Characteristics of an N-level converter are provided. Lastly, practical implementations of the capacitor energy sharing mechanism and connectivity techniques alongside simulated results of an 8-capacitor 8-level converter are shown to validate the proposed topological framework.

II. Topology Framework

Derivation of the proposed topological framework begins with its simplest implementation. The 2-capacitor ($k = 2$) 2-level ($N = 2$) converter can be seen in Fig. 1. Although this topology is capable of bidirectional power conversion, for the

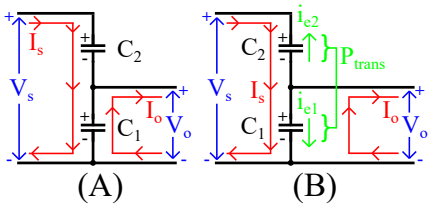

Fig. 1. Simplest implementation of the stacked capacitor multilevel framework (2-capacitor, 2-level). (a): Basic Topology. (b): Power transfer, highlighted in green, required to maintain voltage balance in steady state.

sake of brevity this paper considers the converter operating in step-down buck mode and the terms and figures are labeled as such. The input current I_s and output current I_o can be considered external current sources and draws, respectively. The input voltage is equal to the sum of capacitor voltages $V_s = V_{C1} + V_{C2}$ and the output voltage is equal to the lower capacitor voltage $V_o = V_{C1}$.

All power converters must follow the law of conservation of energy where the input power equals the output power (assuming ideal components with negligible losses). In the context of the proposed topological framework, this can be formally written as

$$P_s = P_o \tag{1}$$
$$V_s I_s = V_o I_o, \tag{2}$$

where P_s and P_o are the input and output powers, respectively. As the level voltages are defined by the capacitor voltages, to maintain voltage balance of all levels in steady state, the average capacitor currents must equal zero. The capacitor currents for the circuit of Fig. 1-(a) are

$$I_{C1} = I_s - I_o \tag{3}$$
$$I_{C2} = I_s. \tag{4}$$

This shows that the circuit of Fig. 1-(a) does not maintain voltage balance in steady state as the capacitor currents do not equal zero for non-zero input and output currents. I_{C2} will always be positive as, in the context of this analysis, I_s is always positive. I_o will be greater than I_s as this analysis considers this converter to be operating in step-down buck mode and I_{C1} will always be negative. As a result of this, V_{C2} will be steadily increasing and V_{C1} will be steadily decreasing and the converter of Fig. 1-(a) can be considered unbalanced in steady state.

This imbalance can be considered a result of excess power P_e applied to each capacitor

$$P_{e,C1} = V_{C1}(I_s - I_o) \tag{5}$$
$$P_{e,C2} = V_{C2} I_s, \tag{6}$$

where $P_{e,C1}$ and $P_{e,C2}$ represent the power that needs to be removed from each capacitor in order to achieve voltage balance in steady state. As the capacitor voltages are considered to always be positive, $P_{e,C2}$ will always be positive and $P_{e,C1}$ will always be negative. $C2$ has positive excess power and $C1$

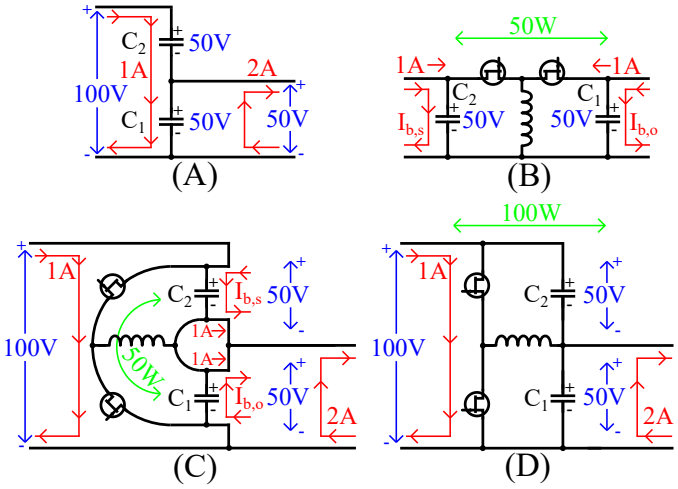

Fig. 2. 50W buck boost converter reconfigured into a 100W half-bridge converter. (a): Proposed stacked capacitor topology equivalent half-bridge converter. (b): 50W back boost converter. (c): Folding of the buck boost into a half-bridge converter. (d): 100W half-bridge converter.

has negative excess power. It can be seen that, given (1) - (6), $P_{e,C2}$ and $P_{e,C1}$ are equal in magnitude but opposite in sign, that is

$$V_{C1}(I_s - I_o) = -V_{C2} I_s \tag{7}$$
$$P_{e,C1} = -P_{e,C2} \tag{8}$$

and this can be proven through simple algebraic manipulation and holds true for all values of $0 \leq V_o/V_s \leq 1$. Therefore, in order to maintain capacitor voltage balance, the positive excess power from $C2$ can be transferred to $C1$ to compensate for both the negative excess power within $C1$ and the positive excess power within $C2$. This power transfer has the effect of neutralizing the capacitor currents of (3) and (4), resulting in average capacitor currents equaling zero and voltage balance in steady state being achieved. The equations for average capacitor currents can be adjusted to reflect this power transfer

$$0 = I_{C1} = I_s - I_o + i_{e1} \tag{9}$$
$$0 = I_{C2} = I_s + i_{e2}, \tag{10}$$

where

$$P_{trans} = P_{e,C1} = -P_{e,C2} \tag{11}$$
$$i_{e1} = \frac{P_{trans}}{V_{C1}} \tag{12}$$
$$i_{e2} = -\frac{P_{trans}}{V_{C2}} \tag{13}$$
$$0 = P_{e,C1} + P_{e,C2}. \tag{14}$$

Furthermore, as equal power is removed from the upper capacitor $C1$ as added to the lower capacitor $C2$, the law of conservation of energy is upheld. This power transfer can be visualized in Fig. 1-(b).

The amount of power that needs to be transferred between $C1$ and $C2$ is strictly a product of input/output voltages and currents and can be seen in the ratio of

$$\left|\frac{P_{trans}}{P_o}\right| = \left|\frac{I_s - I_o}{I_o}\right| = \left|\frac{V_s - V_o}{V_s}\right| \leq 1. \tag{15}$$

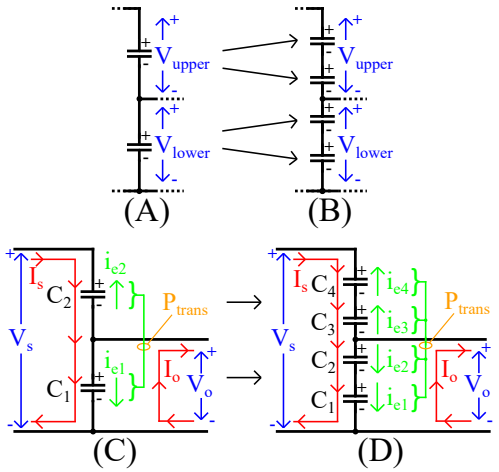

Fig. 3. Process of splitting a 2-capacitor 2-level converter into a 4-capacitor 4-level converter. (a), (c): 2-capacitor 2 level converter. (b), (d): 4-capacitor 4-level converter.

This amount of power that needs to be transferred P_{trans} will always be less than the output power of the converter P_o as $V_s - V_o \leq V_s$ and $|I_s - I_o| \leq I_o$. This is an important result as it implies that converters of this topology do not need to convert the entire input and output power P_o but rather just a conversion ratio dependant fraction of P_o.

This effect can be demonstrated through a practical implementation of a capacitive power transfer scheme for the 2-capacitor circuit of Fig. 1. Although the exact method of implementing the capacitive power transfer is not completely relevant to the topology, one such scheme that can be used to balance the circuit of Fig. 1 is a buck-boost converter. The buck-boost converter and its connectivity can be seen in Fig. 2.

To more effectively demonstrate the power transfers of this topology, values are assigned to the input and output currents and voltages of Fig. 2. The complete converter has input values of $V_s = 100$V and $I_s = 1$A, output values of $V_o = 50$V and $I_o = 2$A, and an overall power $P_o = 100$W. The buck-boost converter, used to transfer power between capacitors $C1$ and $C2$ has input values of $V_{b,s} = 50$V and $I_{b,s} = 1$A, output values of $V_{b,o} = 50$V and $I_{b,o} = 1$A, and an overall power $P_{b,o} = 50$W.

Fig. 2-(a) shows the shows the stacked capacitor topology without the buck-boost power transfer scheme. Fig. 2-(b) shows the buck-boost converter that is used to share power between the upper capacitor C2 and the lower capacitor C1. Fig. 2-(c) shows how the buck-boost converter is connected within the stacked capacitor topology so that it effectively transfers power between C1 and C2.

Current flows are noted in Fig. 2 and it can be seen that in this configuration the 50W buck-boost converter can be used to create a 100W converter. In this manner, this stacked capacitor topology handles less power than it flows. Lastly, it is worth noting that using the buck-boost converter to transfer power between capacitances in this 2-capacitor configuration results in the ubiquitous half-bridge converter.

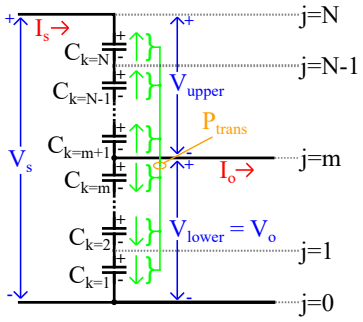

Fig. 4. N-level converter of the proposed topological framework.

III. Expansion to N-levels

The stacked capacitor topology is not limited to the 2-capacitor converter of Fig. 1. Each capacitor of Fig. 1 can be split into any arbitrary number of series capacitors. For the sake of clarity, the process of expansion to N-levels begins with splitting each capacitor of Fig. 1 into two series capacitors, resulting in a converter of $k = 4$ series capacitors and $N = 4$ levels. This converter can be seen in Fig. 3.

Analysis of this 4-capacitor converter follows the same process as the analysis of the 2-capacitor converter of Fig. 1. As stated previously the converter needs to adhere to the laws of conservation of energy outlined in (1) and (2). The capacitor currents due to externalities I_s and I_o are

$$i_{C1} = I_s - I_o \tag{16}$$
$$i_{C2} = I_s - I_o \tag{17}$$
$$i_{C3} = I_s \tag{18}$$
$$i_{C4} = I_s, \tag{19}$$

and the excess power within each capacitor for voltage balance is

$$P_{e,C1} = V_{C1}(I_s - I_o) \tag{20}$$
$$P_{e,C2} = V_{C2}(I_s - I_o) \tag{21}$$
$$P_{e,C3} = V_{C3}I_s \tag{22}$$
$$P_{e,C4} = V_{C4}I_s. \tag{23}$$

It can be seen that the upper capacitors $C3$ and $C4$ have the same values for excess powers P_e and capacitor currents i_c. This is also true for the lower capacitors $C1$ and $C2$. The distinction into upper and lower capacitors can be made, and excess powers within the upper and excess powers within the lower capacitors combined

$$P_{e,upper} = P_{e,C3} + P_{e,C4} = I_s V_{upper} \tag{24}$$
$$P_{e,lower} = P_{e,C1} + P_{e,C2} = (I_s - I_o)V_{lower}, \tag{25}$$

where the upper and lower voltages V_{upper} and V_{lower} are

$$V_{upper} = V_{C3} + V_{C4} \tag{26}$$
$$V_{lower} = V_{C1} + V_{C2}. \tag{27}$$

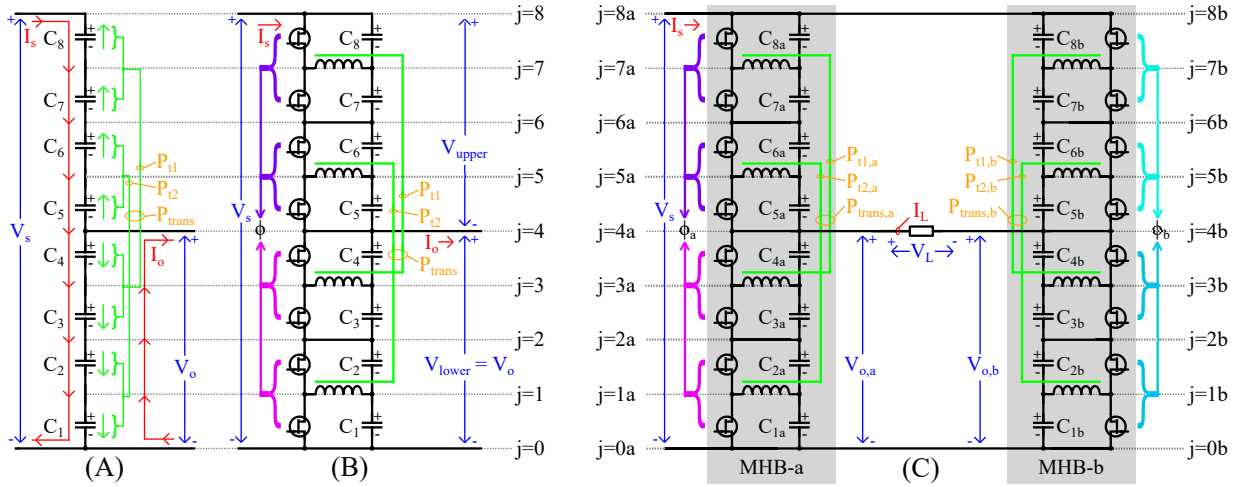

Fig. 5. 8-capacitor 8-level converters of the proposed Manhattan Configuration utilizing Dual Active Half-Bridges (DAHBs) as capacitive power transfer mechanisms. (a): stacked capacitor schematic with obfuscated capacitive power transfer mechanisms. (b): Multilevel Half-Bridge (MHB) implementation of proposed topology with DAHBs used as the capacitive power transfer mechanisms. (c): Multilevel Full-Bridge (MFB) implementation of the proposed topology with DAHBs used as the capacitive power transfer mechanism.

The total power that needs to be transferred from the upper capacitors to the lower capacitors to maintain voltage balance in steady state is then

$$P_{trans} = -P_{e,lower} = P_{e,upper} \tag{28}$$

An equivalency can then be drawn between the excess powers of the 4-capacitor converter and the excess powers of the 2-capacitor converter. For a given input/output voltage/current, the excess powers within the upper capacitors of both the 4-capacitor and the 2-capacitor converters are equal. The same true for both sets of lower capacitors. This effect can be leveraged, and it can be seen that the magnitude of the required capacitance power transfer to maintain voltage balance in steady state does not change with the number of series capacitors in the stack (and therefore the number of levels). Furthermore, the number of capacitors below the output node does not need to equal the number of capacitors above the output node.

The theory behind the 2-capacitor and 4-capacitor converter can then be generalized for a converter of k-capacitors and N-levels. The generalized N-level converter can be seen in Fig. 4. Nodes are numbered with the nomenclature j and capacitors with the nomenclature k. The output node is taken at node $j = m$, and capacitors $1 < k < m$ belong to the set of lower capacitors and capacitors $m + 1 < k < N - 1$. The capacitor currents due to I_s and I_o externalities are

$$i_{c,lower} = I_s \tag{29}$$

$$i_{c,lower} = I_s - I_o. \tag{30}$$

The excess powers are found in an identical manner as previously defined

$$P_{e,lower} = \sum_{k=1}^{m} i_{ck} V_{ck} = I_s V_{upper} \tag{31}$$

$$P_{e,upper} = \sum_{k=m+1}^{N-1} i_{ck} V_{ck} = (I_s - I_o) V_{lower}. \tag{32}$$

It is worth noting that the excess powers of the above generalized N-level converter match both the excess powers of the 4-capacitor converter ((24) and (25)) and the 2-capacitor converter ((5) and (6)). The same relationship between the necessary power transfer for voltage balance P_e and the power of the converter P_o can be made

$$P_o = I_s \sum_{k=1}^{N-1} V_{ck} = I_o \sum_{k=1}^{m} V_{ck} \tag{33}$$

$$P_{trans} = I_s \sum_{k=1+m}^{N-1} V_{ck} = (I_s - I_o) \sum_{k=1}^{m} V_{ck}. \tag{34}$$

Two equivalent ratios of P_{trans}/P_o can then be found

$$\left| \frac{P_{trans}}{P_o} \right| = \left| \frac{I_s \sum_{k=1+m}^{N-1} V_{ck}}{I_s \sum_{k=1}^{N-1} V_{ck}} \right| = \left| \frac{V_{upper}}{V_s} \right| \tag{35}$$

$$\left| \frac{P_{trans}}{P_o} \right| = \left| \frac{I_o \sum_{k=1}^{m} V_{ck}}{I_o \sum_{k=1}^{m} V_{ck}} \right| = \left| \frac{I_s - I_o}{I_o} \right|. \tag{36}$$

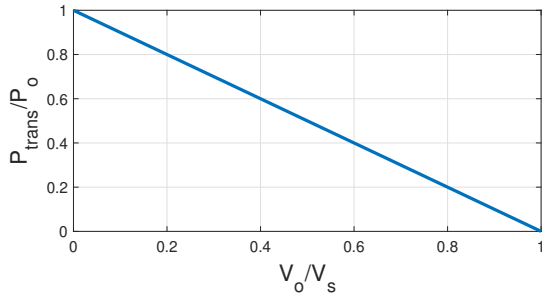

Fig. 6. P_{trans}/P_o ratio as a function of voltage conversion ratio V_o/V_s.

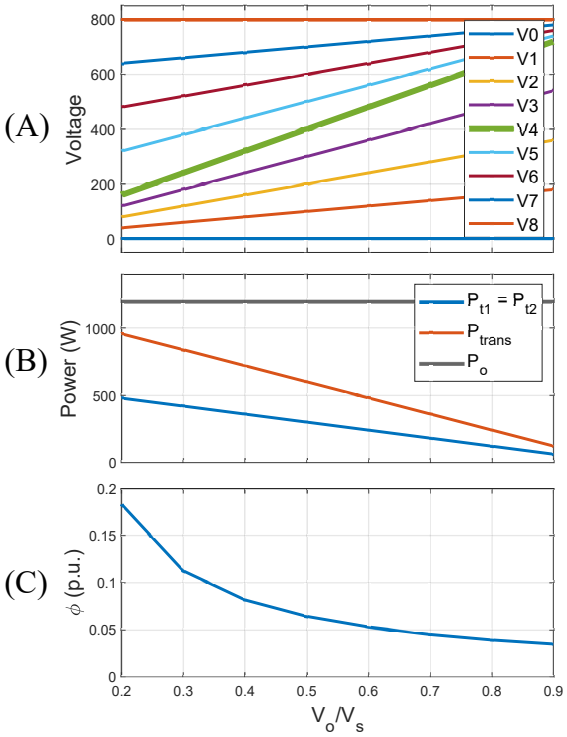

Fig. 7. MHB DC/DC conversion results. (a): Individual level voltages. (b): Internal and external power flows of the MHB. (c): Normalized phase difference ϕ between opposing sides of both DAHBs.

where the P_{trans}/P_o ratio for the N-capacitor converter ((35) and (36)) are identical to the ratio for 2-capacitor converter (15). The P_{trans}/P_o ratio as a function of the voltage conversion ratio V_o/V_s can be seen in Fig. 6.

The above results show that P_{trans} does not depend on the number of levels. Furthermore, as can be seen in Fig. 6, the relationship between P_{trans} and conversion ratio V_o/V_s is linear and always less than 1 over the entire output voltage range. This has the implication that component stresses, for a given input/output voltage and power level, do not change with the number of levels. Therefore, this converter can be considered linearly scalable to N-levels with respect to both component quantities and component stresses.

IV. Practical Implementations Through High-Fidelity Simulation

Two methods of implementing the capacitive power transfer links have been explored. The first of which is through non-isolated half-bridges, which have previously been studied and can be found in [11]. For the sake of brevity this paper includes only one new method of capacitive power transfer which utilizes Dual Active Half-Bridges (DAHBs) to link capacitances together. The schematic for this method implemented in 8-capacitor 8-level converters can be seen in Fig. 5 where each DAHB services a set of 4 capacitors (2 upper capacitors and 2 lower capacitors). It is important to note that each side of the DAHB is on opposite sides of the output node. This is because power must be moved from the upper capacitors into the lower

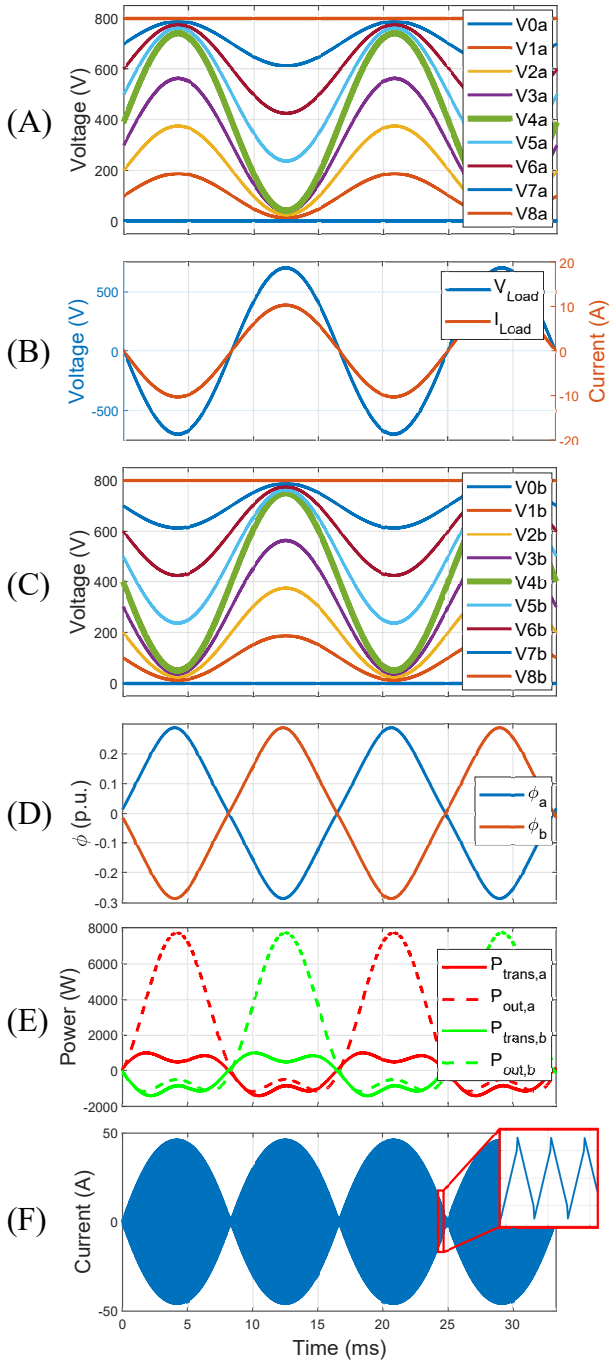

Fig. 8. MFB DC/AC conversion results. (a): Individual level voltages for MHB-a. (b): Load voltage and current. (c): Individual level voltages for MHB-b. (d): ϕ_a and ϕ_b for MHB-a and MHB-b, respectively. (e): Leakage inductor L_{lk} current.

capacitors. As shown in [11], moving power from capacitors in a cascading (not exclusively from upper to lower) scheme will induce circulating currents.

There are two circuits considered in this evaluation. The first is the Multilevel Half-Bridge (MHB) implementation which can be seen in Figs. 5-(a) and 5-(b). The second is the Multilevel Full-Bridge (MFB) circuit seen in Fig. 5-(c).

The MHB circuit is used for the DC/DC results and the MFB circuit is used for the DC/AC results. Both circuits have the same parameters of leakage inductance $L_{lk} = 4\mu$H, capacitance values of $C_{1-8} = 12\mu$F, coupled inductor turns ratio of $n = 1$, input voltage $V_s = 800V$, and switching frequency $f_{sw} = 250kHz$.

Rudimentary PI control is implemented for both the DC/DC and DC/AC circuits. For both circuits, the duty cycle of all half-bridges is set to $D = 0.5$ and the switching states are synchronized. The phase differences ϕ, normalized to the switching period, between opposing sides of all DAHBs for each MHB are set to be the same value. For each MHB, ϕ is controlled by the PI controller to achieve a desired reference output voltage V_o. A single PI controller with a DC reference voltage is used for the DC/DC circuit. Two PI controllers, each with AC reference voltages of opposite phases, are used for the DC/AC circuit where each MHB has its own controller.

The DC/DC results can be seen in Fig. 7. The reference output voltage is varied from $0.2V_s$ to $0.9V_s$ while the output power is held constant at $P_o = 1.2kW$. It can be seen that ideal voltage splitting across the capacitors is achieved (where $V_{C1-4} = V_o/4$ and $V_{C5-8} = (V_s - V_o)/4$) and the calculated power flows match the measured power flows of Fig. 6 at all points in this sweep.

The DC/AC results can be seen in Fig. 8. These results demonstrate bidirectional power flow, as shown in Fig. 8-(b) where the polarity of the load current alternates and power flows both in and out of each MHB. Ideal voltage splitting is maintained throughout the AC cycle and the control of ϕ_a and ϕ_b are effective in achieving the reference output AC waveforms. It can also be seen that the output power of each MHB P_{out} is always greater than the internal amount of power than needs to be converted P_{trans} to maintain capacitor voltage balance. Lastly, the leakage inductor current for a single DAHB can be seen in Fig. 8 where typical DAHB circuit behaviour can be observed.

In this manner, the predicted results of the previous section are validated. It can be seen that converters of this topological family do not need to convert the full output power, but rather just move a proportionally smaller amount of power from the upper set of capacitors to the lower set of capacitors. As this amount of power is proportional to the difference between input and output voltages, this topology can be considered as a new family of differential power converters.

V. Conclusion

The results provided in this paper show that the proposed stacked capacitor multilevel topology is linearly scalable to N-levels and can function bidirectionally in both DC/DC and DC/AC modes of operation. Furthermore, the potential simplicity of the example control scheme and capacitive power transfer mechanism is demonstrated as the entirety of the converter, regardless of the number of levels, can be controlled through a single parameter (the phase difference ϕ between opposing sides of the DAHBs). Lastly, the amount of power that needs to be converted, or transferred, internally to the converter is less than the output power of the converter, an attribute that is unique to this multilevel topology. Further work for this topology involves construction of an experimental testing platform and investigating other methods of capacitive power transfer.

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