A Family of Fully Balanced and Vertically Stacked Multilevel Power Converters with Linear Scaling

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***Abstract*—This paper presents methods of practically implementing capacitive power transfer schemes for the stacked capacitor Manhattan Configuration multilevel topology. The Manhattan Configuration is a multilevel topological framework with linear component quantity and stress scaling to N-levels. It is composed of a center stack of capacitors where each capacitor defines a single level of the converter. The functionality of the converter is controlled through the movement of power between capacitors in the center stack. It is shown that the amount of power that needs to be moved between these capacitors to maintain voltage balance in steady state is less than the output power of the converter, denoting the differential aspect of this topological framework. Four capacitive power transfer methods are provided as well as state space equations for each that can be used for future control formulations. Each capacitive transfer method is benchmarked against each other with respect to component quantities, stresses, and transient step response settling times. Lastly, selected steady state transient high-fidelity simulations are provided.**

I. Introduction

There is an ever-present push for higher voltages within society. This can be partially attributed to the drive for increased electrical power as beyond a certain point it becomes ineffective to increase the current to achieve higher powers. An example of this phenomenon is in long distance power transmission, where voltages have steadily increased into the GV range [1]. Electric Vehicle (EV) batteries have also seen an increase in voltage since their most modern introduction [2]. Even the basic USB standard has increased from 5V to 20V, largely a product of the desire for increased USB power delivery [3].

Increasing the voltage of a power converter up to a certain limit is a straightforward process. Typical (buck, boost, buck/boost) or more exotic (Cuk, SEPIC) single-level topologies can be used until the voltage levels within the converter increase to the limit of what the individual circuit components can handle [4], [5]. Beyond this voltage a multilevel topology is required, as these types of topologies serve to bridge the gap between lower voltage components and higher voltage applications [6], [7].

The individual circuit component voltage limit often lies within the switching device. State-of-the-art but readily available Silicon Carbide (SiC) FETs have a breakdown voltage less than 2000V [8]. Other components, such as inductors and capacitors, can be placed in series with minimal supporting adjustments for higher voltage ratings. However, the series connection of FETs is not as straightforward a process as precaution needs to be taken to ensure the voltage distribution across the FETs is even. Therefore, a multilevel topology is required.

This paper proposes a stacked capacitor multilevel topological framework, denoted as the Manhattan Configuration. It is a generalization of the topology found in [9], which is a derivation of the high conversation ratio converters of [10], [11]. Increased voltage is achieved through the series connection of capacitors. Converter performance is defined through the control of the amount of power shared between capacitors. This enables the voltage across the entire set of series capacitors to be arbitrarily distributed amongst each individual capacitance, allowing for the control and conversion of voltages higher than the rating of any individual component, which is a necessity for any multilevel topology. Voltage balance is maintained in steady state and component quantities scale linearly with the number of levels.

Furthermore, the total amount of power that needs to be moved internally between capacitors is less than the output power of the converter. Any method of capacitive power transfer can be used in conjunction with this topological framework, however, some are more beneficial than others. Four methods of capacitive power transfer are provided and benchmarked against each other with respect to component quantities, stresses, and theoretical maximum output voltage slew rate. A mathematical framework upon which an optimized control scheme can be derived is provided alongside methods of adapting this framework to any arbitrary capacitive power transfer scheme.

II. Topological Framework

As discussed previously, the Manhattan Configuration is defined by a set of series capacitors where each capacitor represents an additional level of the entire multilevel converter. The generalized Manhattan configuration can be seen in Fig. 1. For the sake of brevity, this paper considers the converter to always be operating in step-down buck mode and the terms are labeled as such. Likewise, throughout this paper, the output is

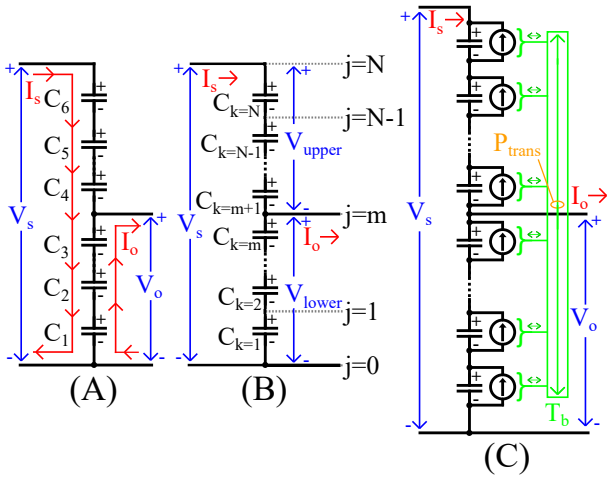

Fig. 1. Generalized Manhattan Configuration multilevel topological framework. (a): 6-level implementation. (b): N-level implementation. (c): capacitive power transfer scheme with connectivity of $\mathbf{T_b}$.

taken at exclusively the center node, but this is not a necessity and may not be optimal for all applications.

Analysis begins with noting the law of conservation of energy, which all power converters must follow. The ideal case is considered, and this constraint in conjunction with the nomenclature used in this paper is

$$P_s = P_o \tag{1}$$
$$V_s I_s = V_o I_o, \tag{2}$$

where P_s and P_o are the input and output powers, respectively. V_s and I_s are the input voltage and current and V_o and I_o are the output voltage and current.

The distinction between upper capacitors and lower capacitors can be made, where the upper capacitors consist of those in the center capacitance stack between the output node and the positive node of the input voltage ($C6$, $C5$, and $C4$ in Fig. 1-(a)). The lower capacitors consist of those in the center capacitance stack between the output node and the negative node of the input/output voltage ($C3$, $C2$, and $C1$ in Fig. 1-(a)). Basic circuit analysis of Fig. 1-(b) provides the capacitor currents for the N-level implementation as

$$I_{C,l} = I_{C,k=1} = I_{C,k=2} = \ldots = I_{C,k=m} \tag{3}$$
$$I_{C,u} = I_{C,k=m+1} = I_{C,k=m+2} = \ldots = I_{C,k=N} \tag{4}$$
$$I_{C,l} = I_s - I_o \tag{5}$$
$$I_{C,u} = I_s. \tag{6}$$

where j is used to number nodes and k is used to number capacitors. Node $j = m$ is used to denote the node where the output is taken. It can be seen in (3) - (6) that the capacitor voltages are not balanced in steady state for non-zero values of input and output currents I_s and I_o. $I_{C,l}$ will always be negative and $I_{C,u}$ will always be positive as I_o will always be greater than I_s in step-down buck mode operation. As a result of this, the upper capacitors will steadily increase in voltage and the lower capacitors will steadily decrease in voltage, and capacitor voltage balanced is not maintained. A method of capacitive power sharing must be implemented in order to maintain capacitor voltage balance in steady state.

However, before implementing a capacitor power transfer scheme, both the direction and magnitude of the required power flows must be defined. The excess power in the upper capacitors $P_{e,upper}$ is equal to the product of the upper capacitor current $I_{C,u}$ of (6) and the upper voltage V_{upper}

$$V_{upper} = \sum_{i=m+1}^{N} V_{C,i} \tag{7}$$
$$P_{e,upper} = V_{upper} I_{C,u}. \tag{8}$$

The excess power $P_{e,upper}$ must be removed from the series combination of the upper capacitors in order to maintain capacitor voltage balance in steady state. Likewise, there is excess power $P_{e,lower}$ in the lower capacitors that is equal to the product of the lower capacitor current $I_{C,l}$ of (5) and the lower voltage V_{lower}

$$V_{lower} = \sum_{i=1}^{m} V_{C,i} \tag{9}$$
$$P_{e,lower} = V_{lower} I_{C,l}, \tag{10}$$

where the excess power in the lower is, in the context of this analysis, negative. A quantity of power equal to $P_{e,lower}$ must be added to the series combination of the lower capacitors in order to maintain capacitor voltage balance in steady state.

Using the law of conservation of energy equations of (1)-(2), the equations for excess powers of (8) and (10), and simple algebraic manipulation, it can be seen that

$$V_{upper} I_{C,u} = -V_{lower} I_{C,l} \tag{11}$$
$$P_{e,upper} = P_{e,lower} = P_{trans} \tag{12}$$

where the excess powers in the upper and lower, $P_{e,upper}$ and $P_{e,lower}$, are equal in magnitude but opposite in sign. This is a convenient result as it implies that capacitor voltage balance in steady state can be achieved by internally sending excess power of the quantity P_{trans} from the upper capacitors to the lower capacitors, cancelling out the entirety of the excess powers in the process.

This capacitive power transfer can be visualized in Fig. 1-(c) where $\mathbf{T_b}$ is a connectivity matrix that defines the capacitive power transfer links. The power transfer between capacitances can be considered as current sources in parallel with each capacitor where the role of each current source is to support capacitor voltage balancing.

A state space model with respect to capacitor voltages can then be defined. I_s and I_o can be considered external current flows, and the nomenclature $i_e = [I_s, I_o]'$ ascribed. The relationship between capacitor current and capacitor voltage is

$$dV_c = \frac{I_c}{C} dt \tag{13}$$

where I_c is the total capacitor current and C is the capacitance value. I_c can be split into two components, the capacitor

current due to externalities i_e and the capacitor current due to internal capacitive power transfer links i_b

$$dV_c = \frac{i_e + i_b}{C} dt. \tag{14}$$

The equation for capacitor voltage of (14) can then be reconfigured into a state space formulation

$$V_c^+ = V_c + \frac{T_s}{C}\mathbf{T_b} i_b + \frac{T_s}{C}\mathbf{T_e} i_e. \tag{15}$$

with a constraint of

$$V_c \mathbf{T_b} i_b = 0. \tag{16}$$

This state space model can be used as a foundation to formulate an optimized control method. The constraint represents the limitation that the sum of the powers into each capacitor that comes from the internal capacitive power transfer mechanisms must equal zero. V_c is a vector of capacitor voltages $V_c = [V_{C,1}, V_{C,2}, \dots V_{C,N}]'$. T_s is the sample interval of the controller upon which this state space model runs. $\mathbf{T_e}$ is a topology matrix that represents the connectivity of the input and output nodes and when multiplied with i_e results in the individual capacitor currents due to externalities I_s and I_o. For reference, the topology matrix $\mathbf{T_e}$ of Fig. 1 is

$$\mathbf{T_e} = \begin{bmatrix} 1 & 0 \\ 1 & 0 \\ 1 & 0 \\ 1 & -1 \\ 1 & -1 \\ 1 & -1 \end{bmatrix}. \tag{17}$$

$\mathbf{T_e}$ also represents the direction of current flow of the external input and output currents. This shows how it is necessary to transfer power from cells above the output node to cells below the output node to maintain capacitor voltage balance in steady state.

Lastly, the final components of the state space model of (15) are $\mathbf{T_b}$ and I_b, which jointly represent the internal capacitive power flows. $\mathbf{T_b}$ is a connectivity matrix that defines which capacitors are linked together and can share power with eachother, and I_b is a vector that denotes the amount of power that gets shared across each capacitive power transfer link. $\mathbf{T_b}$ and I_b are unique to each capacitive power transfer scheme and are discussed in the following section.

III. Capacitive Power Transfer Link Implementations

As discussed previously a capacitive power transfer scheme is necessary to maintain capacitor voltage balance in steady state. The exact method of power transfer is not crucial for the functionality of the topology but will impact the overall converter performance.

Four example methods of capacitive power transfer are provided. An example 8-capacitor 8-level converter is used to demonstrate each capacitive power transfer scheme.

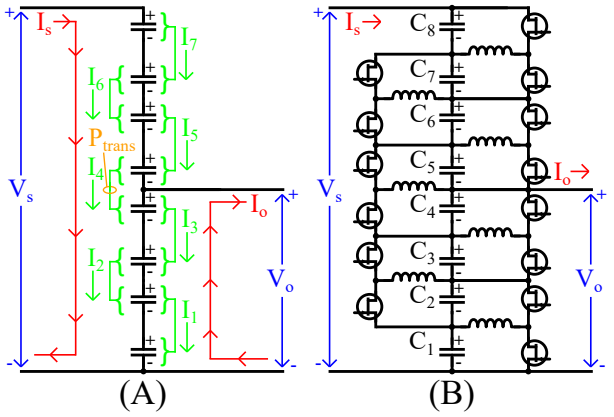

Fig. 2. 8-level half-bridge (HB) implementation of the Manhattan Configuration. (a): Internal power flow diagram and notation. (b): Circuit schematic.

A. Case 1: Half-Bridges

Half-bridges (HB) allow for power transfer between two adjacent capacitors in the center capacitance stack. By interleaving half bridges along the stack, all capacitors are connected together in a cascading manner. This technique is discussed in depth in [9]. The circuit that utilizes this technique can be seen in Fig. 2.

This HB circuit has a connectivity matrix $\mathbf{T_b}$ and link current vector I_b of

$$I_b = \begin{bmatrix} I_1 \\ I_2 \\ I_3 \\ I_4 \\ I_5 \\ I_6 \\ I_7 \end{bmatrix} \mathbf{T_b} = \begin{bmatrix} 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ -1 & 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & -1 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & -1 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & -1 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 & -1 & 1 & 0 \\ 0 & 0 & 0 & 0 & 0 & -1 & 1 \\ 0 & 0 & 0 & 0 & 0 & 0 & -1 \end{bmatrix}. \tag{18}$$

It can be seen in (18) that the each HB is considered to remove power from one capacitor and transfer it to another (for the top most HB of Fig. 2, positive power flow is considered as power removed from $C8$ and sent to $C7$).

This capacitive power transfer scheme has the benefit of not requiring any inductive couplings, however, its cascading nature results in circulating currents, the entirety of which pass through the center HB that straddles the output node. This is because each capacitor must support the current of its adjacent capacitors. In the circuit of Fig. 2, the power needed to support C1 must come from the upper capacitors and pass through $C4$, $C3$ and $C2$ before it reaches $C1$. Likewise, power needed to support $C2$ must pass through $C4$ and $C3$ before it reaches $C1$.

This results in nonlinear component stress scaling with the number of levels. For this reason it is not recommended to be used outside of high conversion ratio and low power applications. More complete analysis on the circulating currents and scaling can be found in [9].

B. Case 2: Dual Active Half-Bridges

Dual active half bridges (DAHB) allow for the power transfer from a set of two adjacent capacitors to another set

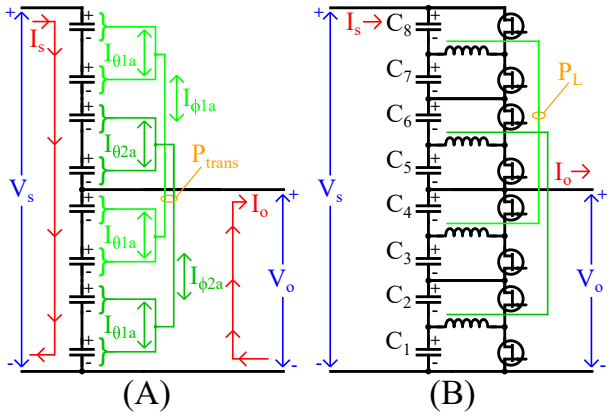

Fig. 3. 8-level dual active half-bridge (DAHB) implementation of the Manhattan Configuration. (a): Internal power flow diagram and notation. (b): Circuit schematic.

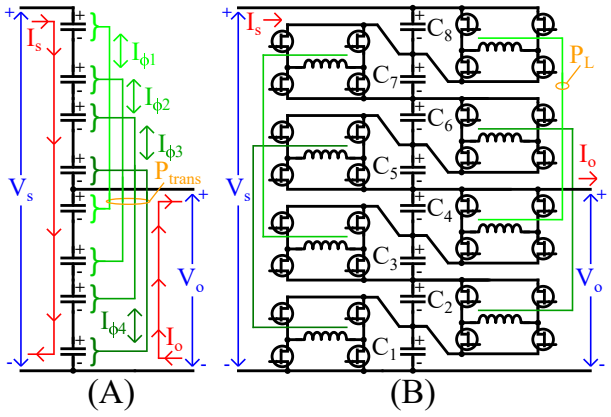

Fig. 4. 8-level dual active full-bridge implementation of the Manhattan Configuration. (a): Internal power flow diagram and notation. (b): Circuit schematic.

of two adjacent powers across an isolated inductive coupling. One set of two adjacent capacitors belongs to the set of upper capacitors and the complementary set of two adjacent capacitors belongs to the set of lower capacitors. The circuit that utilizes this technique can be seen in Fig. 3.

This DAHB circuit has a connectivity matrix $\mathbf{T_b}$ and link current vector I_b of

$$I_b = \begin{bmatrix} I_{\phi 1} \\ I_{\theta 1a} \\ I_{\theta 1b} \\ I_{\phi 2} \\ I_{\theta 2a} \\ I_{\theta 2b} \end{bmatrix} \mathbf{T_b} = \begin{bmatrix} 1 & 1 & 0 & 0 & 0 & 0 \\ 1 & -1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 1 & 0 \\ 0 & 0 & 0 & 1 & -1 & 0 \\ -1 & 0 & 1 & 0 & 0 & 0 \\ -1 & 0 & -1 & 0 & 0 & 0 \\ 0 & 0 & 0 & -1 & 0 & 1 \\ 0 & 0 & 0 & -1 & 0 & -1 \end{bmatrix}. \quad (19)$$

It is important to note the ascribed functionality of each DAHB. Each DAHB services a set of four capacitors. I_ϕ and I_θ represents the component of balancing capacitor current due to power flow across the inductive coupling and power flows within each individual half bridge, respectively. This can be visualized in Fig. 5-(b).

Transferring power over inductive couplings results in the elimination of the circulating currents present in the HB capacitive power transfer scheme. This is because power can flow directly from the upper set of capacitors to the lower set of capacitors without having to travel through any intermediate set of capacitors. This results in linear component stress scaling with number of levels.

C. Case 3: Dual Active Full-Bridges

Dual active full-bridges (DAFB) allow for power transfer between two capacitors across an isolated inductive coupling. Each DAFB services two capacitors, one upper capacitor and one lower capacitor. This allows for direct transfers of excess powers from an upper capacitor to a lower capacitor. The circuit that utilizes this technique can be seen in Fig. 4.

This DAFB circuit has a connectivity matrix $\mathbf{T_b}$ and link current vector I_b of

$$I_b = \begin{bmatrix} I_{\phi 1} \\ I_{\phi 2} \\ I_{\phi 3} \\ I_{\phi 4} \end{bmatrix} \mathbf{T_b} = \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \\ -1 & 0 & 0 & 0 \\ 0 & -1 & 0 & 0 \\ 0 & 0 & -1 & 0 \\ 0 & 0 & 0 & -1 \end{bmatrix}. \quad (20)$$

Each value in I_b represents the power transferred over each inductive coupling. This can be visualized in Fig. 5-(a). It is important to note the connectivity of each DAFB in this example. As it is drawn in Fig. 4, it is not strictly necessary to connect the inductive couplings in an alternating approach. As long as each inductive coupling traverses the output node the functionality of this capacative power transfer scheme is maintained (an outer-inner approach will also work). If this is not the case, then circulating currents identical to those of the HB example will be induced.

D. Case 4: Mixtures and Inductive Bus

Lastly, there are edge cases which deserve noting. The first of which is the sharing of a common inductive bus through which power flows from the upper set of capacitors to the lower set of capacitors. This can be implemented with DAHB or DAFB, the DAHB implementation can be seen in Fig. 6.

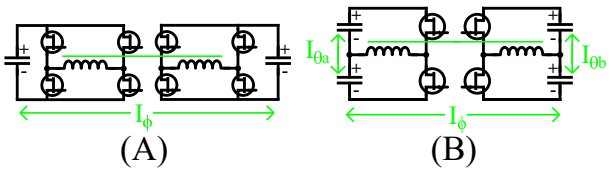

Fig. 5. (a): Power flows within the dual active full-bridge (DAFB). (b): Power flows within the dual active half-bridge (DAHB).

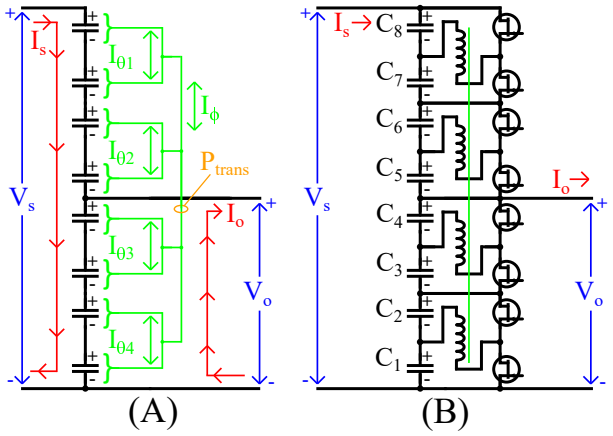

Fig. 6. 8-level dual active full-bridge implementation of the Manhattan Configuration with common inductive bus. (a): Internal power flow diagram and notation. (b): Circuit schematic.

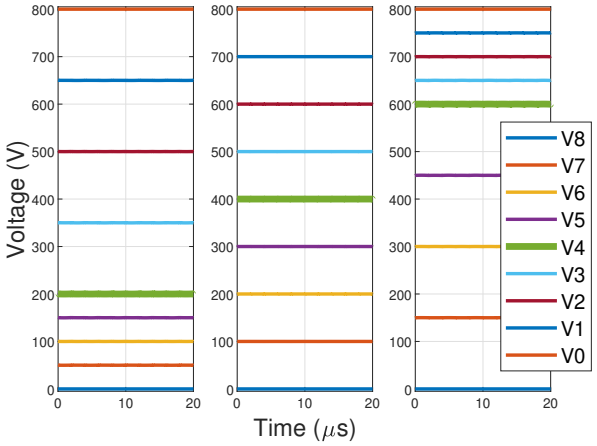

Fig. 7. Level voltages of the DAFB implementation. Left: $V_{out}/V_{in} = 0.25$. Center: $V_{out}/V_{in} = 0.25$. Right: $V_{out}/V_{in} = 0.25$.

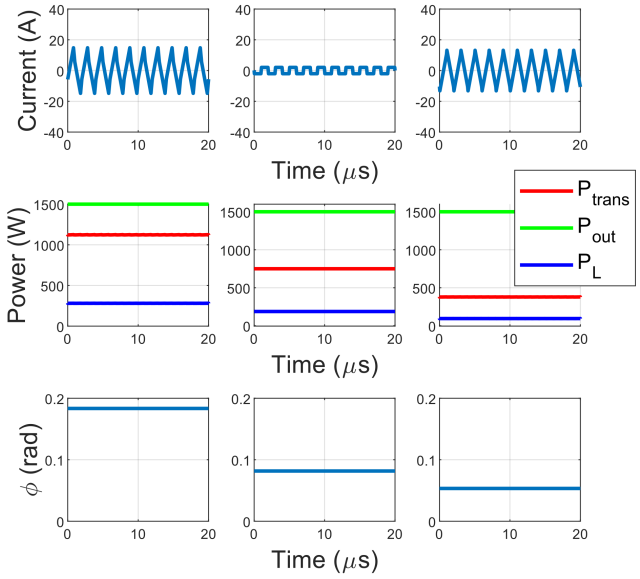

Fig. 8. Inductor currents (top row), internal power flows (middle row), and ϕ (bottom row) of the DAFB implementation. Left: $V_{out}/V_{in} = 0.25$. Center: $V_{out}/V_{in} = 0.25$. Right: $V_{out}/V_{in} = 0.25$.

This DAHB implementation of the common inductive bus has a connectivity matrix $\mathbf{T_b}$ and link current vector I_b of

$$I_b = \begin{bmatrix} I_\phi \\ I_{\theta 1} \\ I_{\theta 2} \\ I_{\theta 3} \\ I_{\theta 4} \end{bmatrix} \mathbf{T_b} = \begin{bmatrix} 1 & 1 & 0 & 0 & 0 \\ 1 & -1 & 0 & 0 & 0 \\ 1 & 0 & 1 & 0 & 0 \\ 1 & 0 & -1 & 0 & 0 \\ -1 & 0 & 0 & 1 & 0 \\ -1 & 0 & 0 & -1 & 0 \\ -1 & 0 & 0 & 0 & 1 \\ -1 & 0 & 0 & 0 & -1 \end{bmatrix}. \quad (21)$$

It is also worth noting that any mixture of the 3 types of capacitive power transfer mechanisms (HB, DAHB, and DAFB), both with and/or without a common inductive bus, can be used in a single converter. The only requirement is that whatever method is chosen can send sufficient power from the upper set of capacitors to the lower set of capacitors. As long as there is a path for each upper capacitor to send power to the lower set of capacitors and a path for each lower capacitor to receive power from the set of upper capacitors, capacitor voltage balance will be maintained in steady state.

IV. Validation

The capacitive power transfer mechanisms have been validated through hi-fidelity simulation. The HB methodology simulation results can be found in [9]. For the sake of brevity, only the results of the DAFB circuit of Fig. 4 are included in this paper. All capacitance values are set to the same value of 68μF and the leakage inductance of each coupled inductor, referred to the primary, is 4μH with a turns ratio $n = 1$. The switching frequency is 500kHz and the input voltage V_s is 800V. A resistive load is applied that changes value over the output voltage sweep to maintain a constant output power. P_{out} is set to 1.5kW and the output voltage is swept from $0.25V_{in} \leq V_{out} \leq 0.75V_{in}$.

All duty cycles are set to a static value of $D = 0.5$. The phase difference between opposing sides of each bridge ϕ, normalized to the switching period, is configured to be the same for all DAFBs within the converter. A single PI controller is implemented to find the required phase difference ϕ to achieve a desired output voltage V_{out}.

The level voltages, inductor currents, and power flows can be seen in Figs. 7 and 8. It can be seen that capacitors C1-C4 evenly split the output voltage V_o. Capacitors C5-C8 evenly split the difference between the input voltage and the output voltage $V_s - V_o$. Inductor current waveforms match typical DAFB performance. The power transferred over each inductive coupling P_L is the same for all DAFBs as they are all operating in a parallel manner. Total power transferred over all inductive couplings P_{trans} is less than the output power P_{out}. This is because the power that is required to move between capacitors to maintain capacitor voltage balance is always less than the output power and does not depend on the number of links nor

number of levels.

V. Benchmarking

One method of measuring the dynamic performance of each capacitive power transfer scheme is to calculate the theoretical maximum output voltage slew rate of each implementation. When the output voltage increases, the upper capacitors must discharge and the lower capacitors must charge through their respective capacitive power transfer links and vice versa. This can potentially be a bottleneck if the links saturate.

To demonstrate this, each of the 4 cases is considered with obfuscated power transfer links. The maximum power that can be transferred across each of these links is set to an arbitrary maximum of 1kW per link. An input voltage V_s of 800V is applied with a desired output voltage V_o transient from 200V to 600V. The same circuit parameters are used in this section as in the previous section and the case of no output load is considered. The slew rate is normalized to the number of links.

Using the equation for energy stored in a capacitor

$$E_{cap} = \frac{1}{2}CV^2, \tag{22}$$

it can be calculated that the set of upper capacitors must lose 1088J of energy and the set of lower capacitors must gain 1088J of energy. Individually, each upper capacitor must lose 272J of energy and each lower capacitor must gain 272J of energy. The slew rate results for each circuit, along with component quantity scaling as a function of number of levels N can be seen in Table I.

The HB scheme suffers a strong bottleneck as a single link I_4 serves to transfer all the power from the set up upper capacitors to the set of lower capacitors. This results in a time of 1.088s with a slew rate of 368V/s to complete the output step. It is also important to note that the total power transferred over the inductive couplings is greater than the required power transfer due to the cascading nature of the power transfer links. For the example used in this exercise, I_1 transfers 272J of energy, I_2 transfers $2 * 272$J, I_3 transfers $3 * 272$J, etc... with the end result being that 4352J of energy in total is transferred across the couplings.

The DAHB and DAFB schemes do not have an individual bottleneck link as power transfer is evenly split amongst all the inductive couplings. However, as the DAFB scheme has 2x the number of links as the DAHB scheme, it can complete the transient step twice as fast as the DAHB scheme. This results in a slew rate of 736V/s for the DAHB scheme and 1472 for the DAFB scheme.

TABLE I
Benchmarking Capacitive Power Transfer Techniques

Criteria	HB	DAHB	DAFB	Common L
Slew Rate (V/s)	368	736	1472	368
Normalized Slew Rate (V/s)	52.5	368	368	368
E_{trans} (J)	4352	1088	1088	1088
FET Quantity	$2(N-1)$	N	$4N$	N
Inductor Quantity	$N-1$	$N/4$	$N/2$	1
Capacitor Quantity	N	N	N	N

Lastly, for the Common inductive coupling case, it can be seen that it suffers from the same bottleneck as the HB case with all the power being transferred across a single link. However, as there is no cascading of links, the total power transferred over all links is equal to the total power transfer required to maintain capacitor voltage balance.

VI. Conclusion

The results presented in this paper show that the proposed stacked capacitor topological framework functions effectively as a multilevel converter. Defining the nature of the topology as a set of series capacitors is purposefully broad as the capacitive power transfer method, necessary for the functionality of the converter, is not inherently a property of the topological framework. It is shown that the component quantities scale linearly with the number of levels and, depending on the capacitive power transfer method chosen, the component stresses can also scale linearly. Finally, the power transferred between capacitances internally is less than the output power the of converter, an attribute unique to the proposed framework. Further work includes physical experimental validation and investigation into optimal control methods.

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