2022 IEEE International Symposium on Electromagnetic Compatibility & Signal/Power Integrity (EMCSI) | 978-1-6654-0929-2/22/$31.00 ©2022 IEEE | DOI: 10.1109/EMCSI39492.2022.9889339

Optimizing the Placement of Non-Functional Pads on Signal Vias Using Multiple Reflection Analysis

Muqi Ouyang
Missouri S&T EMC Laboratory
Missouri University of Science and Technology
Rolla, MO, USA
ouyangm@mst.edu

Kevin Cai
Unified Computing System
Cisco Systems, Inc
San Jose, CA, USA
kecai@cisco.com

Chaofeng Li
Missouri S&T EMC Laboratory
Missouri University of Science and Technology
Rolla, MO, USA
clf83@mst.edu

Anna Gao
Unified Computing System
Cisco Systems, Inc
San Jose, CA, USA
annagao @cisco.com

Felen Fu
CRDC
Cisco Systems, Inc.
Shanghai, China
fefu@cisco.com

Hannah Bian
CRDC
Cisco Systems, Inc.
Shanghai, China

Bidyut Sen
Unified Computing System
Cisco Systems, Inc.
San Jose, CA, USA
bisen@cisco.com

DongHyun Kim
Missouri S&T EMC Laboratory
Missouri University of Science and Technology
Rolla, MO, USA
dkim@mst.edu

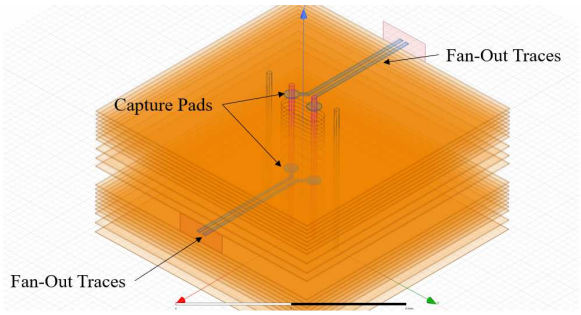
***Abstract*—In this study, the effects of using non-functional pads to optimize the performance of high-speed signal vias are investigated based on multiple reflection analysis. The non-functional pads on signal vias introduce more capacitive coupling and are possible to improve the response of the via structure if the original via has relatively larger impedance compared to the system reference impedance. The effectiveness of the non-functional pad optimization is validated through a numerical example, and the eye diagram of the via structure without and with non-functional pads are compared. The eye opening becomes 5.4 times larger after the via optimization using non-functional pads.**

Keywords—multiple reflections, non-functional pad, signal integrity, via optimization

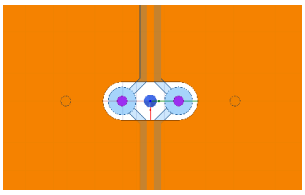
I. INTRODUCTION

When designing printed circuit boards, vias are widely used to make conductive connections for metals on different layers. Due to the physical geometries of the vias and the nearby metals on different PCB layers, the distance between the signal path on the via and the return current path keeps changing at different via locations, where reflection could occur. Therefore, the discontinuities of the impedance always exist on vias. Apart from this impedance discontinuities, there are usually capture pads, or functional pads, on the fan-out layers of a via, as shown in Fig. 1. When a high-speed signal trace approaches to a via transition structure, it will first lose the reference plane beneath it due to the anti-pad structure, and then a much wider capture pad shows up, followed by the via with changing impedance. All of these issues introduce negative impacts to the performance of high-speed signal channels and can cause serious signal distortions on the received signal.

The target data rate on modern high-speed systems becomes much higher in recent years, and PCBs with 112 Gbps channels have been developed [1]. The negative impacts introduced by via discontinuities must be well controlled during the design process. The most straight forward solution is to avoid via transitions for high-speed channels, but in most of the designs, changing routing layers is necessary and via transition structures are unavoidable. Therefore, many methods have been proposed and implemented by signal integrity engineers to optimize the performance of via transitions to minimize the negative impacts due to the vias. In [2-4], the methods to optimize the via transition structures by tuning the physical geometries, including via diameter, anti-pad size, capture pad size, nearby GND vias, have been discussed in detail, and the effects of



(a)



(b)

Fig. 1. An example of a PCB via structure in the full-wave simulation (a) the side view; and (b) the top view.

This work is supported in part by the National Science Foundation under Grant No. IIP-1916535.

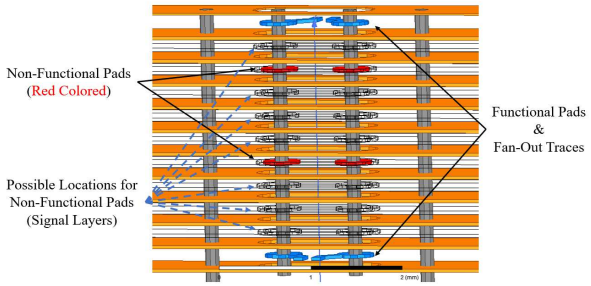


Fig. 2. An example of PCB vias with non-functional pads (red pads) and functional pads (blue pads)

adding diving board like structures are also discussed in [2]. In [5], the physics of coupling between the signal via and reference return path was investigated, and the capacitance introduced by capture pads on signal vias are evaluated using TDR impedance waveforms. In [6], the effect of non-functional pads on both signal vias and nearby GND vias was studied, but the methods to optimize the via transition performance with non-functional pads were not discussed. Non-functional pads have similar geometries compared to capture pads (functional pads) on fan-out layers, but non-functional pads do not connect to any traces to fan out, as shown in Fig. 2. Due to the PCB manufacture technology, non-functional pads can only be placed at the locations of metal layers, not the places in the middle of a substrate between two adjacent layers.

In this study, the via transition optimization method is investigated by analyzing the multiple reflections on signal vias. Generally, adding non-functional pads on signal vias introduces more capacitive coupling between the signal via and the reference, so the equivalent characteristic impedance will be lower compared to the same via without additional non-functional pads. Therefore, if the original via has an equivalent characteristic impedance higher than the system impedance, it is possible to optimize the via transition by lowering the impedance value using the additional non-functional pads. Although the possible locations for adding the non-functional pads are limited to the locations with PCB layers, the number of added non-functional pads and their locations need to be chosen carefully to achieve the optimized performance of the via transition structure. The multiple reflection analysis is based on the analytical formulations developed in [7, 8] for cascaded signal channel analysis. The most important advantage for this multiple reflection analysis method compared to the common ABCD-parameter or T-parameter matrices multiplication calculation for cascaded channels is that each individual ripple observed in the time-domain single-bit response can be backtracked. Therefore, the most critical ripples and the corresponding signal propagation paths can be identified in the multiple reflection analysis, and the solutions for channel optimizations can be easily determined.

II. Multiple Reflection Analysis

The detailed discussions on the multiple reflection analysis and the applications on cascaded channel optimizations were included in [7, 8], and the related formulations are also briefly introduced in this section.

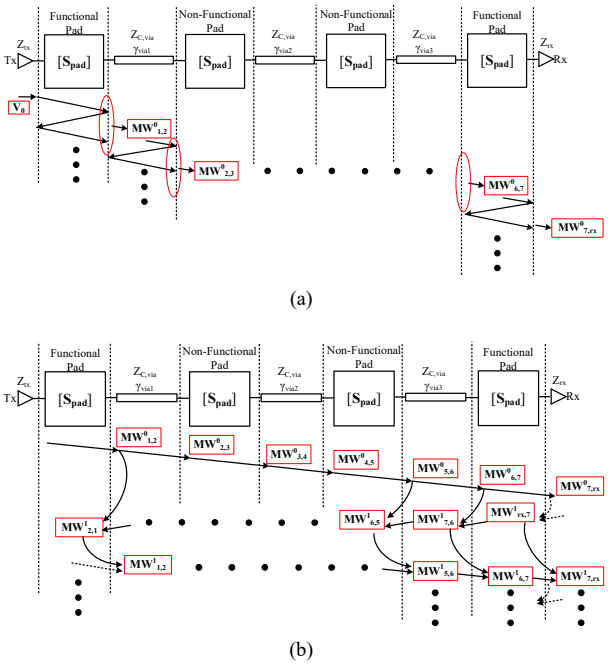


Fig. 3. An example of wave multiple reflections in a cascaded channel (a) reflections inside a single segment; and (b) reflections between multiple channel segments.

A. Multiple Reflection Formulation

The formulation of multiple reflections in a cascaded channel is developed based on the wave propagations and reflections in the channel. The analysis on the wave reflections is separated into two different parts: wave reflections inside a single segment of the cascaded channel and wave reflections between multiple channel segments. These two different wave reflections in a cascaded channel with 3 transmission-line segments, two functional pads and two non-functional pads are shown in Fig. 3. The effects of the functional pads and non-functional pads are modeled using S-parameter networks in the cascaded channel. The functional pads are located right after the transmitter and right before the receiver, and the via channel is divided into 3 segments by the two more non-functional pads in the middle.

1) Reflections inside a single segment

For $1 \le A < +N$, the wave incident from the A^{th} segment to the $(A+1)^{th}$ segment in Fig. 3(a) can be calculated by

$$MW^0_{A,A+1}(M) = V_0 \mathrm{T}_{tx,1} \prod_{i=1}^{A} \left[e^{-\gamma_i l_i} \cdot T_{i,i+1} \cdot CM_i(M) \right] \qquad (1)$$

where M is the number of reflected wave inside the segment considered in the calculation, and

$$CM_i(M) = \frac{1 - \left(\Gamma_{i,i+1}\Gamma_{i,i-1}e^{-2\gamma_i l_i}\right)^{M+1}}{1 - \Gamma_{i,i+1}\Gamma_{i,i-1}e^{-2\gamma_i l_i}} \qquad (2)$$

$$\lim_{M\to\infty} CM_i(M) = \frac{1}{1 - \Gamma_{i,i+1}\Gamma_{i,i-1}e^{-2\gamma_i l_i}} \qquad (3)$$

In addition, the transmission coefficient T and the reflection coefficient Γ from the segment i to segment j are defined as

$$\mathrm{T}_{i,j}(\omega) = \frac{2Z_{C,j}(\omega)}{Z_{C,j}(\omega) + Z_{C,i}(\omega)} \tag{4}$$

$$\Gamma_{i,j}(\omega) = \frac{Z_{C,j}(\omega) - Z_{C,i}(\omega)}{Z_{C,j}(\omega) + Z_{C,i}(\omega)} \tag{5}$$

2) Reflections between multiple segments

$MW_{i,j}^{M'}$ in Fig. 3(b) indicates the total wave incident from the i^{th} segment to the j^{th} segment, and the superscript M' is defined as the number of reflections between multiple segments considering in the calculation.

Since no further discontinuity exists before the transmitter or after the receiver, so

$$MW_{0,1}^{M'}(M) = MW_{tx,1}^{M'}(M) = 0 \tag{6}$$

$$MW_{N+1,N}^{M'}(M) = MW_{rx,N}^{M'}(M) = 0 \tag{7}$$

When $M' = 0$, the value of $MW_{A,A+1}^{0}$ can be calculated using (1).

For $M' > 0$, the backward components:

$$MW_{A+1,A}^{M'}(M) = \left[MW_{A,A+1}^{M'-1}(M) \cdot e^{-\gamma_{A+1} l_{A+1}} \Gamma_{A+1,A+2} + MW_{A+2,A+1}^{M'}(M)\right] \cdot e^{-\gamma_{A+1} l_{A+1}} \mathrm{T}_{A+1,A} CM_{A+1}(M) \tag{8}$$

for $1 \le A \le N-1$.

Then, for $M' > 0$, the forward components:

$$MW_{A,A+1}^{M'}(M) = \left[MW_{A+1,A}^{M'}(M) \cdot e^{-\gamma_A l_A} \Gamma_{A,A-1} + MW_{A-1,A}^{M'}(M)\right] \cdot e^{-\gamma_A l_A} \mathrm{T}_{A,A+1} CM_A(M) \tag{9}$$

for $1 \le A \le N$.

3) Transmission coefficient for the cascaded channel

Ideally, to calculate the transmission coefficient of the cascaded channel, or $S_{21}(\omega)$ of the channel, all the wave reflections in the cascaded channel need to be considered, i.e., $M \to \infty$ and $M' \to \infty$, and

$$S_{21}(\omega) = \frac{1}{V_0} \lim_{M,M' \to \infty} \sum_{k=0}^{M'} MW_{N,N+1}^{k}(\omega, M) \tag{10}$$

The details on the formulation derivation from (1) to (10) are not presented in this section and the detailed steps on formulation derivation can be found in [6].

B. Handling on the Via Pad Capacitance

The effects of both functional pads and non-functional pads are modeled using simplified lumped circuit elements, as shown in Fig. 4.

As discussed in the previous section, the functional pads on the fan-out layers and the additional non-functional pads on the via introduce additional capacitive coupling, and can be modeled using a shunt capacitor. The two impedance elements in the T-network shown in Fig. 4 are small resistors representing the loss on the via pads.

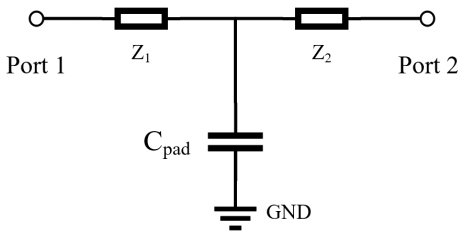


Fig. 4. The T-network to model the effects from the non-functional pads and functional pads.

To include the circuit network for the via pad in the cascaded channel evaluation, the Z-parameter matrix of this T-network is determined first:

$$\mathbf{Z} = \begin{bmatrix} Z_1 + \frac{1}{j\omega C_{pad}} & \frac{1}{j\omega C_{pad}} \\ \frac{1}{j\omega C_{pad}} & Z_2 + \frac{1}{j\omega C_{pad}} \end{bmatrix} \tag{11}$$

and the S-parameter of this network can be obtained from Z-parameter to S-parameter conversion [9].

The method to handle S-parameter network in the cascaded channel is presented in detail in [8]. The basic idea is to add pseudo segments at all S-parameter network ports. The pseudo segments are zero-length, no loss and the characteristic impedance is the reference impedance of the S-parameter network. There are two kinds of reflections at the S-parameter port: 1) the reflection due to impedance mismatch between the external transmission-line impedance and the S-parameter reference impedance and 2) the reflection from inside of the S-parameter network (return loss). These two kinds of reflections are separated at two sides of the pseudo segment for individual analysis. Therefore, after adding the pseudo segments at S-parameter network ports, the same formulations from (1) to (10) can be used for the cascaded channel evaluation.

C. Modeling of Signal Via with Non-Functional Pads

Generally, vias on PCB are much shorter compared to other parts of the total signal channel, and the conductive loss and the dielectric loss on PCB vias are usually negligible. Therefore, the PCB via for multiple reflection analysis and optimization can be modeled using lossless and frequency-independent transmission-line segments connected with the S-parameter network of the via pads, as shown in Fig. 5(a).

Theoretically, the non-functional pads can be added on the via locations of all the signal layers. However, in practical cases, adding non-functional pads may introduce too much capacitive coupling. Therefore, the designs with two non-functional pads are discussed in the following section. Apart from the non-functional pads, there are two functional pads on both sides of the via and the effects of the via stub on the receiver side is included.

D. Multiple reflection analysis & eye diagram calculation

After modeling the signal via with non-functional pads, the transmission coefficient (insertion loss) of the channel can be calculated using (10). Based on the calculated transmission coefficient of the cascaded channel, the single-bit response of

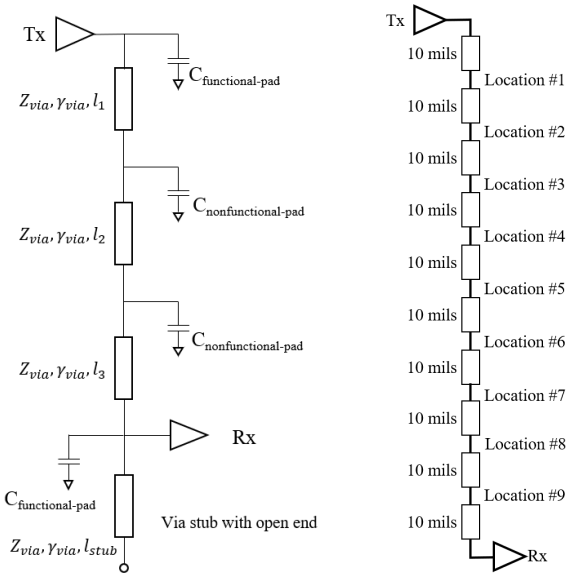


Fig. 5. The schematic of a via with two non-functional pads: (a) the via segments and the via stub; and (b) the possible locations for the non-functioanl pads on the via.

the channel can be calculated, and an example of the calculated single-bit response waveform is shown in Fig. 6. The single-bit input in the calculation is defined using a Gaussian pulse with limited bandwidth so that the unimportant very high frequency components due to fast rising and falling edges are neglected in the calculation. The data rate of the single-bit input is 56 Gbps in Fig. 6. In this single-bit response, the dispersion on the shape of the output waveform as well as the small ripples after the main pulse can be clearly observed.

The details of using the multiple reflection analysis method to optimize the signal integrity performance of a cascaded channel have been discussed in [8]. Based on the analysis method, the single-bit response can be divided into each individual ripple with different reflections and propagation paths in the cascaded channel, and the separated ripples of the single-bit response are shown in Fig. 7.

Since the propagation paths and the reflections of each individual ripples in Fig. 7 can be backtracked using the multiple reflection analysis, the response of the cascaded channel can be optimized by the following steps:

Step 1: identify the most critical ripples. The ripples arrive later and have larger magnitudes can introduce larger negative impacts on the signal integrity performance.

Step 2: tune the parameters related with those critical ripples and the main pulse. The parameters to be tuned in this study is the locations of the non-functional pads.

Step 3: achieve the largest main pulse magnitude and the smallest ripples by tuning the parameters of the channel and validate the optimization by evaluating the eye opening in the channel's eye diagram simulation.

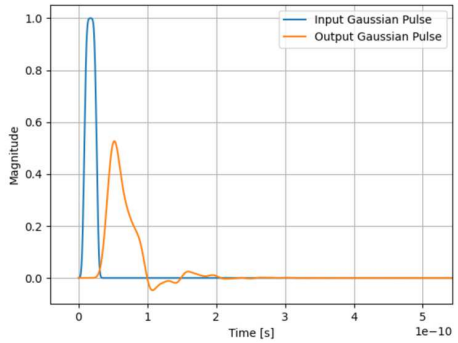


Fig. 6. An example of the calculated single-bit response.

The eye diagram is calculated using the transmission coefficient of the cascaded channel from (10), and a 56-Gbps PRBS is used as the input for the eye-diagram calculation. Rising and falling edges are 30 % of the UI, and the eye opening can be measured after the eye diagram calculation.

III. Numerical Analysis and Discussions

In [7, 8], it has been discussed that the multiple reflections in differential channels can be analyzed by converting the differential channels to odd-mode channels.

Assume the total length of the active via ($l_1 + l_2 + l_3$) is 100 mils; the length of the via stub at the receiver side is 8 mils; the capacitances of the functional pads and the non-functional pads are 0.3 pF and 0.2 pF, respectively. In addition, for the lossless frequency-independent via structure (vertical), $Z_{via} = 60\ \Omega$ and $\gamma_{via} = j\omega \cdot \frac{\sqrt{\varepsilon_r}}{c_0} \cdot l$. The load impedance at the transmitter and the receiver is 42.5 Ω, and $\varepsilon_r = 3.7$. The target data rate for the channel is 56 Gbps.

On the 100-mil via structure, it is assumed that there are 9 possible locations for non-functional pads and the distances between any two possible locations are 10 mils. These possible locations are distributed uniformly on the via. Then, define the location #1, #2, #3, …, #9 at the locations where their distance to the transmitter are 10 mils, 20 mils, 30 mils, …, 90 mils, as shown in Fig. 5(b).

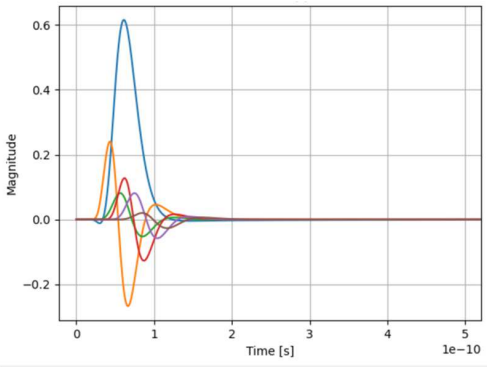


Fig. 7. An example of the separated ripples in the single-bit response.

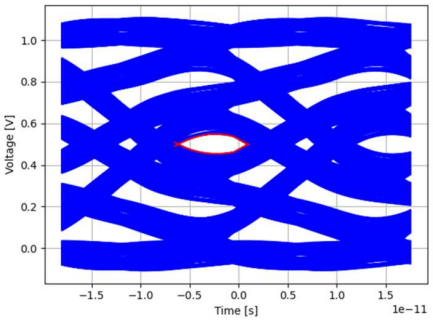


Fig. 8. The eye diagram of the via structure without non-functional pad

A. *The Original Via without Non-Functional Pad*

At first, the original via without non-functional pad is evaluated, and the eye diagram of the via structure is shown in Fig. 8.

For the original via structure without non-functional pad, there is only a small eye opening ($0.0953\ V \times 7.05\ ps$). This small eye opening at the receiver can lead to large bit-error-rate of the system. Optimizations on the original via is necessary.

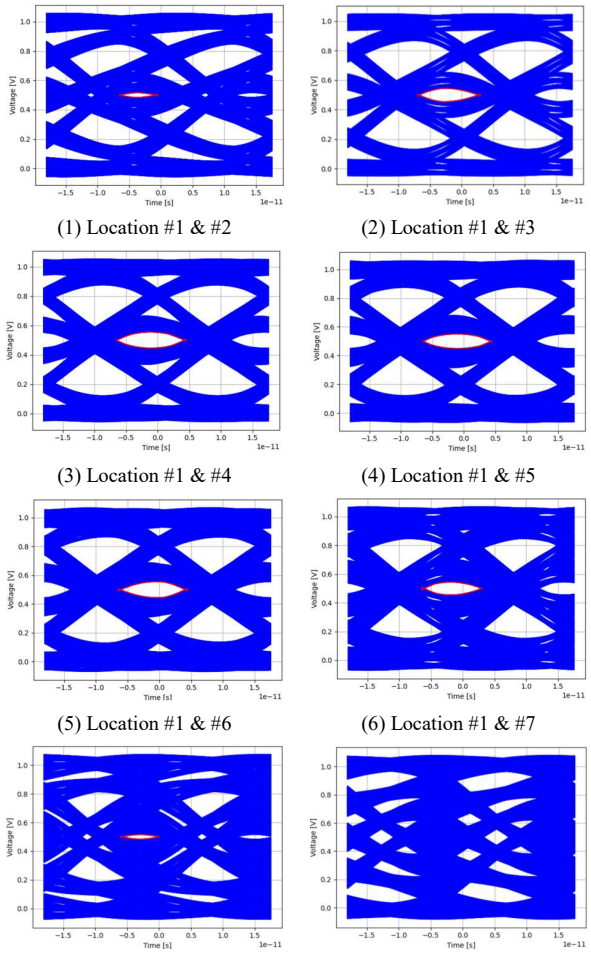


Fig. 9. The eye diagram of the via structure with two non-functional pads at different locations

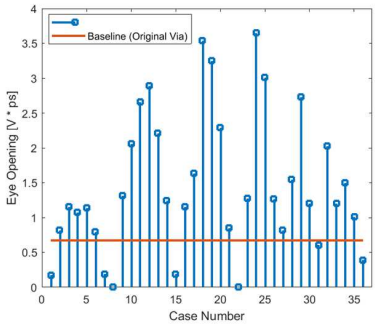


Fig. 10. The eye opening of the via structure with two non-functional pads at different locations

B. *Via with Non-Functional Pad Equations*

Based on the discussions in the previous section, adding non-functional pads on the via with larger characteristic impedance can increase the capacitive coupling and may improve the performance of the via structure. However, adding the non-functional pads does not guarantee an improvement on the channel performance. For example, when assigning the two non-functional pads at location #1 and location #2, the eye opening (Fig. 9-1) is $0.0317\ V \times 5.41\ ps$, which becomes worse compared to the original via structure.

Therefore, to optimize the via structure using non-functional pads, the choice of non-functional pad locations needs to be

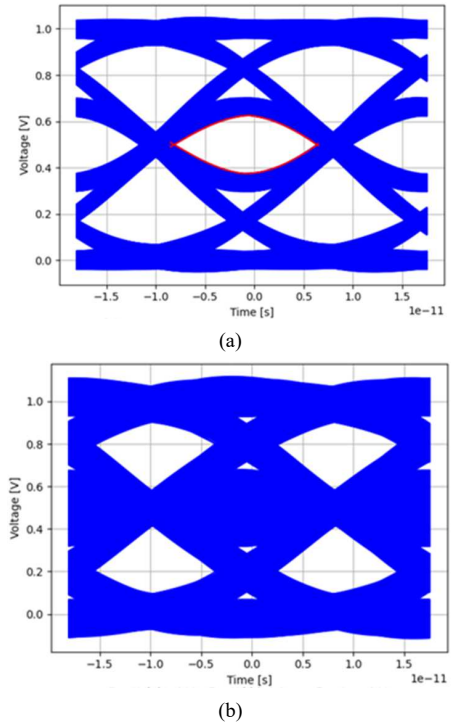


Fig. 11. (a) the best-case eye diagram when non-functioanl pads at location #4 and location #7; and (b) the worst-case eye diagram when non-functioanl pads at location #1 and location #9

determined carefully. To choose two non-functional pad locations in the total 9 locations, there are in total 36 combinations (Location #1 & #2, Location #1 &#3, Location #1 & #4, ……, Location #7 & #9, and Location #8 & #9). Use the eye opening of the original via structure as the baseline, and the eye openings under each non-functional pad configurations are shown in Fig. 10.

When the two non-functional pads are relatively far away from the transmitter or the receiver, the eye diagram of the via tends to have better eye-opening performance. In the worst case, one non-functional pad is close to the transmitter, and the other non-functional pad is close to the receiver. The eye diagrams of the best case and the worst case is shown in Fig. 11.

The worst-case eye is completely closed, and the best-case eye opening is $0.2538\ V \times 14.38\ ps$, which is about 5.4 times larger compared to the eye opening of the original via structure without non-functional pad.

IV. Conclusion

In this paper, using non-functional pads to optimize the performance of high-speed via structure is discussed based on multiple reflection analysis. When the original via has relatively larger characteristic impedance compared to the system reference impedance, it is possible to use non-functional pads to increase the capacitive coupling and improve the performance of the via structure. If the locations of non-functional pads are well designed, effective improvement on the eye opening at the receiver of the channel can be expected without adding layout complexity.

References

[1] H. Wu, M. Shimanouchi and M. PengLi, "Effective Link Equalizations for Serial Links at 112 Gbps and Beyond," *2018 IEEE 27th Conference on Electrical Performance of Electronic Packaging and Systems (EPEPS)*, San Jose, CA, USA, 2018, pp. 25-27.

[2] S. Jin, J. Zhang and J. Fan, "Optimization of the transition from connector to PCB board," *2013 IEEE International Symposium on Electromagnetic Compatibility*, Denver, CO, USA, 2013, pp. 192-196.

[3] A. Vardapetyan and C. -J. Ong, "Via Design Optimization for High Speed Differential Interconnects on Circuit Boards," *2020 IEEE 29th Conference on Electrical Performance of Electronic Packaging and Systems (EPEPS)*, San Jose, CA, USA, 2020, pp.

[4] Q. Dong, K. Cai, A. Gao and B. Sen, "Automated 3D discontinuity optimization with speed sensitivity for high-speed Serdes channels," *2021 IEEE International Joint EMC/SI/PI and EMC Europe Symposium*, Raleigh, NC, USA, 2021, pp. 977-981.

[5] J. N. Hu, N. K. H. Huang and B. -C. Tseng, "Via Design Optimization for Server Applications," *2020 International Symposium on Electromagnetic Compatibility - EMC EUROPE*, Rome, Italy, 2020, pp. 1-3.

[6] A. C. Scogna, "Signal integrity analysis of a 26 layers board with emphasis on the effect of non-functional pads," *2008 IEEE International Symposium on Electromagnetic Compatibility*, Detroit, MI, USA, 2008, pp. 1-6.

[7] M. Ouyang *et al*., "An Investigation on Multiple Reflections and Group Delay Behavior in High-Speed System Designs," *2021 IEEE International Joint EMC/SI/PI and EMC Europe Symposium*, Raleigh, NC, USA, 2021, pp. 423-428.

[8] M. Ouyang *et al*., "Novel Formulations of Multi-Reflections and Their Applications to High-Speed Channel Design," submitted to IEEE Transactions on Signal and Power Integrity.

[9] D. M. Pozar, *Microwave Engineering*, 4th ed. New York, NY, USA: Wiley, 2012.