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PEEC-Based On-chip PDN Impedance Modeling Using Layered Green's Function

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***Abstract*—This paper presents an impedance model of on-chip power distribution network (PDN), which is an efficient criterion for estimating simultaneous switching noises (SSNs) on 3-D integrated circuit (IC). The impedance of on-chip PDN, including the effect of silicon substrate, is accurately modeled based on partial element equivalent circuit (PEEC) and layered Green's function (LGF). The equivalent circuit model of PDN is extracted based on the physical dimensions and electrical material characteristic of PDN at first. And then the LGF is used to consider the effect of silicon substrate for improving the accuracy of on-chip PDN impedance model. The effectiveness of proposed model has been validated by full wave simulation. The high order resonance of PDN impedance can also be accurately predicted.**

***Keywords*—impedance modeling, PDN, PEEC, LGF, SSNs, silicon substrate**

I. Introduction

Simultaneous switching noises (SSNs) on 3-D stacked memory Integrated Circuit (IC) in gigahertz range is becoming more and more serious challenge with the increase of bandwidth and power consumption, which obviously degrade the performance and reliability of the IC [1]-[2]. To estimate the SSNs generation and evaluate the Power Distribution Network (PDN) design for 3-D IC, calculation of PDN impedance is found to be an efficient criterion because a high impedance level across a high bandwidth might generate a large amount of SSNs. In other words, it is really useful to accurately model the impedance of on-chip PDN for estimation of SSNs [3]-[6]. Because the dimension range of on-chip PDN is wide and the geometry and material are complex, it is difficult to obtain the impedance of on-chip PDN with separated power and ground current paths by full-wave simulation as mentioned in [6].

In recent years, many methods have been proposed to model the impedance of on-chip PDN based on partial element equivalent circuit (PEEC) method. In [3], an impedance modeling method of PDN based on resonant cavity model was proposed. But the method can only be applied to low frequency range that below gigahertz. A segmentation-based method of modeling on-chip PDN impedance was proposed in [4]-[6]. But they don't consider the effect of lossy silicon substrate which would introduce some deviations on modeling. The effect of silicon substrate was modeled as series capacitors between the substrate and power/ground (P/G) line in [7]-[12]. However, these methods still cannot predict the impedance of on-chip PDN accurately, especially near the resonance frequency.

In our proposed method, the impedance model of on-chip PDN is established based on PEEC method and layered Green's function (LGF). Firstly the unit cell of PDN is extracted based on a segmentation method. Then the equivalent circuit of unit cell is modeled by PEEC method. The equivalent circuit of whole PDN is presented by connecting the equivalents circuits of all unit cells. Because the lossy silicon substrate right below on-chip PDN could affect the capacitive couplings between metal lines of on-chip PDN, the LGF was introduced to achieve the right capacitance between metal lines. By means of considering the effect of lossy silicon substrate, the accuracy of impedance modeling of on-chip PDN is improved. Compared with the existing method, which added additional capacitors into equivalent circuit of PDN mentioned above, the proposed

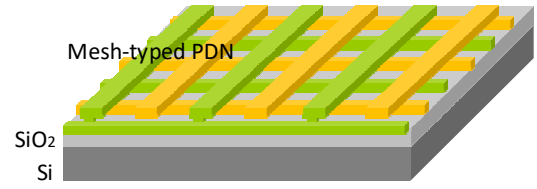

Fig. 1. On-chip PDN structure.

equivalent circuit would be more efficient. Because the capacitive coupling between P/G line is calculated by LGF including the effect of silicon substrate. Ultimately, some simulation results from HFSS are used to validate the effectiveness of the proposed method.

II. Methodology

The on-chip PDN is constructed by mesh-typed P/G PDN, insulator of silicon dioxide and silicon substrate, as shown in Fig. 1. In reality, the PDN is in silicon dioxide area above silicon substrate. The mesh typed PDN with silicon oxide medium can be modeled as equivalent *RLC* circuit based on PEEC method. The *RLC* parameters are extracted based on the physical dimensions and electrical material characteristic of PDN and silicon oxide medium.

On-chip PDN environment can be treated as multilayer structure. Then the LGF is used to take account into the effect of silicon substrate to guarantee an accurate impedance model of on-chip PDN.

A. Proposed PDN Impedance Model

The mesh-typed PDN can be separated into small unit cells as shown in right-top of Fig. 2. One unit cell can be represented as equivalent *RLC* circuit as shown in the right-bottom of Fig. 2. R and L are the partial resistances including the skin effect and the partial self-inductances of the P/G lines of PDN, respectively. To accurately model the PDN impedance, the mutual-inductance L_m between parallel P/G lines of PDN on same layer are considered. C_{m1} is the partial mutual capacitances between cross P/G lines on different layers while C_{m2} is the partial mutual capacitances between parallel P/G lines on same layer of PDN as shown in Fig. 2.

Resistance calculation here is defined as

$$R = \frac{L_p}{L_w \cdot t \cdot \sigma}\sqrt{1+\alpha \cdot f} \quad (1),$$

where σ is the conductivity of P/G metal line. L_p is the pitch between power and ground line. L_w and t is the width and thickness of the P/G lines. α is the correction factors for skin effect, which is related to the thickness and conductivity of metal lines [9], [11]. For on-chip PDN where the P/G metal lines are very close to each other that means the current pass through in one metal line could be affected by the current in near metal line. Therefore the skin effect in on-chip PDN is really important. f represents the frequency and indicates a high frequency portion for resistance.

The formulation for partial inductance calculation [13] here is

$$L = \frac{1}{t^2 \cdot L_w^{\,2}} \int_{V_i}\int_{V_j} G_A dV_i dV_j \quad (2)$$

where G_A is the corresponding vector potential Green's function for inductance calculation which relates to permeability of silicon oxide medium. $V_{i/j}$ is the volume of the mental line. When $i = j$, it represents the self-inductance L. When $i \neq j$, it is the mutual-inductance L_m.

The partial mutual capacitance between power line and ground line is calculated from sub-coefficients of capacitance

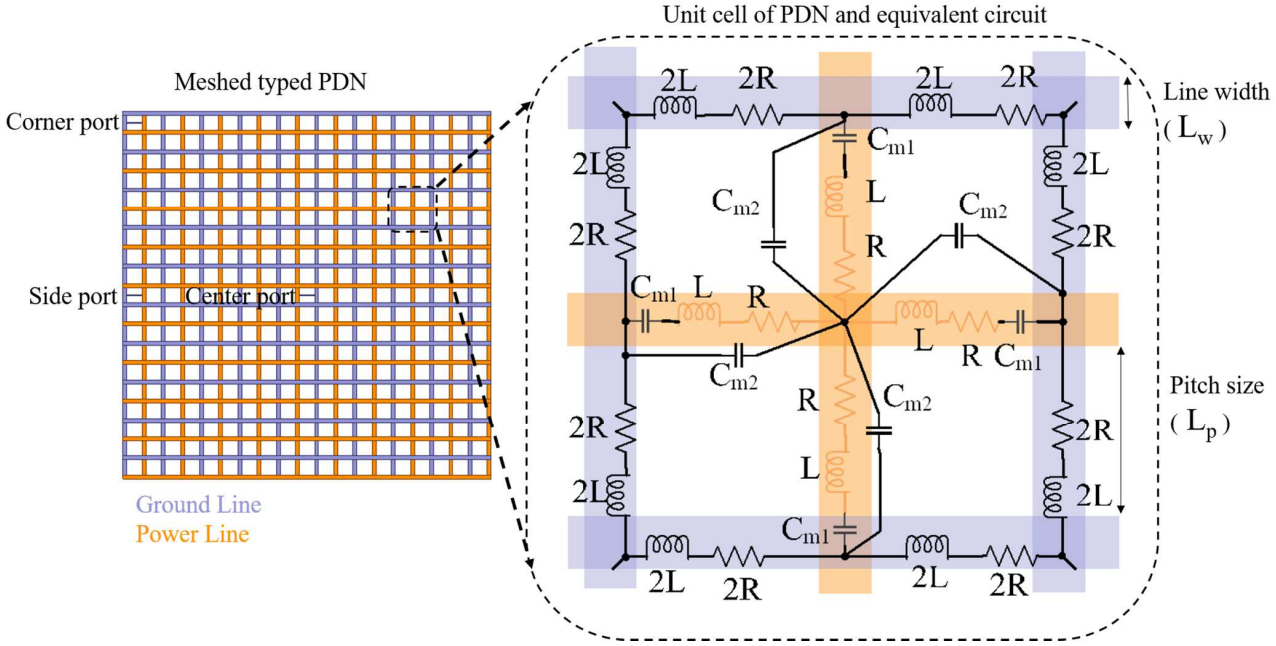

Fig. 2. Top view of mesh-typed P/G PDN and the equivalent circuit of PDN unit cell.

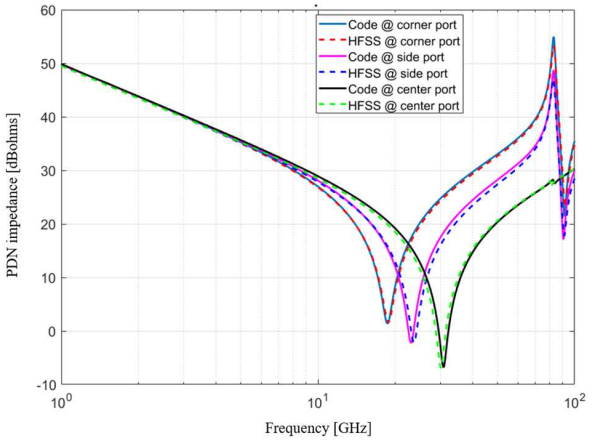

Fig. 3. PDN impedance comparison from our code and HFSS for three port positions.

c_s [14]. And c_s is calculated as $c_s = ps^{-1}$. Here ps is the coefficient of potential matrix and is defined as

$$ps = \frac{1}{S_p \cdot S_g} \int_{S_p} \int_{S_g} G_\phi dS_p dS_g \tag{3}$$

Here, G_ϕ is the corresponding scalar potential Green's function for capacitance calculation which relates to the permittivity of silicon oxide medium. In on-chip PDN impedance modeling, G_ϕ should include the effect of silicon oxide medium where the PDN located in. S_p and S_g are the surface area of power line and ground line, respectively.

B. Considering the Effect of Silicon Substrate Using LGF

Because on-chip PDN structure can be treated as multilayer medium, LGF is used here to consider the effect of silicon substrate. From the LGF analysis of layered medium in [15]-[16] for 3-D IC/packaging systems, the vector potential G_A is dominated by the direct coupling, but the scalar potential G_ϕ is dominated by direct coupling and complex images due to the lossy silicon substrate. The complex image term of Green's function can be extracted by the discrete complex image method [14] as

$$G_{ci} = \sum_N \frac{1}{4} a_i \frac{e^{-jkr_i}}{r_i} \tag{4}$$

where k is the wavenumber of the layer of metal line, N represents the number of complex images, a_i is the complex image coefficients and r_i relates to the complex image locations. Thus equation (3) is changed to (5).

$$ps = \frac{1}{S_p \cdot S_g} \int_{S_p} \int_{S_g} G_\phi + G_{ci} dS_p dS_g \tag{5}$$

The effect of silicon substrate is included in the capacitance of equivalent circuit of PDN. Because it doesn't add additional circuit component of capacitance, the equivalent circuit of PDN is simplified.

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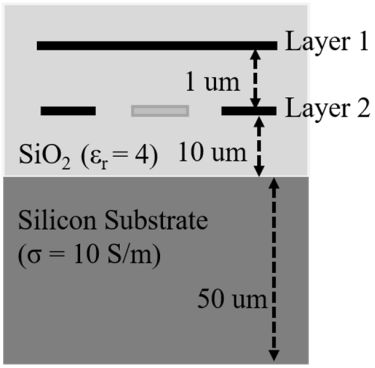

Fig. 4. Cross section view of on-chip PDN.

III. VERIFICATION

First, the impedance modeling of PDN in free space is validated. A mesh-typed P/G PDN as shown in Fig. 2 is modeled in HFSS-a commercial 3D full wave simulator. The width L_w of P/G line is 5um, the pitch L_p between power and ground line is 35um. The thickness t of P/G line is 1um. The length and the width of PDN are fixed as 985 um. The conductivity of metal line of PDN is 5.8×10^7 S/m. In the analysis of this PDN, the correction factors of α for skin effect is set as 0.54×10^8. Three ports are defined to check the input impedance of PDN, which is located at the corner, side and center of PDN respectively as shown in Fig. 2. Fig. 3 plots the input impedance curves from the code based on our method and HFSS simulation for three port positions within frequency range from 1 GHz to 100 GHz. The input impedances of PDN at three different positions from our code are all correspond to simulation results. Even at resonance frequency points, the impedance of PDN can be predicted accurately. Obviously, it means the equivalent circuit of PDN is effective and accurate.

Second, an on-chip PDN with lossy silicon substrate is modeled to validate the proposed model. Fig. 4 shows the cross section view of the on-chip PDN. The geometrical parameters

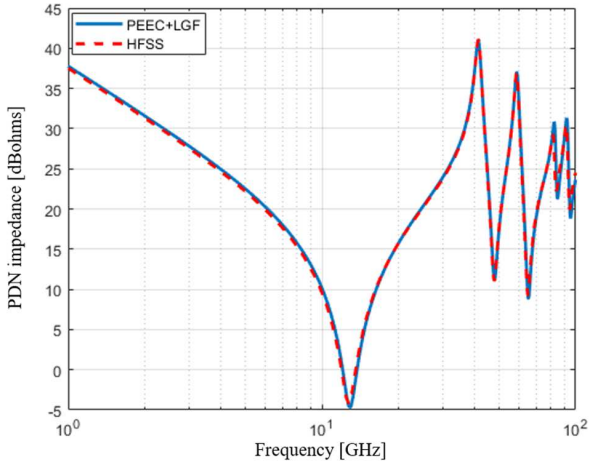

Fig. 5. On-chip PDN impedance comparison from the proposed method and HFSS for corner port.

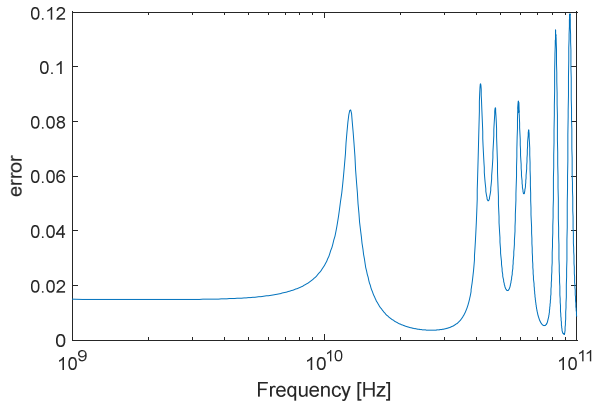

Fig. 6. Difference between HFSS simulation and the proposed method (PEEC+LGF).

and conductivity of PDN are the same as the first example. The height of silicon substrate is assumed as 50 um. The distance between PDN and silicon substrate is 10 um. The relative permittivity of silicon oxide and the conductivity of silicon substrate are shown in Fig. 4. Three ports as described in previous example have also been analyzed, and the corner port is chosen as the representative case to check the impedance. The impedance curves of this on-chip PDN from the proposed model and HFSS are presented in Fig. 5. A good match can be observed in the whole frequency range from 1 GHz to 100 GHz. The differences between simulation and the proposed method are plotted in Fig. 6. We can observe that the difference could be limited below 12% at high order resonance frequency points. The accurate of the proposed model is verified for a wideband frequency, up to 100 GHz.

The simulation was conducted in a server with 3.45 GHz CPU speed and 512 GB memory. The cost of computational resources for simulation and the proposed method are compared in table I. It shows that the proposed method is more efficiency than full wave simulation.

IV. Conclusion

An on-chip PDN impedance modeling method based on PEEC and LGF is presented in the paper. The equivalent *RLC* circuit of unit cell of PDN is proposed at first. The *RLC* parameters are extracted with the known physical parameters of PDN based on PEEC method. And then, the equivalent circuit of PDN can be modeled by connecting the equivalent circuits of all unit cells. Then LGF is applied to include the effect of lossy silicon substrate into the capacitance for the first time, which not only enhance the accuracy of the proposed impedance model but also simplify the impedance model compared with existing methods. A mesh-typed P/G PDN in free space is modeled firstly to validate the effectiveness of PEEC-based equivalent circuit of PDN. Then an on-chip PDN with silicon substrate is presented to verify the proposed method of modeling on-chip PDN impedance. The impedance of on-chip PDN from the proposed method matches with full wave simulation results at all resonance frequency points from 1 GHz to 100 GHz with tolerable errors. The efficiency of the proposed method is verified by comparison the computational resources cost in Table I. The proposed method could also be used to model the impedance of other complex 3-D package for performance analysis. In the future, some measurements will be conducted to validate the proposed method.

Table I. Comparison of Computational Resources Cost

Method	Memory Cost (GB)	CPU Time (hours)
Simulation	74	1.3
Proposed method	1.4	0.05

V. Acknolwedgements

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