Modeling an ESD Gun Discharge to a USB Cable

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2022 IEEE International Symposium on Electromagnetic Compatibility & Signal/Power Integrity (EMCSI) | 978-1-6654-0929-2/22/$31.00 ©2022 IEEE | DOI: 10.1109/EMCSI39492.2022.9889484

***Abstract*—When an electrostatic discharge (ESD) gun discharges to a USB cable, the routing and quality of the cable impacts the waveform seen at the printed circuit board (PCB) connected to the cable and the ability of an on-board transient voltage suppressor (TVS) to protect sensitive electronics. The impact of cable configurations during ESD gun contact discharge tests was investigated for multiple cable configurations. Injection to a cable pin whose shield is "floating" at the injection site can cause a double-peak in the ESD waveform at the PCB and a lower maximum stress level than when the cable shield is connected to the return plane. Poor shielding of the USB connector can further induce a pre-pulse effect, where a smaller ESD pulse arrives at the PCB before the main pulse. This pre-pulse can result in poor firing of the TVS device and thus worsen ESD stress at a sensitive IC. Circuit models were developed to anticipate and explain both of these phenomena. These models were incorporated into a system-level transient simulation including models of a PCB with a TVS and a pair of on-chip diodes. This system-level model was able to predict the quasi-static and peak voltages and currents at the on-chip diode during 1-8 kV ESD contact-discharge tests with various USB cable configurations to within less than 30%. These models were used to develop test and design guidelines to account for the impact of the quality and configuration of a USB cable during an ESD discharge.**

Keywords- Electrostatic discharge (ESD); system-efficient ESD design (SEED); System-level ESD; USB cable; transient voltage suppressor.

I. INTRODUCTION

The USB interface is one of the most commonly used high-speed interfaces within electrical devices. Because these connectors are easily accessible to users, they are highly susceptible to electrostatic discharge (ESD). Transient voltage suppression (TVS) diodes are typically added to I/O interfaces to improve the system's immunity to ESD. TVS devices can shunt most ESD current away from sensitive integrated circuits (ICs) during a transient over-voltage event. Ensuring the TVS diode turns on during an ESD event and the on-chip protection device does not take the entire charge can be challenging, however, as many on-chip ESD protection structures will turn on faster at lower voltages than the off-chip TVS [1]. The high data rate of USB interfaces, 480 Mbit/s for USB 2.0 and 5 Gbit/s for USB 3.0, requires substantial attention to signal integrity, making the design of robust ESD protection strategies even more challenging due to the low required capacitance of the device. The USB 3.0 specification requires the total parasitic capacitance be less than 1.1 pF [2], but the sub-pF capacitance ESD structure can create a large voltage overshoot during an ESD strike, which may cause hardware failure [3].

System Efficient ESD Design (SEED) is an approach to modeling the response of a system to an ESD event in order to achieve a robust ESD design [1]. Accurate modeling typically requires an understanding of the characteristics and limitations of the ESD protection devices, as well as of the parasitics associated with printed circuit board (PCB) and passive components connected to the circuit. An accurate model of the injected ESD waveform is also essential. The waveform seen by the TVS and IC, however, is easily impacted by the test setup. For example, the discharge waveforms may change depending on the ground connection and return path [4], or with the type and length of the USB cable and the capacitance between the EUT and ground plane [5].

The impact of the USB cable on an ESD gun discharge test was further investigated in this paper, and models were developed to simulate its effect. The measurement setup is given in Section II, together with an overview of the impact of cable configuration on the injected ESD stress level. Models for different cable configurations are developed in Section III and are paired with SPICE models of ESD protection devices where they are used to perform a complete SEED analysis. Conclusions are given in Section IV. Results demonstrate the importance of properly modeling the cable's impact when evaluating ESD protection strategies early in the design process.

II. EXPERIMENTAL MEASUREMENTS

A high-level diagram of the test setup is shown in Fig. 1. It consists of an ESD gun discharging to one USB cable pin. The USB cable is connected to a printed circuit board (PCB) with an off-chip TVS protecting an IC with dual-diode on-chip ESD protection. The test board was put inside a shielding enclosure, with the USB cable set outside of the enclosure, to avoid transient field coupling to the test board during the ESD discharge. The USB cable shield was connected to the shielding enclosure where it penetrates the enclosure to connect to the test board. Three cable configurations were investigated, as shown in Fig. 2. In Case 1, the USB cable was run along the enclosure surface with the shield connected to the enclosure at both ends. The USB cable was run in the same way for Case 2, but the shield was only connected where the cable penetrated the enclosure. In Case 3, the cable was drawn straight out, normal to the enclosure surface and 1.2 m above and parallel to the ground plane.

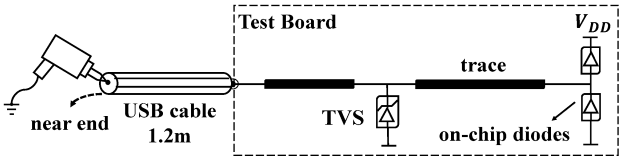


Fig. 1. Test set up for characterizing the impact of a USB cable on the response of a TVS and on-chip diodes to a contact-discharge ESD event.

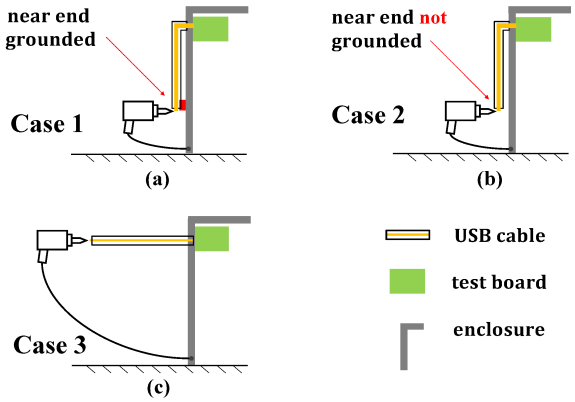


Fig. 2. Tested USB cable configurations: (a) Case 1: Cable run along enclosure and shield connected at both ends; (b) Case 2: Cable run along enclosure and shield connected only at test board; (c) Case 3: cable run straight out from enclosure, parallel to and 1.2 m above "ground" plane.

Experiments were first performed with the test board replaced with a 50 Ω load to demonstrate the impact of the cable alone on the ESD waveform. 1-8 kV ESD gun contact discharge tests were performed to the D+ pin of the USB cable. The other lines in the cable were left floating, as terminating them showed negligible impacts on the ESD events on D+. Example measurements at 4 kV are shown in Fig. 3 for all three cable configurations. The peak current is largest when the cable shield is well connected to the enclosure at the discharge point, as in Case 1, and smallest for a poor connection, as in Case 3. For Case 3, there are furthermore two peaks separated by a several nanosecond delay. This delay will be denoted as peak-delay throughout the rest of this paper. Roughly, one can think of the initial sharp peak results from capacitive coupling between the cable shield and the ESD gun body, which immediately allows a portion of the discharge pulse to propagate down the USB cable. The second pulse is caused by a "transmission line" created by the cable shield relative to the return plane and shorted at one end by the enclosure, as will be addressed in Section III. The delay of this second pulse is two times the propagation delay along the outside of the shield from the injection point to the enclosure.

The pre-pulse phenomenon is clearly shown in Fig. 3b for Case 3 (cable straight out). Even before the main pulse arrives at 0 ns, the load receives a non-zero current. The pre-pulse duration is around 2 ns, and the peak magnitude is 0.7 A (35 V at the 50 Ω load). Consequently, when tested with the typical protection topology (Fig. 1), the pre-pulse is high enough to turn on the TVS before the start of the ESD pulse, making it more difficult to predict the ESD stress seen on-chip. The impact of the peak-delay and pre-pulse on the on-chip ESD stress will be further investigated in Section III.

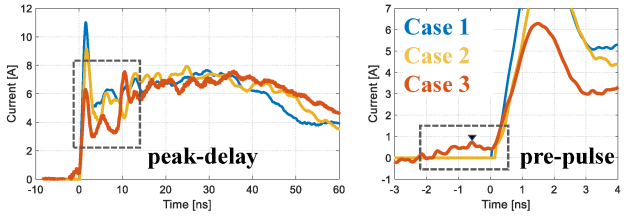


Fig. 3. Measured currents when discharging to a 50 Ω load during a 4 kV contact discharge: (a) Measured currents over entire event; (b) Currents over first several nanoseconds. Cable configurations are shown in Fig. 2.

III. Impact of USB Cable Configuration

The impact of USB cable configuration on ESD discharge to the system outlined in Fig. 1 and 2 was studied using the test board shown in Fig. 4. Fig. 4 shows a high-level circuit diagram. A detailed description is given in [6]. The board allows measurement of the voltage at the TVS and on-die diode locations, measurement of the current before and after the TVS (which can be used to predict current through the TVS), and measurement of current just before the on-chip diode. These voltages and currents were measured during contact discharge tests for all the cases shown in Fig. 2. These measurements will be used to study and develop models for the peak delay and the pre-pulse events caused by the cable configurations.

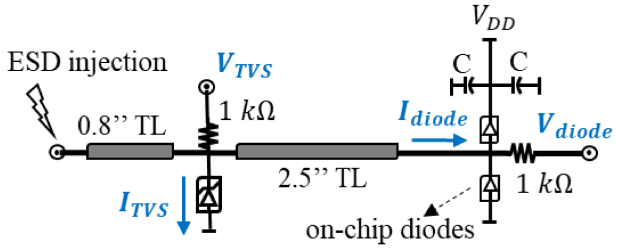


Fig. 4. Circuit diagram of the test board including off-chip protection (TVS) and on-chip protection (the dual-diode structure).

A. Impact and Modeling of the Peak-Delay

The current flowing through the TVS device, I_{TVS}, is shown in Fig. 5 for Case 1 (cable shield grounded at both ends) and Case 3 (cable straight out) for a 4 kV discharge event. Not surprisingly, the initial peak was much lower when the cable's near-end shield was not grounded, and there was a short delay after the first peak followed by a second peak, similar to the peak-delay seen when discharging to 50 Ω load. The behavior observed for Case 2 is similar to Case 3. Case 2 will be further addressed at the end of this subsection.

The current and voltage seen by the on-chip diode during ESD contact discharges from 1-8 kV is shown in Fig. 6. The figure shows the "quasi-static" on-chip diode current and voltage at roughly 10 ns (averaged from 9~11 ns). Although the TVS shunts most of the current away from the chip, the ESD stress seen on-chip is not negligible. The magnitude of the current depends on the cable configuration.

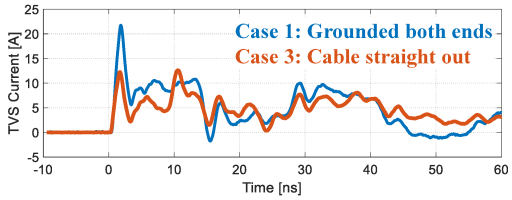
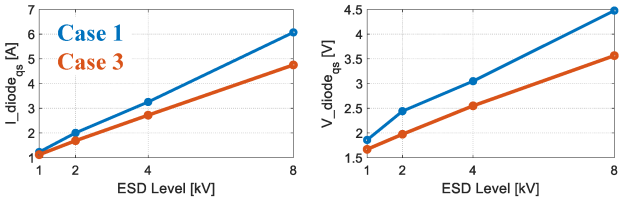


Fig. 5. Measured TVS current during a 4 kV contact discharge to the system (Fig. 1).



(a) I_{diode_10ns} (b) V_{diode_10ns}

Fig. 6. Impact of the cable configuration on the measured ESD stress at the on-chip diode: (a) on-chip diode current, I_{diode}, at ~10 ns; (b) on-chip diode voltage, V_{diode}, at ~10 ns.

A model was developed to explain the cause of the peak delay and predict the overall waveform when the cable is run straight out from the enclosure as in Case 3. Modeling this event is challenging [7], in part because the discharge waveform is highly dependent on the complex interaction between the ESD gun, the cable, and the ground plane, as well as the arrangement of the ground strap. To investigate these interactions, a simplified injection setup was built with a similar discharge path, as shown in Fig. 7. Here, cable #1 is a coaxial cable representing the USB cable. Both it and the USB cable have a 50 Ω impedance between the center conductor (e.g., D+) and the cable shield. A transmission line pulser (TLP) was used as the source to provide greater stability. The TLP injects current to the inner pin of cable #1 through coaxial cable #2. Note that only the inner conductor is connected between cable #1 and #2. One end of the shield of cable #1 connects to a 1.3x1.0 m metal plate connected to the metal ground plane, while the other end is not connected at the discharge point. The large metal plate was used to minimize the impact of cable #2 and the TLP. The metal plane is 5 mm away from the shield of cable #1, mimicking the coupling between the ESD gun and the cable shield. Several ferrites were added around cable #2 to impede any common mode current and ensure that current is injected only through the inner conductor. The TLP was grounded through a wire to represent the grounding of the power cord. The waveform that would be received by the test board inside the enclosure was measured with an oscilloscope.

The TLP in Fig. 7 is designed to roughly represent the ESD gun in Fig. 2c. The current is injected only through the inner conductor of cable #1 in both cases, and the middle metal plane is similar to the ground strap of the ESD gun. In Fig. 7, however, the return path along with the metal plate and the geometry (and associated parasitics) of the injection source (e.g., the ESD gun) are both much better controlled.

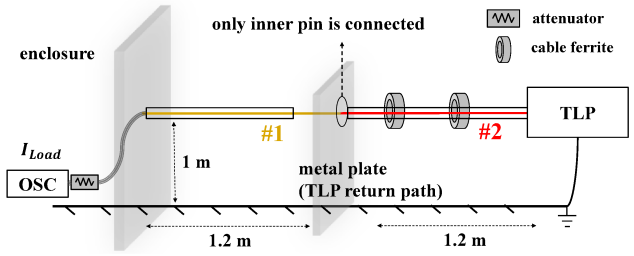


Fig. 7. Simplified setup built to study factors influencing waveform development in Case 3 (cable straight out, Fig. 2c).

A 3D full-wave simulation model was built in CST Microwave Studio based on the TLP injection setup, where it was straightforward to monitor the current at the cable's inner conductor, the cable's outer shield, and along the return path. Simulations with this model showed a strong common mode current on the outer shield of cable #1, exhibiting the peak-delay and having a magnitude similar to the current flowing through the metal plate (i.e., the TLP return path). This analysis showed that the injection would create currents along two paths: 1) a differential mode current between the inner conductor and shield of cable #1, which results in the first peak seen at the test board; and 2) a common-mode current flowing along the outer shield of cable #1, primarily as a result of the voltage generated between the shield and the return plane, which travels along the shield to the enclosure, where it is reflected and creates a second differential voltage at the input of cable #1 (and thus a second peak at the load).

A simple circuit model representing the interactions between the cable, enclosure, TLP, and return plane was developed based on this analysis, as shown in Fig. 8. The TLP was modeled as a pulsed voltage source with a 50 Ω source impedance R_S. 'TL1' and 'TL2' represent coaxial cables #1 and #2, respectively. Both have a 50 Ω characteristic impedance. Notice that only the inner conductors of 'TL1' and 'TL2' are connected. The shield of TL2 is connected to the metal plate. The shield connection of cable #1 is connected to the metal plate through an RLC circuit whose values were extracted from 3D simulation, accounting for the coupling between the shield of cable #1 and the plate. Cable 'TL1.1' represents the "transmission line" formed by the outer shield of cable #1 and the ground plane. The transmission media of this transmission line is air. The shields of TL1 and TL1.1 are connected at the injection point and the enclosure – since the inner shield and outer shield of cable #1 are shorted. In contrast, the "transmission line" formed by the outer shield of cable #2 and the ground plane was not included in the circuit model since ferrites were added around cable #2 and the overall potential to drive common mode current on this cable is low. This circuit model was verified by comparing the currents found with this model to those using the 3D model. The currents on the inner conductor of cable #1, on the inside shield of cable #1, on the inner conductor of cable #2, on the outer shield of cable #1, and on the metal plate were found to match within 10%.

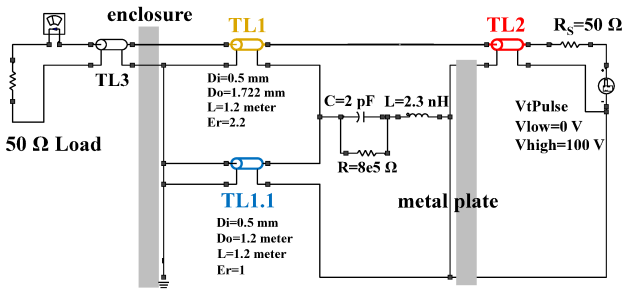


Fig. 8. Circuit model of the TLP injection setup shown in Fig. 7.

Fig. 9 shows a comparison between the current at the 50 Ω load found in measurement, found in the CST model, and found using the circuit model in Fig. 8. Similar to the current observed for Case 3 in Fig. 5, there are two peaks or transitions at the beginning of the waveform which are separated by twice the propagation delay along the outer shield of the cable. Notice that the peak-delay duration is 8 ns instead of 12 ns for a 1.2 m cable, which further confirms that the root cause of the peak-delay is the additional common mode path resulting from the ungrounded shield condition (i.e., the one-way propagation delay over 1.2 m in the air is 4 ns while the delay through a 1.2 m cable is 6 ns considering the cable dielectric).

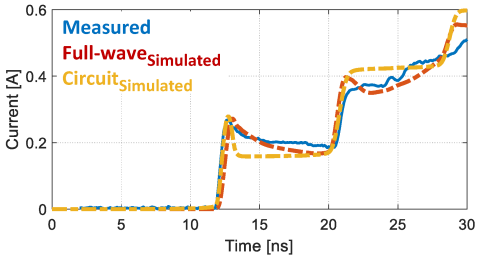
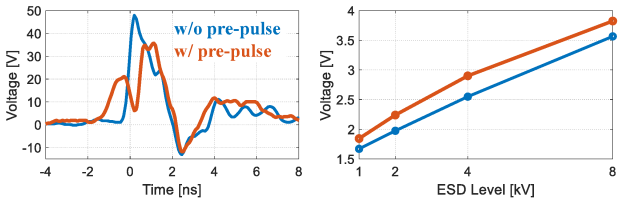


Fig. 9. Current waveform at the 50 Ω load when a 100 V TLP was injected into the cable shown in Fig. 7, as found in measurement, as found with a full-wave simulation, and as found with the circuit model in Fig. 8.

While a similar circuit model can be used to represent the conditions of Case 2, the characteristic impedance of the transmission line between the outer shield of the cable and the return plane (around 100 Ω) should be substantially smaller than the impedance seen in Case 3, as the cable is just over the enclosure in Case 2 while it is 1.2 m above the ground plane in Case 3. This lower impedance causes a larger differential voltage to initially form between the center conductor and shield of the cable and smaller voltage between the cable shield and ground plane, which results in a much larger initial peak received at the load and a smaller secondary peak, as is observed in Fig. 3.

B. *Impact and Modeling of the Pre-Pulse*

The voltage at the TVS device (V_{TVS}) and the voltage at the on-chip diode (V_{diode}) are shown in Fig. 10 when tests were performed with a USB cable configuration that caused a pre-pulse and with a configuration that did not. Both tests were performed with the same USB cable, though the cable connector shield was slightly modified as will be addressed later. When the ESD waveform received by the test board contained a pre-pulse, the voltage across the TVS contained two peaks because the TVS turns on for the pre-pulse as well as the primary pulse. While one might think this early turn-on behavior would benefit the on-chip protection, more ESD stress was observed by the on-chip diode when there was a pre-pulse than when there was not, as shown in Fig. 10b.



(a) V_{TVS} (b) V_{diode_10ns}

Fig. 10. Measured response of the TVS and on-chip diode to an ESD waveform with or without a pre-pulse: (a) TVS voltage waveform during a 4 kV injection; (b) Diode voltage at ~10 ns as a function of injection level.

Several experiments were performed to identify the root cause of the pre-pulse. It was found that the pre-pulse will not occur when ferrite common mode chokes are placed on the USB cable. It is also worth noting that the transmission delay along the inside of a 1.2 m coaxial cable is 6 ns (by TDR test), while the delay is 4 ns for the common mode path formed by the cable shield and the ground plane (Fig. 2). The delay difference is 2 ns between the inner path and the common mode path, which is exactly the length of the pre-pulse. These results suggest the pre-pulse is caused by common mode currents flowing on the outside the shield which are then coupled back to differential mode currents associated with D+ at the enclosure.

To partially validate this hypothesis, the plastic shell surrounding the connector of a USB cable that exhibited significant pre-pulse current was removed, and the USB connector's shield connection was exposed, as shown in Fig. 11. The connector shield was only connected to the cable shield by a thin wire, which forms an effective path for mutual inductive coupling between the inner (differential mode) and outer (common mode) shield currents at the enclosure. The common-mode current on the outside of the shield can easily be coupled to the signal lines with this poor shield connection.

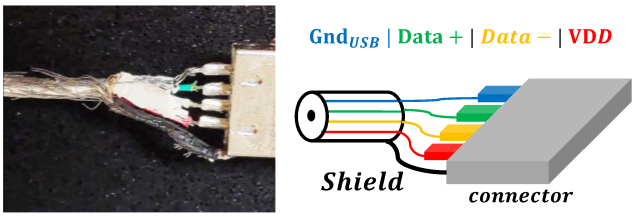


Fig. 11. The poor shield connection between the cable shield and the USB connector: photo and sketch.

C. *Circuit Model for Case 3 Cable Configuration*

A circuit model describing the peak-delay and pre-pulse behaviors observed in Fig. 3 can be developed as shown in Fig. 12 based on the observations in the previous sub-sections. The current source 'ItDataset' (the measured current on a 50 Ω load in a contact discharge event without cable), together with a 330 Ω resistor, represents the ESD gun. A measured current source was used to provide better accuracy than a typical ESD

gun circuit model [4]. The measurement-based source's accuracy was verified with simulations and measurements of Case 1, where both ends of the cable shield are grounded. The transmission line 'TL1' is a coaxial cable of 50 Ω characteristic impedance representing the differential mode currents inside the USB cable, while 'TL2' is a 377 Ω transmission line representing the common mode path formed by the cable shield and the ground plane. The two mutual coupled inductors 'L1' and 'L2' represent the coupling between the inner current path and the common mode path.

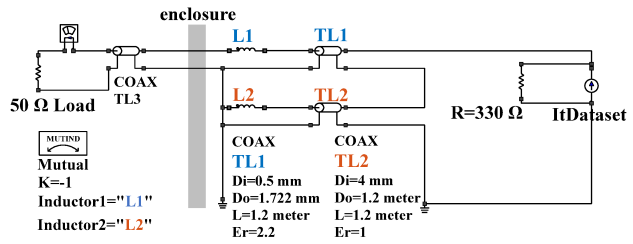
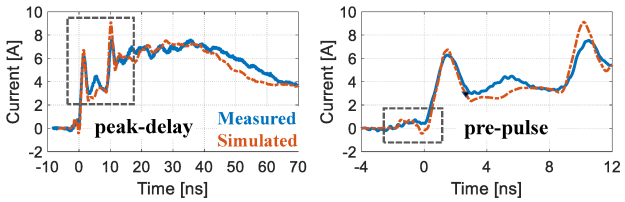


Fig. 12. Circuit model for Case 3 (cable straight out) during an ESD gun contact discharge event as illustrated in Fig. 2.

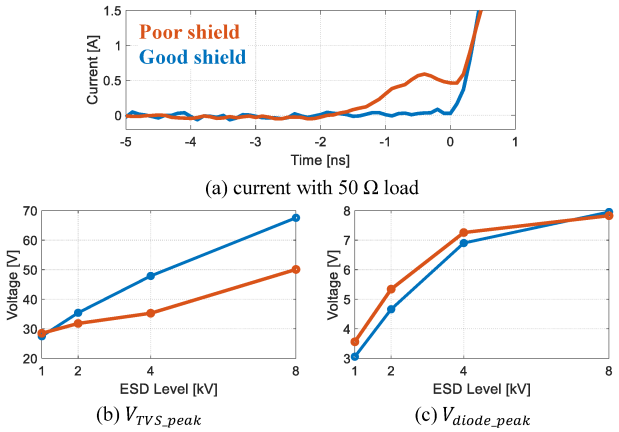
Simulation results from this circuit are shown in Fig. 13. Both the peak-delay effect (modeled by the additional common mode path) and pre-pulse effect (modeled by the inductive coupling) are reasonably well captured. The peak-delay duration is linearly proportional to the cable length. Perfectly matching the peak magnitude is difficult and requires fine-tuning of the inner conductor diameter of the common mode path 'TL2'. The discrepancy is acceptable, considering that the transmission line TL2 only roughly approximates the common-mode path along the shield as more than TEM modes are present between the cable shield and the ground plane. The values of L1 and L2 and the coupling coefficient between them depend on the cable configuration. Their inductance values were set here to 6 nH and the coupling coefficient to -1 for convenience, but could later be extracted for different USB cables.



(a) (b)

Fig. 13. Measured and simulated current at the 50 Ω load for a 4 kV ESD contact discharge in the Case 3 cable configuration (cable straight out): (a) Measured currents over entire event; (b) Currents over first several nanoseconds.

The pre-pulse can be avoided by shielding the USB connector. Fig. 14 shows the impact of using a poorly shielded and well shielded USB connector on the ESD stress seen at the test load. These results were found through measurement when the cable was in the Case 3 configuration (straight out). Fig. 14a shows the transient current for two tested cable configurations when injecting into a 50-ohm load. Fig. 14b and 14c show the peak voltage across a TVS device and on-chip diode when they are used as in Fig. 1, as a function of the applied ESD gun voltage. The TVS voltage is lower if the USB connector is poorly shielded since the pre-pulse will induce two peaks at V_{TVS} and reduce the voltage overshoot. An exception is at 1 kV because the pre-pulse is not strong enough to turn on the TVS. Poor shielding of the USB connector also causes worse ESD stress at the on-chip protection over a wide range of injection voltages, which also be addressed in Fig. 10b.



(a) current with 50 Ω load

(b) V_{TVS_peak} (c) V_{diode_peak}

Fig. 14. Impact of the quality of the USB connector shield on the response to an ESD gun contact discharge in the Case 3 cable configuration (cable straight out): (a) Measured current at a 50 Ω load with a 4 kV injection; (b) Peak measured voltage across a TVS and (c) across a diode as a function of ESD gun voltage when TVS and diode are arranged as in Fig. 1.

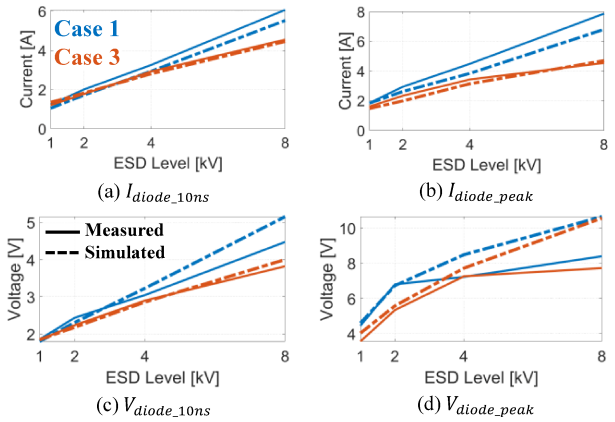
To determine the practical range of the inductive coupling associated with the USB connector shields, experiments were performed on ten commercial USB cables, including USB to micro-USB, USB to USB-C, USB to lightning, and USB-C to lightning cables. Tests were performed with a 50 Ω load under an ESD gun contact discharge in the Case 3 configuration (cable straight out). The inductance values were found by adjusting the inductance value in the simulation model (Fig. 12). Values ranged from 0-8 nH. The larger the poorly shielded region at the USB connector, the larger the coupling inductance, which results in a worse pre-pulse issue.

D. System-Level Simulation

The circuit model predicting the impact of the cable configurations can be merged with models of the ESD protection devices to form a SEED simulation model of the overall system. A model for the system was created using the circuit in Fig. 12, but replacing the 50 Ω load with circuit models of the board, TVS, and on-chip diodes. Models for these components and the test board are described in [6]. The circuit model in Fig. 12 was further modified to represent the cable configurations shown in Case 1 (cable shield grounded on both ends) and Case 2 (cable along enclosure and connected only at one end). For Case 1, the common-mode path 'TL2' was removed since the common mode path does not exist in this configuration. For Case 2, the common-mode TL2 transmission line impedance was set to 100 Ω since the cable is very close to the ground. System-level tests were done with good shielding at the USB connector to avoid the impact of pre-pulse, since it was difficult to accurately capture the pre-pulse voltage overshoot at the on-chip diode due to limitations in the oscilloscope's dynamic range and the turn-on behavior of TVS.

The simulated and measured current and voltages seen by the on-chip diode are shown in Fig. 15 for the Case 1 and Case 3

configurations. The simulated on-chip diode current and voltage at 10 ns (averaged from 9~11 ns) are captured within 12% of the measurement for 1-8 kV injections, while the peak current and peak voltage are captured within 30%. The peak values are particularly hard to capture because small errors in the TVS or diode's turn-on time could significantly change the interaction between TVS and on-chip diode. Similar simulation performance was achieved when a 1 Ω resistor and a 10 nH inductor were placed between the TVS and diode, as well as for the Case 2 cable configuration.



(a) I_{diode_10ns} (b) I_{diode_peak}

(c) V_{diode_10ns} (d) V_{diode_peak}

Fig. 15. Simulated and measured currents for the on-chip diode in Fig. 1 for 1-8 kV contact ESD gun discharge to a USB in cable configurations Case 1 (both ends grounded) and Case 3 (cable straight out): (a) On-chip diode current at 10 ns; (b) On-chip diode peak current; (c) On-chip diode voltage at 10ns; (d) On-chip diode peak voltage.

IV. Discussion and Conclusions

The characteristics of the ESD waveform at the PCB change substantially depending on the configuration of the USB cable during an ESD gun contact discharge event. When the cable's shield is not grounded at the discharge point, an additional common mode current path will be formed between the cable shield and the ground plane, leading to a peak-delay phenomenon, where two smaller peaks are observed at the PCB (separated by twice of the speed-of-light propagation delay along the outer cable shield) rather than one prominent peak. The farther the cable shield is from the test ground plane, the lower the ESD stress. Moreover, if the USB connector is not well shielded at the enclosure, the common-mode current on the outside of the shield can couple energy to the signal lines and cause a pre-pulse in the observed waveform, before the main ESD pulse arrives. This pre-pulse can cause higher ESD stress levels at the on-chip ESD protection. While the level of added stress was not substantial (e.g., the on-chip diode dissipated 3-14% more energy with a poorly shielded cable than with a well-shielded cable as shown in Fig. 14), it is still a phenomenon worth considering during ESD testing. Circuit models were developed which explain and predict both the peak-delay and pre-pulse phenomena. When combined with models of the TVS and on-chip ESD protection diodes to form a system-level SEED simulation model, the model was able to predict quasi-static voltages and currents at the on-chip diode within 12% and the peak voltages and currents within 30%. This level of performance is more than adequate to allow evaluation of ESD protection designs early in the design process.

Results from these models suggest several guidelines for testing and evaluating the ESD response of a system with a USB cable. If the shield is unconnected where the ESD discharge is made, a peak-delay phenomenon will show up in the waveform at the board and the initial peak will be reduced. If a USB adapter is needed, the transition from the USB cable to the adapter should use well-connected shielding to avoid the pre-pulse phenomena. Testing with a poorly-shielded cable connector may be warranted when evaluating the quality of the TVS protection, however, as the pre-pulse can modify the behavior of the TVS and may modestly increase the stress to the on-chip ESD protection. Of course, USB cables should be designed to effectively shield the transition between the USB cable and the connector to avoid coupling of common-mode noise on the outer cable shield.

V. Acknowledgment

This work was supported in part by the National Science Foundation (NSF) under Grant IIP-1916535.

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