A Low-Power Asynchronous Level Crossing ADC designed in 180nm CMOS process for Electrophysiological Signal Recording Applications

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***Abstract*—Presented in this paper is the design of a level-crossing ADC for biomedical potentials. This architecture takes advantage of the time sparse nature of neural signal recording applications by only sampling when the signal is moving. A 10-bit architecture with a novel threshold control scheme was chosen to help capture both the higher amplitude local field potentials and lower amplitude action potentials found in these systems. The ADC operates on a power of 13.5 μW from a 1.8 V supply and achieves a root-mean-square error (RMSE) of 0.65 mV. The design is implemented and simulated in a 180 nm CMOS process using the Cadence Virtuoso Custom IC design tool.**

***Index Terms*—analog-to-digital converter (ADC), biomedical, ADC, asynchronous, neural recording, action potentials, local field potential**

I. Introduction

Portable and implantable medical devices are great assets that today's medical personnel have at their disposal. These allow for a level of information available to doctors that were not possible for most of human history. The designs for these systems, however, are required to be extremely power efficient and have a low silicon footprint [1]. One of the areas that have developed over the recent decades is neurological signal acquisition. These signals can be classified into local field potential (LFP) and action potentials (APs) [2].

APs are the result of activity for a single neuron. LFPs, on the other hand, are generated by the superimposition of electrical activity of neurons in the region. The signal characteristics of LFPs are typically in the frequency range of 0.1-250 Hz with a peak amplitude of several mV. For APs, the peak amplitude can be about a few μV and with a frequency range of 0.25-5 kHz [3].

The analog-to-digital converter (ADC) block used in these recording systems is instrumental in accurately recreating the LFPs and APs in the signal. The typical choice for this process is an SAR ADC with a resolution ranging from 8-10 bits [4]. The SAR architecture is popular because it can meet the demands of biopotential sampling, including low power, low sampling rate, and the resolution criteria. However, due to the time sparse nature of neural signals, level-crossing ADCs have gained recent attention as an alternative method [5]. Since this architecture only samples when the signal is active, it has been shown to save power for the biomedical signals [6].

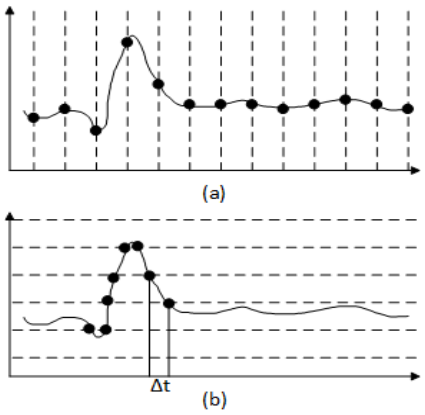

Fig. 1. (a) Uniform sampling. (b) Asynchronous or level-crossing sampling

Many of the level-crossing ADCs reported in recent years for biomedical applications have been aimed at ECG [7]. The characteristics of these signals allow the ADCs to operate at 8-bits of resolution. However, since the aim of this paper is to capture both the high amplitude and low amplitude signals found in neural signal recording, a 10-bit resolution is necessary. This work presents a digital logic design fast enough to handle all 10 of the required bits.

This paper is organized as follows. The individual blocks found in the ADC architecture are discussed first in Section II. This includes the comparator, digital-to-analog converter (DAC), the timing circuit, and lastly the digital logic. Simulations results are presented in Section III, followed by the conclusion in Section IV.

II. ADC Architecture

The principle of level-crossing ADCs in literature can be traced back to papers as early as 1966 [8]. This scheme works similar to a flash ADC, with the difference of only using two comparators in its design [9]. Fig. 1 helps to explain the difference between a typical synchronous ADC design and

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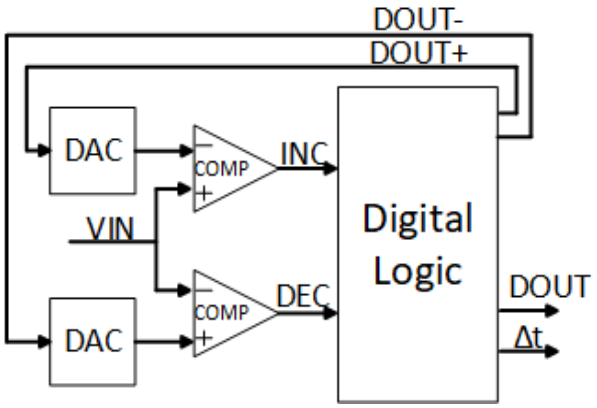

Fig. 2. Architecture of the asynchronous ADC

the asynchronous design. Fig. 1 (a) shows how a uniform sampling scheme works in ADCs. As can be seen from the figure, no matter how the signal is behaving, the synchronous system takes a data point, as represented by the black circles on the signal, at every dotted line. The dotted line represents the sampling frequency for our example ADC. The level-crossing example shown in Fig. 1 (b) demonstrates how this scheme only takes data points when certain voltage thresholds are crossed. Because of the nature of this method, the time between samples, Δt is also required for reconstruction.

The block-level diagram for a typical asynchronous ADC is shown in Fig. 2. There are three main components for this architecture. These are the DAC, comparators, and the digital logic. The input neural signal, *VIN*, is fed to the two comparators that trigger whenever *VIN* crosses one of the voltage thresholds. The outputs of these comparators are labeled as *INC* and *DEC* and represent when the input signal hits the upper or lower threshold voltages, respectively. The digital logic block then takes these two inputs and outputs four lines of information.

The *DOUT* and Δt lines are the outputs of the system. *DOUT* is the 10-bit representation of the input voltage, and Δt is the time in between samples. The other two signals generated by the digital logic, *DOUT*+ and *DOUT*-, are also 10-bit numbers used by the DACs to set the values for the upper and lower voltage thresholds for the comparators.

A. Comparator

Due to the asynchronous nature of the level-crossing method, a continuous-time (CT) comparator is used in most of the prior works. The CT comparator designed for the proposed ADC is a Class-A amplifier that reduces the rise and fall times through a pair of inverters at the output [10]. The bias current chosen for this design was 5 μA.

B. DAC

As mentioned earlier, the DAC is responsible for setting up the threshold levels for the comparators based on the *DOUT*+ and *DOUT*- 10-bit inputs. The accuracy of the two DACs is a major component of how the overall system performs. This assertion can be thought of intuitively by remembering how the overall architecture works. For conventional level-crossing schemes, the error produced in the system is one in the value of Δt and not the voltage level. So, having an accurate output for the DAC to get as close to the ideal case as possible is important to accomplish.

The topology chosen for this design is the popular charge-scaling DAC. While not ubiquitous in the literature for this application, it can be found in various forms in prior works [11]. The architecture has a binary-weighted array of capacitors with a total value of 2^NC. A digital code $D_0D_1...D_{N-1}$ is sent to switches connected to the bottom plate of these capacitors to connect them to either the supply voltage, 1.8 V in this design, or ground. This causes V_{out} to be a function of voltage division between the capacitors.

C. Timing circuit

The timing circuit is responsible for determining the time in between samples, Δt. For the purpose of the simulations, a combination of a ring oscillator and a counter circuit was used for this block. The traditional ring oscillator is comprised of a closed-loop of identical inverter stages that meet the Barkhausen criteria to oscillate [12]. The topology used for this design is known as a current starved ring oscillator. As the name suggests, this architecture limits the amount of current available to the inverter stages through a control voltage that controls the frequency of operation [12]. The number of stages for this design was chosen to be 21 to reach the target frequency of 1 MHz. This would result in a timer resolution of 1 μs that was used in the simulations.

The counter circuit was implemented through the use of VerilogA code. The code acts as an up counter to track the number of cycles between the samples. The output of the ring oscillator is fed into an input for the code block that causes the counter to tick up by one on the rising edge of each clock cycle. There is also a clear input that resets the counter after a sample has been generated in the digital logic block. The output was chosen to be 10 bits to help ensure the counter never overflows.

D. Digital Logic

The block-level diagram for the digital logic is shown in Fig. 3. The blocks found in this part of the system are the *Output Logic*, *Control Bits*, and *Track bits*. As mentioned earlier, the digital logic takes the *INC* and *DEC* lines as inputs.

The *Output Logic* block is responsible for setting the values for *DOUT*, *DOUT*+, and *DOUT*-. The operation of this circuit is as follows: Whenever *INC* or *DEC* goes high, a copy of the current *DOUT* value is saved in 10 different D flip flops as a temporary signal. This temporary signal is fed into a 10-bit adder/subtractor circuit. Through a combination of *B0* and *K*, as shown in Fig. 3, the new value of *DOUT* is generated. *B0* is the least significant bit (LSB) for the number being added to the temporary signal of *DOUT*, while the value of *K* controls if the circuit is adding or subtracting. The value for *DOUT* is then sent to another pair of adder/subtractor circuits that use

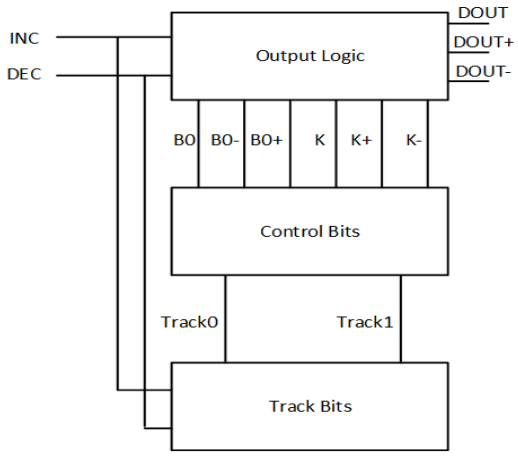

Fig. 3. Digital logic block diagram

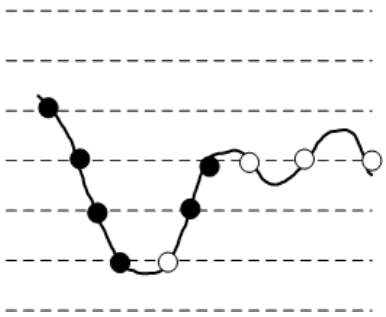

Fig. 4. Level crossings in the ADC. Consecutive level crossing (CLC) shown with black circles. Repeated level crossings (RLC) shown with white circles.

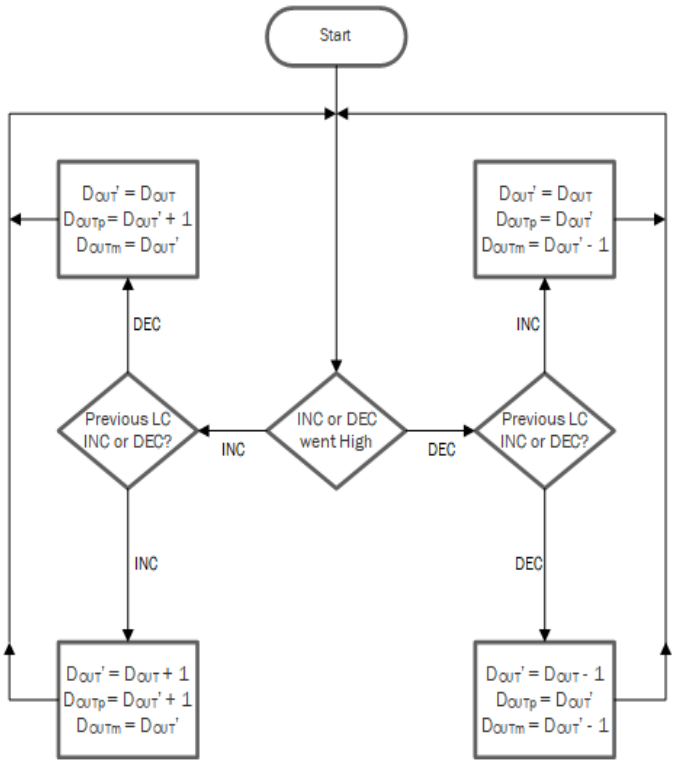

Fig. 5. Digital logic flowchart

B0+, *B0-*, *K+*, and *K-* in a similar fashion to set the *DOUT+* and *DOUT-* values.

The inputs to the *Output Logic* block are controlled through a combination of the *Control Bits* block and the *Track Bits* block. To better explain the logic behind these two blocks we will refer to terminology proposed by Li *et al*. [9]. For this architecture there are two types of level crossings. These will be coined as consecutive level crossings (CLC) and repeated level crossings (RLC). Fig. 4 shows these concepts. RLC can be seen as when the signal comes back on itself and crosses over the previous threshold that was triggered. The CLC is when the signal crosses the threshold that it did not previously cross. Keeping track of this is important as it informs the system as to how *DOUT* is moving. The *Track Bits* block is responsible for keeping track of this movement. *Track0*, as shown in Fig. 3, represents the most recent level crossing, while *Track1* is used for the level crossing before that. In this way, the logic can determine if the level crossing is an RLC or CLC.

Now that the system can keep track of the RLC and CLC instances, the *Control Bits* block is responsible for using this information and setting the inputs to the *Output Logic*. The flowchart shown in Fig. 5 was used to create the logic. This flowchart shows all 4 possible combinations of level crossings. As an example, the case of the signal triggering *DEC* and then *INC* will be used.

In Fig. 5 *Doutp* stands for *DOUT+* and *Doutm* represents *DOUT-*. The example of going from *DEC* to *INC* leads to the upper left portion of the flowchart. This is an example of an RLC. The value of *DOUT* will stay the same as the signal has come back on itself and crossed the same threshold twice. Since the signal's last movement was increasing, the *DOUT+* line is set to 1 above *DOUT* while *DOUT-* is equal to *DOUT*. This keeps the input signal between the thresholds until it has moved enough to trigger again. Similar logic can be found at the end of every branch shown in Fig. 5.

III. Simulated Results

Two input sinusoidal signals were used to validate the design. One signal was chosen to have an amplitude of 400 mV with a frequency of 300 Hz. This was chosen to mimic the LFP portion of neurological signals discussed earlier in the paper. To imitate APs, an input signal of 6 mV with a frequency of 5 kHz was used. These numbers represent typical levels found after the analog front end (AFE) in neural signal recording apparatuses.

Fig. 6 shows the result of the 400 mV simulation. This figure shows both the full cycle as well as the zoomed in view of the peak. For this figure, as well as Fig. 7, the blue line is the input signal and the red *X*s are the sample points taken by the ADC. The level-crossing architecture of the ADC can be demonstrated with these result. In the highest slope portions of the signal there are a relatively large number of samples that are being taken, when compared to the peaks. This shows

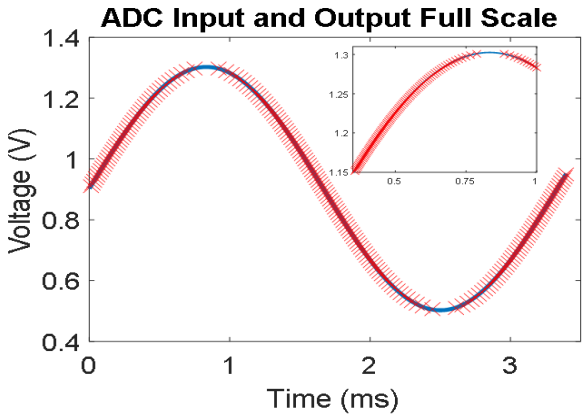

Fig. 6. ADC output for 400 mV input signal

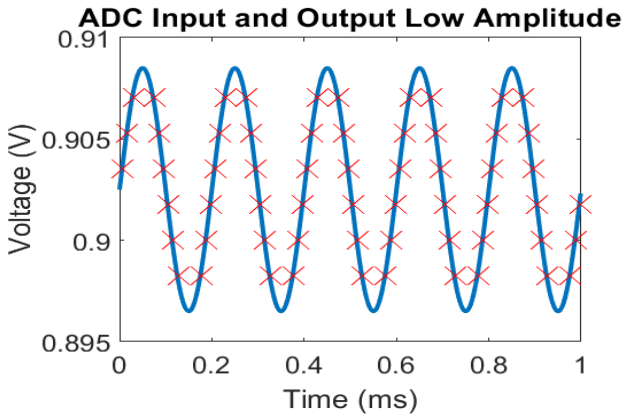

Fig. 7. ADC output for 6 mV input signal

qualitatively that as the signal changes more slowly the ADC is lowering the number of samples being taken. This even leads to a period during the peaks where no samples are being taken at all. From this a root-mean-square error (RMSE) value of 0.65 mV was calculated. Fig. 7 shows the result of the 6 mV simulation. This result illustrates how the ADC is also able to capture the lower amplitude APs.

Table I presents a comparison of this design with other works found in the literature. The effective number of bits (ENOB) reported for this work was calculated using Eqn. 1 and Eqn. 2 [15]. The *OSR* in the SNR equation represents the clock oversampling ratio and is found by taking the ratio of the timer frequency to the input signal frequency. This leads to a very competitive ENOB value of 10.05. This is achieved through a combination of the 10-bit design and the timer resolution having the capability of being set to 0.5 μs in the system, which is also very competitive when compared to prior works. It was chosen to calculate the power consumed by the system without the ring oscillator contribution, as other papers had their timing circuits located off chip and would have lead to a misleading conclulsion.

$$SNR = 20\,log\,OSR - 14.2\,dB \tag{1}$$

TABLE I
PERFORMANCE SUMMARY

Parameter	[13]	[14]	[7]	**This Work***
Technology (μm)	0.18	0.18	0.35	0.18
Supply Voltage (V)	0.7	0.8	1.8-2.4	1.8
Resolution (bits)	4-8	8	4-8	10
Adaptive Resolution	Yes	No	No	No
Timer Resolution (μs)	1	-	1.0-62.5	0.5
Bandwidth (kHz)	1	3.3	1	1.2
ENOB	8.4	-	6-8	10.05[b]
Power Consumption (μW)	25[a]	0.062-106	0.6-2.0	13.5[c]
FOM (pJ/conv.)	37	0.133-0.192	3.9	5.3[b]

* Simulated results
[a] Without off-chip logic
[b] Calculated with derived SNR value
[c] Without ring oscillator power

$$ENOB = \frac{SNR - 1.76\,dB}{6.02\,dB} \tag{2}$$

$$FOM = \frac{Power}{2^{ENOB} * 2\,BW} \tag{3}$$

The figure of merit (FOM) for asynchronous ADCs is defined in Eqn. 3. In this equation, *BW* represents the bandwidth of the system, as reported in Table I. The FOM achieved for this design is 5.3 pJ/conv. These metrics show that this design was able to achieve similar performance in power usage and accuracy while having a greater number of bits to capture more information for neural signal recording applications.

IV. CONCLUSION

A low-power 10-bit asynchronous level-crossing ADC using a novel threshold control scheme is designed in 180 nm CMOS process for electrophysiological signal recording application using Cadence Virtuoso Custom IC design tool. The target application of portable and implantable biomedical system, specifically neurological signal acquisition, was discussed and designed around. A 10-bit resolution was chosen to capture both the LFPs and APs found in these systems. The presented design led to good accuracy with an RMSE value of 0.65 mV, a low power consumption of only 13.5 μW, and a competitive ENOB figure of 10.05. The future work on this project will be to fabricate the chip to experimentally validate the performance reported.

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