MoS_2 Synapses with Ultra-low Variability and Their Implementation in Boolean Logic

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ABSTRACT: Brain-inspired computing enabled by memristors has gained prominence over the years due to their nano-scale footprint and reduced complexity for implementing synapses and neurons. The demonstration of complex neuromorphic circuits using conventional materials systems has been limited by high cycle-to-cycle (C-C) and device-to-device (D-D) variability.

Two-dimensional (2D) materials have been used to realize transparent, flexible, ultra-thin memristive synapses for neuromorphic computing, but with limited knowledge on the statistical variation of devices. In this work, we demonstrate ultra-low variability synapses using chemical vapor deposited 2D MoS_2 as the switching medium with Ti/Au electrodes. These devices, fabricated using a transfer-free process, exhibit ultra-low variability in SET voltage, RESET power distribution and in synaptic weight update characteristics. This ultra-low variability is enabled by the interface rendered by Ti/Au top contact on the Si-rich MoS_2 layers of mixed orientation, corroborated by transmission electron microscopy (TEM), electron energy loss spectroscopy (EELS) and x-ray photoelectron spectroscopy (XPS). TEM images further confirm the stability of the device stack even after subjecting the device to 100 SET-RESET cycles. Additionally, we implement logic gates by monolithic integration of MoS_2 synapses with MoS_2 leaky integrate-and-fire (LIF) neurons to show the viability of these devices for non-von Neumann computing.

KEYWORDS: MoS_2, low C-C variability, low D-D variability, interface mediated, non-volatile, memristor and threshold logic gate

INTRODUCTION

Neuromorphic computing, inspired by the human brain's cognitive processing capability has found its applications in artificial neural networks (ANNs) and machine learning. The neuro-inspired algorithms involve large scale vector matrix operations which require parallelism and in-memory computing at the device and architecture levels for improved efficiency. Memristors fabricated in cross-bar configuration drastically decrease the complexity of vector matrix multiplication, thus increasing the computational speed, thereby enabling the realization of high-density circuits.[1] To this end, memristors are preferred over conventional complementary metal oxide semiconductor (CMOS) circuitry for the implementation of synapses, the basic functional

block of neuro-inspired architectures.[2-3] However, a major obstacle hindering the large scale implementation of memristors for the state-of-the-art memory, logic and computing applications is the presence of high C-C variability and D-D variability due to the intrinsic stochasticity of their switching process.[4] This stochasticity causes variations in the conductance for a single switching cycle between different devices (D-D variability) and within an individual device (C-C variability).[5] Various techniques and materials platforms have been explored to obtain low C-C and D-D variability.[6-11] Some demonstrations utilize a transistor connected serially to the memristor to regulate the switching properties.[12-14] Another interesting technique involves the implementation of ratioed memristor, where two memristors represent a single memristor cell and the ratio of the two resistances is used to encode information.[15] However, these techniques limit scalability and increase design complexity. Therefore, it is necessary to design synapses that exhibit low C-C and D-D variability without the complex peripheral circuitry. Electrode engineering can be used as an efficient method to obtain uniform synapses.[10] Yeon *et al.* employed a metallurgical technique where an Ag-Cu alloyed electrode replaces Ag as the top electrode in amorphous Si (a-Si) based electro-chemical metallization (ECM) memristor to obtain high uniformity in DC cycling and analog weight update characteristics.[10] A low C-C and D-D variability in synapses allows reliable circuit level implementations, such as in perceptrons for pattern recognition and in implementations for in-memory computing. One of the first demonstrations of a single layer perceptron employed Pt/TiO_{2-x}/Ti crossbars. [16] Due to the high D-D variability in this implementation, off-chip wires were required to disconnect individual memristors from the crossbars during the forming process, which is cumbersome. Researchers have used stack engineering to circumvent D-D variability. For instance, Al_2O_3/TiO_{2-x} was used as the switching medium for crossbars in a neural network used to perform classification of 3 ×

3-pixel gray-scale image.[17] It is worth noting that the fundamental description of the NNs can be a mathematical model of a functional unit called neuron which operates in all or no spiking fashion when a threshold is reached. This model and its hardware implementation is called as Threshold Logic Gate (TLG).[18] The neuron computes the weighted sum of its inputs (synaptic weights) and produces the spikes when the threshold is reached.[18] Therefore, the TLG can be utilized for implementing either NN applications by realization of single layer perceptron or in-memory computing applications *via* Boolean logic implementations. Realizing in-memory computing architecture with CMOS technology is wrought with unsatisfactory performance, low productivity and high cost when compared with von Neumann computing devices.[19] In contrast, memristive devices allow low-power and low-cost Boolean logic implementations useful for in-memory computing, where the device characteristics are consistent with the requirements of edge computing devices. [19-20] Additionally, the TLGs built with memristors can be utilized for reconfigurable processing architectures. Memristor-based circuits can replace bulky CMOS-based architectures and through precise combination of signals, the basic circuitry can be easily modified to implement various logic gates that is convenient to solve individual computational problems.[21]

Recently, two-dimensional (2D) materials have been considered for electronic and opto-electronic applications due to their low power consumption, flexibility, transparency and thermal stability.[22-23] Semiconducting 2D materials have been used successfully as the active layer in several demonstrations of synaptic devices. Vertical memristive devices have been realized with exfoliated MoS_2 nanosheets and MoS_2-GO composite structures [24-27], h-BN [28], WS_2,[29-30] and WSe_2.[31] However, for a potential neuromorphic hardware, it is essential to realize synapses on a wafer scale. In that direction, non-volatile resistive switching is observed in chemical vapor deposition (CVD)-grown 2D materials like $MoSe_2$, WS_2, WSe_2, [32] h-BN[9, 33-34] and MoS_2.[32, 35-36]

Although a huge body of literature exists on the demonstration of memristive/synaptic behavior using 2D materials, studies on C-C and D-D variability of 2D materials-based devices are scarce. Chen *et al.* reported low C-C and D-D variability in SET and RESET voltages with CVD h-BN as the switching medium.[9] This report on h-BN based synapses exposes the inherent nature of 2D materials to produce devices with high uniformity, which is necessary for realizing high density electronic circuits. However, for unraveling the true potential of a materials system, it is imperative to not be limited by the demonstration of a single device. Also, it is essential for devices to demonstrate low D-D and C-C variability for reliable circuit implementations. Reports on circuit implementations with 2D materials-based synapses have been limited to the modelling of multi-layer perceptrons wherein the potential of the emerging technology is suggested through simulations.[9]

In this work, we demonstrate MoS_2 based synapses with Ti/Au as the bottom and top electrodes. These devices exhibit ultra-low C-C and D-D variability in SET voltage and RESET power distributions. The synapses exhibit low C-C and D-D variability in weight update characteristics as well, comparable with the industry compatible a-Si based synapses.[10] We demonstrate the existence of 26 distinct conductance states in these devices, with a retention of at least 300 s for each of these states. These devices exhibit excellent endurance by maintaining a consistent ON/OFF ratio for 1000 DC SET-RESET cycles. These exemplary characteristics observed in MoS_2 based devices can be attributed to the underlying switching mechanism which is mediated by the interface between MoS_2 and Ti, corroborated by their area-dependent resistance scaling. Temperature dependent I-V measurements confirm space charge limited current (SCLC) to be the dominant transport mechanism. Further, the TEM images show no degradation in the stressed device indicating the stability of the stack. We integrate these MoS_2 synapses with MoS_2

LIF neurons[37] to realize AND, OR and NOT logic gates. This demonstration of Boolean logic using 2D materials-based synapses and neurons shows the feasibility of 2D materials for large-scale circuit implementations.

RESULTS AND DISCUSSION

The schematic of the MoS_2 synapse is shown in **Figure 1a**. The devices are fabricated by UV lithography on MoS_2 films grown by chemical vapor deposition (CVD), using a transfer-free process, and the fabrication details are provided in the methods section. The optical microscope image of a typical Ti/Au/MoS_2/Ti/Au (bottom to top) device is shown in **Figure 1b**. The active area of the fabricated devices is systematically varied from 2×2 μm^2 to 50×50 μm^2. Cross-sectional TEM is utilized to assess the device stack as shown in **Figure 1c**. The TEM image shows the layered growth of MoS_2 of thickness ~10 nm. Further, the chemical composition of the device stack is analyzed by the elemental energy dispersive X-ray spectroscopy (EDS). The EDS maps clearly reveal the presence of MoS_2, bottom electrode (Au) and top electrode (Ti/Au) as shown in **Figure 1d**.

The devices are probed in vacuum at a base pressure of 10^{-4} mBar for electrical characterization. **Figure 2a** shows the DC I-V characteristics, demonstrating the non-volatile switching of the MoS_2 devices with Ti/Au electrodes. Here the I-V characterization is executed on device of area 5×5 μm^2. To perform this experiment, we apply the bias voltage to the bottom electrode while keeping the top electrode at 0 V during these measurements. These devices do not exhibit abrupt transition from the high resistance state (HRS) to low resistance state (LRS), unlike filamentary memristive devices.[28, 33-34, 38-44] Instead, the devices exhibit a smooth transition from HRS to LRS, hinting at the role played by the interface in the non-volatile switching behavior.

Therefore, we apply a voltage compliance (VC) of 2.5 V for SET and -3 V for RESET, in contrast with the current compliance (CC) applied in filamentary memristive devices during SET, to test the endurance of the device through 1000 DC cycles. To evaluate the low variability evident through the 1000 cycles, the OFF and ON states are extracted at V_{read}= 0.25 V, as shown in the supplementary information (**Figure S1)**. The MoS_2 device exhibits constant ON and OFF states throughout the 1000 DC cycles indicating their ultra-low C-C variability and endurance. It should be noted that the endurance of the device is characterized under a harsh DC cycling of 1000 times, as opposed to a milder pulsed cycling. To establish the necessity of MoS_2 in resistive switching, we fabricate a test structure consisting of Ti/Au top electrode deposited on a Ti/Au bottom electrode. **Figure S2** shows the shorted characteristics of the test structure as expected from a metal-on-metal structure. It should be noted that the top Ti/Au electrodes are patterned and deposited after subjecting the bottom Ti/Au electrodes to the exact processing steps that were used for obtaining MoS_2 films for this study. To evaluate the variation in the SET voltage and RESET power, our MoS_2 device is cycled for 100 times by enforcing a CC keeping the maximum current density at 40 A/cm^2. The voltage at which the current through the device reaches this maximum current density is considered to be the SET voltage. The RESET power is calculated using the formula $P = V \times I$, where I is the maximum RESET current, and V is the maximum RESET voltage applied. Devices of area 2×2 μm^2 are probed for comparing the device performance with industry compatible a-Si/Ag-Cu devices, reported by Yeon *et al*, [10] for SET voltage and RESET power variation as shown in **Figures 2(b-c)**. Recall that the performance of a-Si devices is improved by replacing the Ag top electrode with alloyed Ag-Cu to yield high uniformity in SET and RESET processes.[10] The histogram of the SET voltage variation of our MoS_2 device is shown in **Figure 2b(i)**. The device exhibits a narrow distribution in the SET voltage with a range of only

0.04 V. In contrast, the histogram of SET voltage variation in a-Si/Ag-Cu device (**Figure 2b(ii)**) exhibits a range of 0.45 V, confirming the exemplary ultra-low C-C variability of MoS_2 based devices. Additionally, the RESET power distribution of MoS_2 device and a-Si/Ag-Cu device is shown in **Figure 2c**. Additionally, it is essential to investigate if the narrow distribution in SET voltages and RESET power is consistent over multiple devices. Therefore, a statistical analysis is performed over 12 different devices of areas $2 \times 2\ \mu m^2$, $5 \times 5\ \mu m^2$ and $20 \times 20\ \mu m^2$. Four devices of each area are measured to obtain the SET voltage and RESET power variation. The SET voltage distribution is obtained by enforcing CC that corresponds to a maximum current density of 40 A/cm^2. Therefore, for the devices with area of 4 μm^2, 25 μm^2 and 400 μm^2, a CC of 1.6 μA, 10 μA and 160 μA is enforced respectively. The individual DC characteristics of these devices are shown in **Figure S3**. The SET voltage distribution for each device is plotted in **Figure 2d**. Similarly, the RESET powers of the 12 devices are plotted in **Figure 2e.** The D-D variability is assessed by extracting the coefficient of variation ($CV = standard\ deviation\ (SD)/mean\ (\mu)$)[45] for both SET voltage and RESET power distribution over 12 different devices. The minimum C-C variability for SET voltage and RESET power is observed to be 0.32% and 2.79%, indicating ultra-low variability. Extracting CV over the entire sample set elucidates the low D-D variability observed in MoS_2 devices. The D-D variability increases to only 1.7% in SET voltage variation over the 12 devices. It is worth noting that the CV in SET voltage variation does not exceed 2% indicating the low D-D variability of MoS_2 devices.

The ultra-low variability MoS_2 devices are further characterized as synapses suitable for use in neural network training. DC potentiation (continuous SET) and depression (continuous RESET) measurements are performed by enforcing VC. A continuous SET process is performed by increasing the VC from 2 V to 2.6 V immediately followed by a continuous RESET by

increasing the magnitude of the negative reset stop voltage from -1 V to -2.5 V. The MoS_2 devices exhibit 4 distinct potentiation states and 5 different depression states, shown in **Figure 3a**, rendering preliminary indication of the ability of MoS_2 device to behave like an analog memory. The MoS_2 synapse exhibits excellent retention of >300 s for 26 distinct conductance states, as shown in **Figure 3b**. For evaluating the retention, the device is SET to a particular conductance state by enforcing a VC while performing a DC I-V sweep. Followed by this, the current through the device is read at a voltage of 0.1 V for 26 distinct states. Next, the conductance weight update is measured on 10 synaptic devices and is compared with the a-Si synapses reported by Yeon *et al.*[10] for C-C and D-D variability. For obtaining potentiation, 512 identical voltage pulses of duration 1 ms and amplitude 2 V are applied. To induce pulsed depression, 512 identical voltage pulses of 1 ms duration and amplitude -2.25 V are applied. The train of potentiation and depression pulses are repeated for 100 cycles, write current is measured, and write conductance is extracted for both potentiation and depression. The write conductance, normalized to the maximum conductance obtained, is plotted as a function of the pulse number (n), as shown in the weight update curve in **Figure 3c** for all 100 cycles, showing extremely low C-C variability. The pulsing scheme is shown as the inset of **Figure 3c**. To assess the C-C variability, asymmetric non-linearity factor (ANL) is extracted by the following equation:[10]

$$ANL = \frac{G_P(\frac{n}{2}) - G_D(\frac{n}{2})}{G_{max} - G_{min}} \quad (1)$$

where $G_P(\frac{n}{2})$ and $G_D(\frac{n}{2})$ are the median conductance values along potentiation and depression respectively; G_{max} and G_{min} are the maximum and minimum conductances, respectively. It is evident that the G_{max}/G_{min} ratio of the MoS_2 synapses is low. This can be improved either by increasing the thickness of MoS_2 or by implementing stack engineering which is beyond the scope

of this work. However, to avail the potential of these synapses we have incorporated the MoS_2 synapse in a pseudo-crossbar array of a 2-layer multi-layer perceptron (MLP) network with the support of a circuit-level macro model, NeuroSim.[46] The device parameters like G_{max}/G_{min} ratio, non-linearity factors in both potentiation and depression regimes along with C-C variability are used to obtain online learning accuracy of 70 %. Next, the ANL variation of 100 cycles in MoS_2 synapse is compared with ANL of 10 cycles in the a-Si/Ag-Cu synapse[10] as shown in **Figure 3d**. The MoS_2 synapse exhibits a tighter distribution in the ANL over 100 cycles in comparison to the modest 10 cycles observed in a-Si/Ag-Cu synapses. The weight update measurements are repeated on 10 distinct synaptic devices for 50 cycles each and the mean ANL is extracted for each device. The mean ANL over 50 cycles for 10 MoS_2 synapses is plotted and compared with the mean ANL obtained for 10 a-Si/Ag-Cu[10] synapses cycled only for 5 times as shown in **Figure 3e**. Further, we present the statistics of the weight update characteristics of MoS_2 synapses. The extraction of SD in ANL over multiple cycles provides the precise estimation of the C-C variability in the devices. Therefore, the SD in ANL is extracted for each synapse over 50 cycles. The extracted SD of the MoS_2 synapses (10 devices, 50 cycles each) is then compared to the SD of the a-Si/Ag-Cu[10] synapses (10 devices, 5 cycles each) as shown in **Figure 3f**. The MoS_2 synapses exhibit compact distribution in SD with a range of 0.02 which is superior to the SD distribution observed in a-Si/Ag-Cu[10] synapses where the range is 0.08. The consolidated table showing the ANL and the corresponding SD over at least 50 cycles for 10 MoS_2 synapses is shown in **Figure S4**. It is worth noting that this is one of the few reports in literature where the statistics (10 devices, at least 50 cycles for each device) on both C-C and D-D variability are provided for weight update characteristics. This statistical analysis of the weight update characteristics in MoS_2 synapses is

essential in establishing the low C-C variability of the technology, which justifies the viability of 2D materials in neuromorphic computing.

It is necessary to understand the underlying mechanism in MoS_2 synapses responsible for the low C-C variability. The scaling of resistance with respect to area is considered as a clear indication of the switching mechanism in memristive devices. MoS_2 synapses of area 2×2 μm^2, $5 \times 5 \mu m^2$, 10×10 μm^2 and 20×20 μm^2 are probed for DC I-V characteristics as shown in **Figure 4a(i)**. Here, each device is measured for 50 DC cycles. From the figure, it is evident that both HRS and LRS scale proportionately to the device area. The HRS and LRS are extracted at V_{Read}=0.2 V for 50 cycles and the scatter in the resistance values is represented through box plots for each device area in **Figure 4a(ii)**. Clearly, the HRS and LRS scale linearly with the area insinuating that the dominant switching mechanism is not due to the formation of a conductive filament which is independent of device area.[32] **Figure S5** shows the resistance scaling over 3 different device areas (5 devices for each area) measured for 1 DC cycle. The repeatable trend in resistance scaling with area over multiple cycles and multiple devices establishes that the switching mechanism in MoS_2 devices is interface mediated. However, we note that due to the dependence of LRS and HRS on device area, the variability might increase at nm-scale because of the introduction of edge effects.[47] The presence of Ti as the top electrode is critical for obtaining the low C-C variability. Please note that the Ti adhesion layer for the bottom Au electrode is retained while top electrode (Ti/Au) is replaced by 60 nm Au. In Ti/Au/MoS_2/Au (bottom to top) devices where Ti is not present, the device characteristics are gradual, indicating the role of the interface, but the switching is unstable and shows huge variability from one cycle to another (**Figure S6**). Next, I-V measurements are performed on 4 distinct Ti/Au/MoS_2/Ti/Au devices as a function of temperature which is varied from 300 K to 370 K. The I-V characteristics of a device, with an area of 5×5

μm^2, at both HRS and LRS regions as a function of temperature are shown in **Figure S7(a-b)**. The current in the HRS and LRS increases as the temperature increases for both bottom electrode injection (positive bias on bottom Au electrode) and top electrode injection (negative bias on bottom Au electrode) conditions. The I-V characteristics of the MoS_2 device are symmetric in spite of the dissimilar work-functions of the top Ti and bottom Au electrodes.[41] This indicates that the conduction in the HRS is not limited by the Schottky barrier at the electrodes. Among various mechanisms suggested to explain interface mediated switching, space charge limited conduction (SCLC) mechanism has been one of the strongest contenders.[48] The I-V curves obtained for various temperatures are fitted to explain the SCLC theory.[48-49] The current through the device is given by $I \propto V^{\alpha}$ where α is the slope extracted by plotting I-V in double logarithmic scale. The conduction in the devices that follow the SCLC theory has three distinct regions which can be distinguished by the extracted slopes. The devices where the transport is dominated by SCLC have an initial ohmic region at low voltages. The MoS_2 devices exhibit ohmic conduction at voltages <0.3 V, indicated by α= 1. At voltages >0.3 V, shallow trap SCLC dominates the conduction indicated by $\alpha \approx 2$. The transition voltage at which the current follows a higher than quadratic relationship is called V_{TFL} where the shallow traps get filled causing the current to increase. The slope at voltages higher than V_{TFL} (0.6 V) is observed to be >>2. The fitting data in both HRS and LRS regions are shown in **Figure 4(b-c)**. The band diagram indicating the underlying mechanism following the SCLC theory is shown in **Figure 4d**. The ohmic region is observed at lower voltage because of the lower concentration of injected carriers compared to the thermally generated carriers and impurities. **Figure 4d(i)** shows the band diagram in ohmic conduction mode. At voltages >0.3 V, shallow trap SCLC and SCLC conduction is observed where the electrode injects a larger number of carriers. **Figures 4d(ii-iii)** shows the band diagrams depicting the shallow-trap

SCLC and the SCLC after the V_{TFL}. The extracted slopes for each regime as a function of temperature for both HRS and LRS are shown in **Figure S8.** From **Figure S8**, it is worth noting that the I-V fitting for SCLC regime follows the 'Child's Law' due to the trapping/detrapping process at MoS_2/Ti (top) interface. However, the identification of defects contributing to these traps is out of scope of this work. Any atomic-level characterization to understand the contributing defects for the interfacial switching deserves a detailed study of its own. **Figure S9** shows that the I-V characteristics do not agree with the other transport mechanisms, such as Schottky emission, Poole-Frenkel emission and Fowler-Nordheim tunneling. The temperature-dependent I-V characteristics and the extracted slopes for the other three devices are shown in **Figure S10 (A-C)**, confirming similar conduction processes. **Figure S10 (D)** shows the temperature dependent I-V measurements executed on device of area 400 μm^2 with the temperature varying from 125 K to 370 K. From the I-V fitting, we observe SCLC conduction mechanism consistent with the high temperature I-V measurements.

To confirm the layer structure of MoS_2 and analyze the chemical composition of the sample before and after biasing, high resolution cross-sectional TEM was used. One biased device (100 DC cycles) and one pristine device from the same Ti/Au/MoS_2/Ti/Au sample with the lateral size of 4×4 μm^2 were analyzed. **Figure 5a** shows the top-view Scanning Electron Microscope (SEM) image of the pristine device; the location at which the FIB cut was done is marked with a black rectangle (*i.e.,* the protective Cr/C film deposited before the FIB cut). The MoS_2 stack can be clearly observed at the cross-point region in the SEM image, similar to Figure 1b. From the cross-sectional TEM image and the Electron Energy Loss Spectroscopy (EELS) profiles obtained in the pristine device (**Figures 5b** and **5c**) it is concluded that the structure of the fabricated device is Au/Ti/Si/MoS_2/Au (from up to down). From **Figure 5** two unexpected and critical observations

are made. First, there is an ultra-thin layer of Si in between the MoS_2 and the Ti layer, which most probably migrated from the Si/SiO_2 substrate due to the ~780 ºC applied during the sulfurization step adopted for MoS_2 growth. Secondly, while the structure of the MoS_2 is clearly layered, the orientation of its individual 2D layers varies from 0º to 90º with respect to the horizontal substrate plane (**Figures 5b and 5e**). Statistically, we find that this structure remains unaltered for the biased device (**Figures 5d-e**), indicating that the Au/Ti/Si/MoS_2/Au (up to down) stack is stable to the electrical stresses applied. It is worth noting that, as the switching mechanism is distributed (*i.e.,* shows area dependence and is analog, meaning that it is not based on the formation of local filaments), the observations in Figure 5e correspond to the switching regions. Most memristors employing MoS_2 as the switching medium[22, 50] were based on multilayer stacks of horizontally-aligned 2D MoS_2 planes, and in all cases the switching was filamentary and resulted in high C-C and D-D variability. On the contrary, the unconventional structure of our devices (based on a Si-rich highly crystalline MoS_2 of varying layer orientation) promotes smooth ion migration across it and results in analog resistive switching with ultra-low C-C and D-D variability (Figure 2). Among all mobile species within this Au/Ti/Si/MoS_2/Au structure, most probably the migration of O is the one responsible for the switching. The reasons that support this claim are: i) the signals of Mo, S, Si and Ti in the EELS profiles do not show significant changes, while the O profile does; ii) the MoS_2 is highly crystalline, meaning that forming S vacancies would require the applications of voltages much higher than those applied in our experiments (*i.e.,* up to 2 V in Figure 2);[51] iii) multiple studies have reported the formation of O-vacancies in memristive devices at low electrical fields;[52] and iv) the low variability is not observed without the Ti film which is known to be a very good O adsorber.

X-ray Photoelectron Spectroscopy (XPS) measurements were performed on a film of Au/Ti/MoS_2 (up to down) deposited using the same process used for the device fabrication. The XPS depth profiling is performed at 10 s intervals on the stacked film, and elemental spectra for Ti (2p), Mo (3d) and S (2p) were obtained after each etch step. From **Figure 5g(i)**, clear signatures of TiS_2, TiOS and TiO are observed at 456.2 eV, 457.6 eV and 455.1 eV respectively.[53-54] The binding energy peaks for TiO, TiS_2 and TiOS remain consistent for subsequent etch cycles as shown in **Figure S11a**.The presence of TiS_2 and TiOS indicate the migration of sulfur ions from the underlying MoS_2 layer post top electrode deposition. From the EELS spectra (**Figure 5f**), the change in the profile (post biasing) is indicative of the role played by 'O' vacancies in switching. Furthermore, XPS spectra (**Figure 5g(i)**) on pristine film reveals the formation TiO and TiOS, indicating the reservoir of 'O' vacancies is due to the presence of Ti contact metal. It is noteworthy that the control device with Au contact metal (**Figure S6**) shows high variability. Therefore, the requirement of Ti for obtaining low variability indicates that 'O' vacancies can be the dominant defect species that take part in SCLC mechanism. Analysis of the trap states from the contributing defects merit its own study. **Figure 5g(ii)** shows the XPS spectra of Mo (3d) where the binding energy peaks at 228.7 eV, 227.3 eV and 233.1 eV correspond to MoS_2, $MoSi_2$ and MoO_3 respectively.[55-57] The presence of $MoSi_2$ peak corroborates the observation by TEM and EELS. The subsequent etch cycles also show the presence of MoS_2, $MoSi_2$ and MoO_3 as shown by the corresponding spectra in **Figure S11b**. **Figure 5g(iii)** shows the XPS spectra of S (2p) where the peak binding energy at 162.4 eV signifies the presence of MoS_2, the peak at 161.09 eV corresponds to TiS_2, and the peak at 163.4 eV corresponds to TiOS.[53, 58] **Figure S11c** shows the S (2p) spectra for the subsequent etch cycles.

To establish the viability of these ultra-low variability synapses for circuit implementations, we proceed to connect multiple such synapses to demonstrate Boolean logic gate functionalities through vector matrix multiplication. Recently, we demonstrated LIF neurons using MoS_2 as the switching medium and Ag as the top electrode in a Au/MoS_2/Ag heterostructure.[37] Here, we integrate the MoS_2 synapses with those MoS_2 LIF neurons. The connection of MoS_2 synapses with MoS_2 neurons highlights the possibility of obtaining a monolithically integrated circuit of synapses and neurons. Typically, for the applications requiring the integration of neurons and synapses, these elements are realized with dissimilar materials necessitating heterogeneous integration. This process is wrought with issues in substrate incompatibility, cost and thermal budget. For the realization of large-scale circuitry, such as deep neural networks, monolithic integration of synapses and neurons is helpful.

The integration of MoS_2 synapses and neurons to realize AND, OR and NOT logic gates is shown in **Figure 6**. MoS_2 synapses and an external bias resistor are connected to one MoS_2 neuron. For enabling "integrate and fire" behavior of the neuron, a capacitor (C_0 = 100 nF) is connected as an integrator in parallel with the neuron. The individual MoS_2 neuron characteristics are shown **Figure S12**. The MoS_2 synapses are set at a particular resistance state, which acts as the weight of these synapses as shown in **Figure S13a**. For the implementation of logic gates, voltage pulse trains of amplitude V_i are applied as input to the i^{th} synapse bearing a certain weight (conductance) W_i, which results in current flowing through the path as $I_i = V_i \times W_i$ by Ohm's law. Thus, the current through all 'N-1' synapses and the external bias resistor add up by Kirchoff's law to $I = \sum_{i=1}^{N} V_i W_i$ which essentially is the vector matrix product of the input voltage and weight matrix. This total current at node 'B' (shown in Figure 6a) builds the potential across the capacitor C_0, charging it up. When V_B (shown in Figure 6a) exceeds the threshold voltage of the TSM, the

TSM switches on, allowing the capacitor C_0 to discharge through it. This causes V_B to reduce, which in turn switches the TSM back to its HRS. The process of charging and discharging of the capacitor continues, resulting in current spikes at the output of the circuit. To realize AND and OR logic gates, an input of '0' is represented by a train of low voltage pulses (amplitude 0.01 V, pulse width 1 ms), and '1' is represented by a train of high voltage pulses (amplitude 0.7 V, pulse width 1 ms). Similarly for NOT gate implementation, an input of '0' is represented by a train of low voltage pulses (amplitude -0.01 V, pulse width 1 ms), and '1' is represented by a train of high voltage pulses (amplitude -0.7 V, pulse width 1 ms). However, the input to bias resistor is varied since it is behaves like a differential resistor. For the bias resistor, a constant voltage of -0.7 V (AND and OR gate) and +0.7 V (NOT gate) is applied. The bias resistance is adjusted for the realization of each logic operation. If the circuit parameters determined by the synapse resistances allows the neuron to fire, the output is recorded as '1', else if the neuron does not fire, the output is considered as '0'. The voltage pulse trains are applied for 5 s. First, the synapses S1 and S2 are SET at particular weights or conductance states as shown by the retention plots in **Figure S13b-d**.

AND gate: The circuit used for the two-input AND gate realization is shown in **Figure 6a and S14a**. A bias resistor (R_O) of 100 kΩ is connected to the MoS_2 synapses S1 and S2. The truth table corresponding to the AND gate is shown in **Figure S14b**. Further, the output spiking characteristics for each input is shown in **Figure S14c**. The input pulsing scheme and the spiking output from the MoS_2 neurons for 1 s time period for various input combinations is shown in **Figure 6b**. The voltage pulse trains are applied for 5 s and the number of spikes is extracted and plotted as a function of inputs and time duration as shown in **Figure 6c**. The figure shows the

implementation of AND gate where spikes are obtained for input (1 1) and the absence of spikes is observed for the other input combinations, *viz.* of (0 0), (0 1) and (1 0).

OR gate: For the implementation of OR gate, the same measurement methodology as AND is used. The input pulse parameters are the same as those for the AND gate. However, we change the bias resistor (R_O) to a higher resistance of 470 kΩ. The use of a higher resistance effectively reduces the equivalent resistance of the RC circuit, which is necessary to obtain spiking in (0 1), (1 0) and (1 1) conditions. The schematic of the OR gate indicating the various input combinations and their corresponding outputs are shown in **Figure 6d**. Similar to the AND gate, the input pulsing scheme and spiking output for 1 s is shown in **Figure 6e**. The response of the OR gate for 5 s and the spiking output as a function of the input combination and time duration is shown in **Figure 6f**. The figure depicts the implementation of OR gate where output spikes are observed for (0 1), (1 0) and (1 1) input combinations and no spikes are observed for (0 0) condition. The number of spikes is higher for the (1 1) combination in comparison to the (0 1) and (1 0) combinations due to decreased equivalent resistance of the RC circuit. The circuit implementation, truth table and the output spiking characteristics of the OR gate for all input combinations are shown in **Figure S15**.

NOT gate: The NOT gate is implemented using one MoS_2 synapse and a bias resistor (R_O) of resistance 47 kΩ. The schematic of the NOT gate is shown in **Figure 6g**. The input pulses corresponding to '0' and '1' states are applied to the MoS_2 synapse. It should be noted that for implementing the NOT gate, the MoS_2 synapse plays the role of a differential resistor. A constant voltage of 0.7 V is applied to the bias resistor. The input pulsing scheme and spiking output is shown in **Figure 6h**. Further, the number of spikes is plotted as a function of time duration and inputs as shown in **Figure 6i**. The circuit diagram, truth table and the spiking characteristics of the NOT gate are shown in **Figure S16**. Output spikes are obtained for the '0' input condition. No

spikes are observed for the '1' condition because of the increased equivalent resistance of the circuit. This integration of MoS_2-based synapses and neurons exhibits a two-fold impact. First, it shows the viability of the MoS_2 memristors for circuit implementations, including vector matrix multiplication. Secondly, it proves that MoS_2-based neurons and synapses can be integrated together on the same materials platform, thus establishing the possibility of realizing monolithically integrated neural networks with these devices.

CONCLUSION

In conclusion, we have demonstrated ultra-low variability synapses using MoS_2 as the switching medium, and Ti/Au as the bottom and top electrodes. These devices exhibit excellent DC endurance characteristics while maintaining low cycle-to-cycle variability. Additionally, a comparison of MoS_2 synapses with a-Si/Ag-Cu synapses establishes even lower C-C variability in their weight update characteristics. The switching is facilitated by the interface between MoS_2 and Ti (top electrode) indicated by the area dependent resistance scaling. TEM images of pristine and biased devices confirm no physical degradation in the devices after cycling. The temperature dependent I-V measurements prove that the dominant conduction mechanism follows the SCLC theory. Finally, the ultra-low variability synapses are integrated with LIF neurons based on the same materials system, *viz.* MoS_2, to implement Boolean logic. This study clarifies the viability of these devices for future neuromorphic applications and edge computing.

METHODS

Device fabrication: The MoS_2 devices are fabricated using UV lithography. Bottom electrode is patterned, and 100 nm of Au with 5 nm Ti as the adhesion layer is deposited by e-beam evaporation. To obtain the MoS_2 film, 3 nm Mo is patterned and deposited by e-beam evaporation

on the bottom electrodes. Then, the samples containing the bottom electrodes and the patterned 3-nm-thick Mo film are placed in a quartz tube CVD furnace pre-loaded with Sulfur powder in alumina boat. The base pressure of the CVD furnace is brought down to ~ 1 mTorr with a mechanical pump. To remove any residual gases, the quartz tube is purged with Argon (Ar) gas. The furnace temperature is raised to ~ 780 ℃ in 50 mins and held there for an additional 50 mins. Continuous supply of Argon (Ar) gas flow is provided during the reaction between sulfur and Mo. The furnace is finally allowed to cool down to room temperature naturally. The sulfurization process converts metallic Mo to 2D MoS_2. Finally, the top electrode is patterned, and 6 nm Ti followed by 50 nm Au is deposited. Note that this fabrication process is free of any transfer step, which is simpler and cleaner than standard processes based on 2D materials transfer *via* polymer scaffolds. It is noteworthy that these devices have cross-point configuration which indicates the potential of the device for implementing cross bars. The synthesized CVD film consists of MoS_2 layers in random orientation as indicated by the TEM images.

Electrical Characterization: The MoS_2 devices are characterized using Keysight B1500A Semiconductor parameter analyzer. The devices are probed in Janis cryogenic probe station with a chamber pressure of 4×10^{-4} mBar. The weight update measurements, logic gate implementations were performed using the WGFMU B1530 A modules. For the logic gate realization, the MoS_2 neurons are probed at room temperature using a 6200 Micromanipulator probe station.

Material Characterization:

XPS: The XPS characterization is performed using Physical Electronics 5400 ESCA (XPS) system. Depth profiling was performed where the material was etched for total time of 100 s in 10

s interval. After etch cycle (10 s) elemental spectra of Ti (2p), Mo (3d) and S (2p) was obtained. The deconvolution of the peaks was executed using XPS peak 41 software.

TEM: For the protection of the samples and a good contrast in TEM images, 15 nm Cr and ~2 µm C were deposited on the sample by precision etching and coating system (model Gatan 682, PECS). The high resolution cross-sectional TEM images of the samples were taken as follows: 1) a focused ion beam (FIB, model HELIOS NANOLAB 450S, FEI) was used to cut the samples into ~2µm long and ~40 nm thick lamellas under 30 kV, 7.7 pA; 2) the thin lamellas were placed on a TEM copper grid for inspection using a micromanipulator; 3) the samples were analyzed in a high-resolution TEM (model JEM-2100, FEI) working at 200 kV in high vacuum (10^{-6} Pa). The chemical composition of the samples was analyzed by EDX (model Bruker super-EDS) and EELS (model Gatan) tools integrated in the TEM.

ASSOCIATED CONTENT

Supporting Information

The supporting information if available for free of charge at *ACS Nano* library. DC endurance of MoS_2/Ti/Au devices, Role of MoS_2 in switching, DC characteristics for SET voltage and RESET power distribution, Weight update statistics consolidated table for C-C variability, Area dependent resistance scaling for demonstrating D-D variability, DC characteristics of MoS_2/Au devices, Temperature dependent I-V and fitting data for 4 devices, XPS of Ti (2p), Mo (3d), S (2p) with depth profiling, MoS_2 LIF neuron characteristics, Retention of MoS_2/Ti/Au synapses for logic implementation, Logic gate implementation circuitry, truth table and the spiking outputs.

Acknowledgment

A.K. conceived the idea and T.R. directed this research. A.K fabricated the devices and performed the device characterization. D.D. performed MoS_2 neuron fabrication, neuron characterization and assisted with the monolithic integration of neuron and synapses. S.S.H. and C. Y. synthesized the MoS_2 films under the guidance of Y. J. H.S.C and T.S.B assisted with the TEM, EDS and FIB characterizations. Y.Q. and M.L. assisted with the TEM, EDS and EELS characterization of pristine and biased devices. All the authors analyzed the data, discussed the results, and contributed to the preparation of the manuscript. A. K., D. D. and T. R. were supported by NSF-ECCS-1845331 (CAREER). T.S.B was supported by the Technology Innovation Program (20010542) funded through the MOTIE, Korea. We acknowledge the NSF Major Research Instrumentation (MRI) Award No. 1726636 for measuring XPS spectra.

Conflicts of Interest

The authors declare no conflicts of interest

Data Availability

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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FIGURES

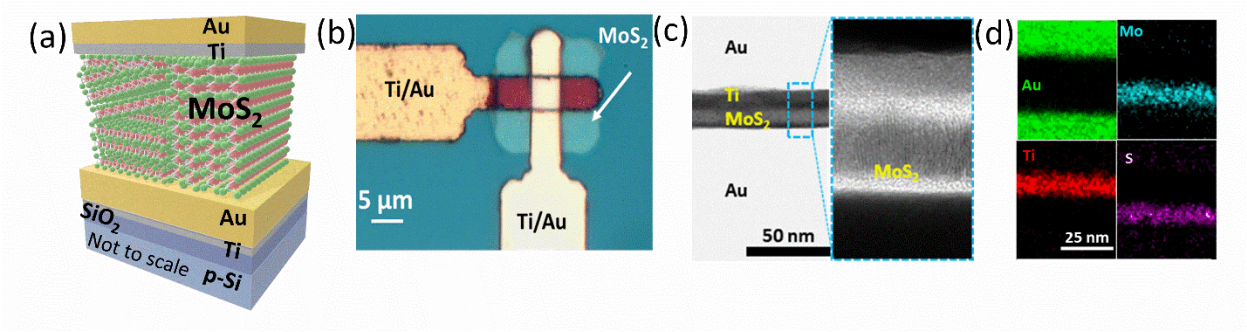

Figure 1. (a): Device schematic. **(b)**: Optical microscope image of a representative device. **(c)**: Cross-sectional TEM of the device. **(d)** EDS spectra showing the signature of MoS_2 and the electrodes; Au (bottom) and Ti/Au (top).

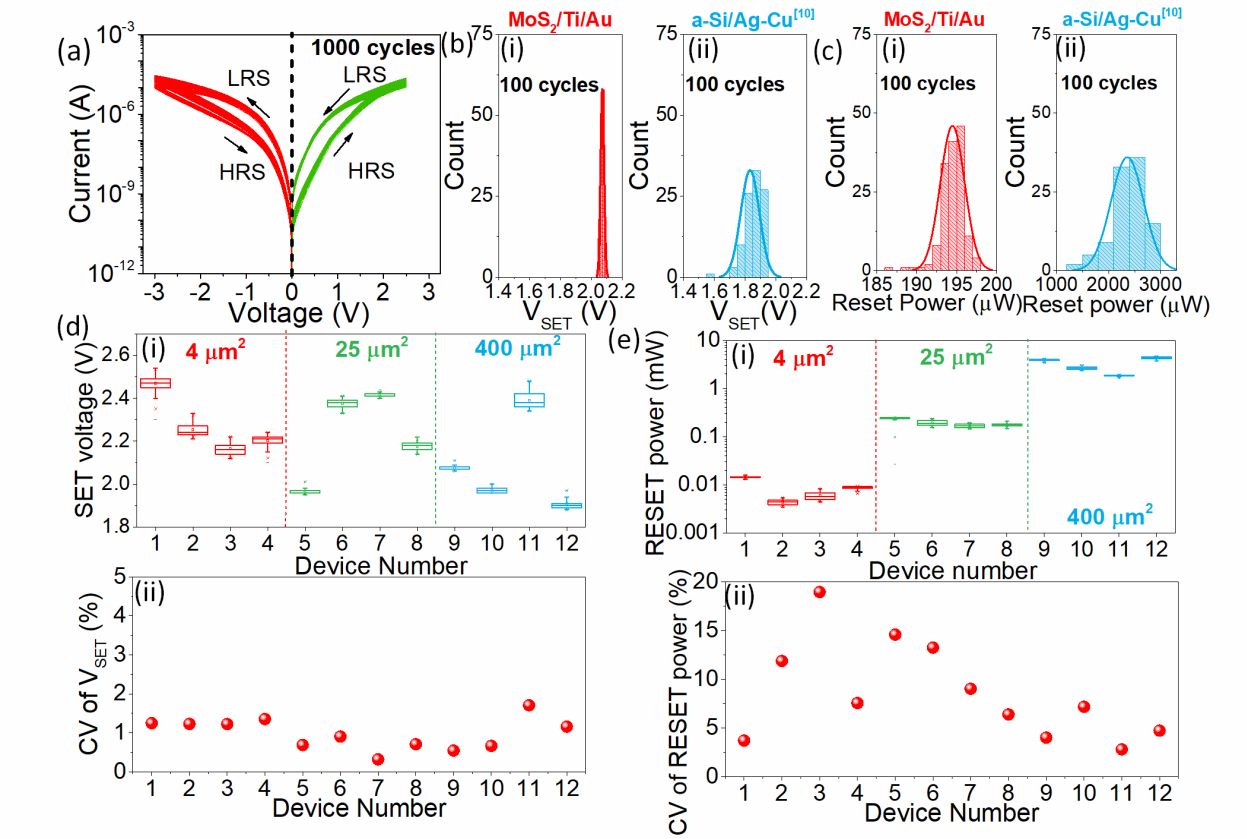

Figure 2. (a): DC cycling: 1000 cycles indicating the low C-C variability and endurance of MoS_2 devices. **(b)**: SET voltage comparison of **(i)** MoS_2/Ti/Au and **(ii)** a-Si/Ag-Cu based device where MoS_2 device exhibits a tight distribution of 0.04 V for 100 cycles **(c)**: RESET power distribution of **(i)** MoS_2/Ti/Au device and **(ii)** a-Si/Ag-Cu device. **(d). (i):** SET voltage distribution observed in 12 MoS_2/Ti/Au devices for >100 cycles. **(ii):** Coefficient of variation (CV) in the SET voltages in MoS_2. **(e). (i)**: RESET power distribution observed in 12 MoS_2/Ti/Au devices for >100 cycles. **(ii)**: Coefficient of variation (CV) in the RESET power in MoS_2 devices.

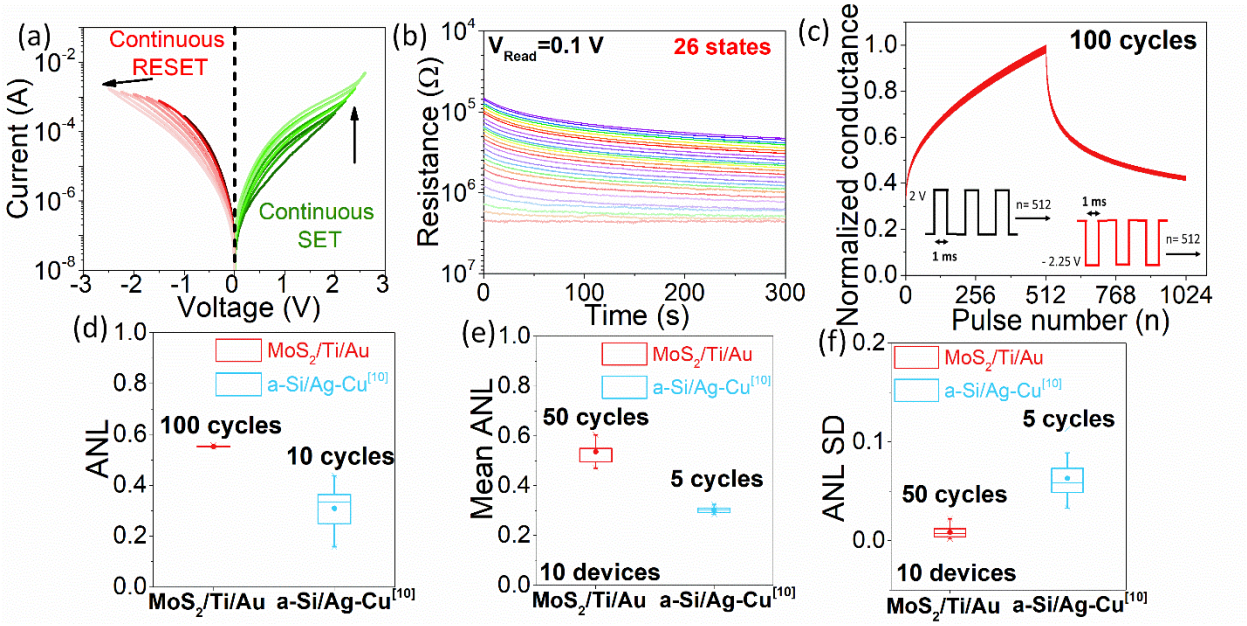

Figure 3. (a): DC potentiation and depression. **(b)**: Retention of ~300 s for 26 distinct states. **(c)**: Weight update characteristics repeated for 100 times. Inset: Pulsing scheme for each cycle. **(d):** ANL comparison of MoS_2 synapse (over 100 cycles) with a-Si synapse (over 10 cycles). MoS_2 synapses exhibit a tighter distribution in the ANL over the entire 100 cycles. **(e)**: Mean of the ANL extracted for 50 cycles plotted for 10 MoS_2 devices shows low variation. This is compared with the mean of the ANL extracted for 5 cycles plotted for 10 a-Si devices. **(f)**: The standard deviation (SD) of ANL for 50 cycles in MoS_2 devices is compared with the SD of ANL for 5 cycles in a-Si based devices for 10 devices in each case.

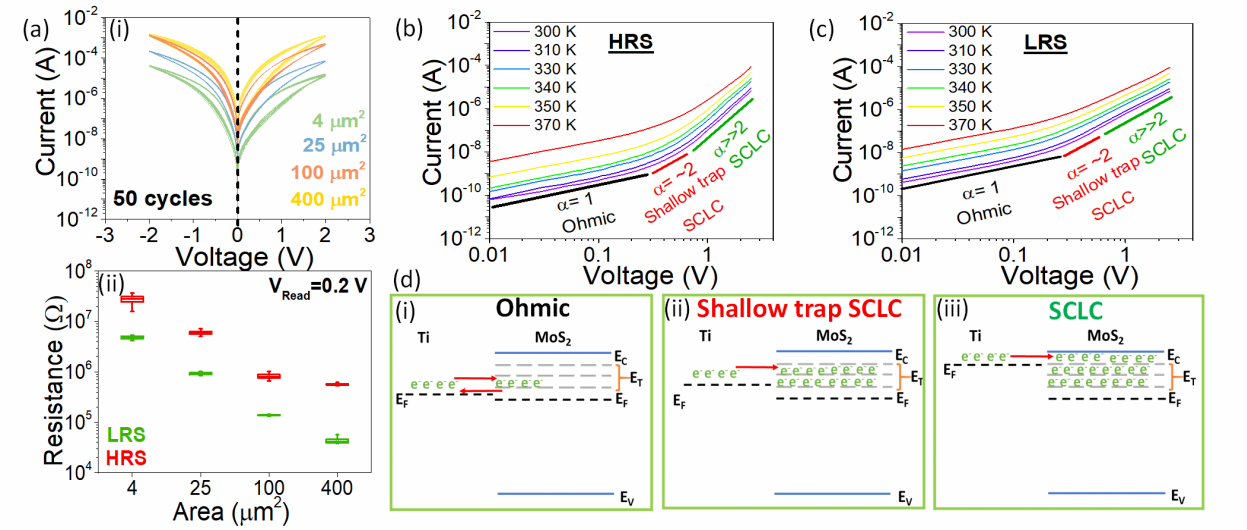

Figure 4. (a)(i): Area-dependent current scaling in MoS_2 devices of 4 different areas measured for ~50 cycles in each case. **(ii)**: HRS and LRS scaling for the 4 different areas, indicating the role played by the interface at MoS_2/Ti top electrode. The error bars represent data for 50 cycles. **(b)**: Temperature-dependent I-V at HRS state showing the increase in OFF current with increasing temperature. Ohmic conduction in lower voltage regimes of the HRS states. Shallow trap SCLC, and SCLC conduction mechanisms at higher voltages in HRS. **(c)**: Temperature-dependent I-V at LRS state where the ON current increases with increasing temperature. Ohmic conduction in lower voltage regimes of the LRS states and shallow trap SCLC, and SCLC conduction mechanisms at higher voltages in LRS. **(d):** Band diagram indicating **(i)** the ohmic conduction observed for voltage <0.3 V. **(ii)** the shallow trap SCLC conduction mechanism at voltages between 0.3 V-0.6 V where the current through the device follows a quadratic relation. **(iii)** the SCLC conduction mechanism at higher voltages where the shallow traps are filled and the current through the device shows a higher than quadratic relation.

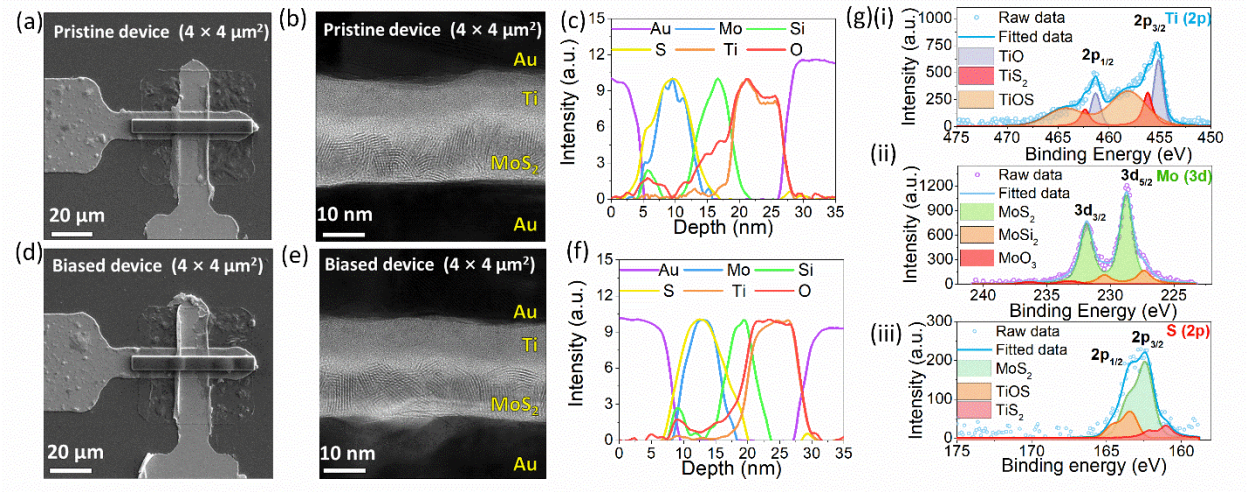

Figure 5. (a) SEM image of the pristine device with the FIB cutting location marked. **(b)** Cross-sectional TEM image of the lateral structure of the same pristine device in (a). **(c)** EELS map of the pristine device. **(d)** SEM image of the biased device (cycled 100 times) with the FIB cutting location marked. **(e)** Cross-sectional TEM image of the lateral structure of the same biased device in (d). **(f)** EELS map of the biased device. Scale in (a) and (d): 5 μm, scale in (b) and (e): 10 nm. **(g).** XPS spectra of Ti (2p), Mo (3d) and S(2p). **(i)** The binding energies of the $2p_{3/2}$ peaks are found at 455.1 eV, 456.2 eV and 457.6 eV correspond to the presence of TiO, TiS_2 and TiOS. **(ii)** Mo ($3d_{5/2}$) peaks at 228.7 eV, 227.3 eV and 233.1 eV correspond to the presence of MoS_2, $MoSi_2$ and MoO_3. **(iii)** S (2p) spectra indicating the formation of MoS_2, TiS_2 and TiOS due to the presence of peak binding energies at 162.4 eV, 161.09 eV and 163.4 eV.

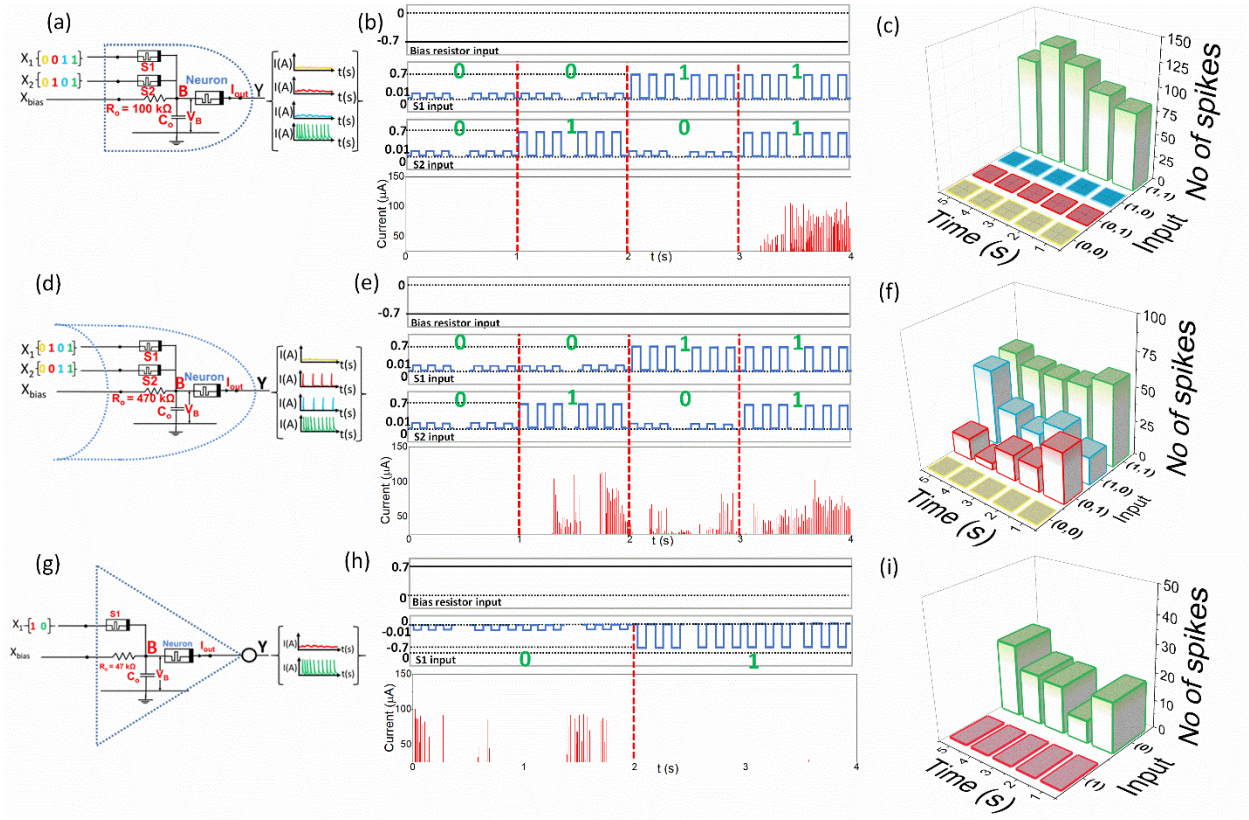

Figure 6. (a): Schematic of two-input AND gate implementation. **b**: Spiking output with corresponding inputs applied to the circuit. **(c):** Number of current spikes obtained from MoS_2 neuron as a function of time for (0,0), (0,1), (1,0) and (1,1) conditions. **(d)**: Schematic of two-input OR gate implementation. (**e)**: Spiking output with corresponding inputs applied to the circuit **(f)**: Number of current spikes obtained from MoS_2 neuron as a function of time for (0,0), (0,1), (1,0) and (1,1) conditions. **(g)**: Schematic of NOT gate implementation. **h**: Spiking output with corresponding inputs applied to the circuit **(i)**: Number of current spikes obtained from MoS_2 neuron as a function of time for (0) and (1) conditions.

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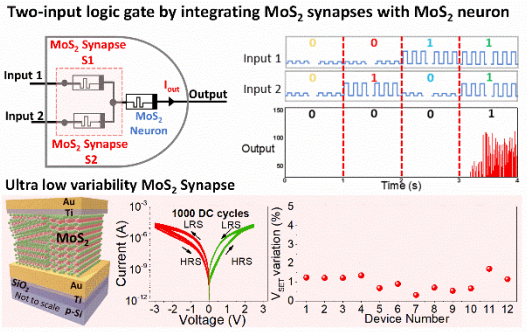
Two-input logic gate by integrating MoS2 synapses with MoS2 neuron
MoS2 Synapse S1
Input 1
Input 2
Iout
Output
MoS2 Neuron
MoS2 Synapse S2
Input 1
Input 2
Output
Time (s)
Ultra low variability MoS2 Synapse
Au
Ti
MoS2
SiO2
Not to scale
P-Si
1000 DC cycles
LRS
HRS
Current (A)
Voltage (V)
VSET variation (%)
Device Number