Phase Noise Analysis of Clock Generator by Using Phase Noise Sensitivity

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***Abstract*—Phase noise represents signal instabilities in the frequency domain and is assessed through power measurements at various offsets from the carrier frequency. Herein, the phase noise of a clock generator is analyzed and modeled. Sources for the phase noise of the clock output at the resonance frequency are identified, including the power supply, the heatsink, and the external crystal. Low-frequency resonance is detected and validated to be caused by the external crystal grounding design. Solutions to decrease crystal-related noise are proposed and validated. In addition, the sensitivity based on the signal-to-noise ratio is proposed and verified with measurements to numerically analyze the effects of power supply noise on clock phase noise. The proposed phase noise sensitivity is extracted from the measured phase noise results and can be used to estimate the phase noise and jitter of different power supply noises. The extraction and prediction methods are validated with different buffer types, including low-voltage differential signal, high-speed current steering logic, low-voltage positive emitter-coupled logic, and low-voltage complementary metal–oxide–semiconductor, in a device under test with the given design.**

***Index Terms*—Clock generator, crystal resonator, ground connection, jitter, phase noise.**

I. Introduction

CLOCK signals play critical roles in electrical and synchronous digital circuits. The performance of high-speed signals in electronic systems is highly dependent on the reference clock used to generate the signals [1], [2]. As digital data are processed or transmitted at increasingly higher speeds, the clock signal must be more stable and precise to ensure the quality of the signal on the receiver side [3], [4].

The quality of the clock signal can be quantified by measurement of the jitter and phase noise. In the frequency domain, phase noise is widely used to measure variations in signal timing. This noise is caused by time-domain instabilities and consists of fluctuations in the phase.

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Various potential noise sources may coexist in high-speed systems, thus requiring careful design. Power supply noise is a common contributor to timing jitter in circuits [5], [6], [7]. The heatsink, an indispensable component in electronic devices, usually involves conductive coupling and radiated emissions to the sensitive circuit [8], [9]. Quartz crystal is generally used as the frequency-determining device to produce a stable oscillator [10]. The quality of the crystal output determines the quality of the clock.

Herein, the root cause of the phase noise of a clock generator at the carrier frequency is first identified in a switch system. The power supply, heatsink, and external crystal are sources corresponding to the phase noise of the clock. The effect of each source is discussed. From the measurement results, spurious noise occurs at the frequency of the voltage regulator module in the phase noise. Low-frequency resonance is detected in the phase noise and is found to be caused by the ground routing design of the external crystal of the clock. Solutions to decrease this crystal-related noise are proposed and validated.

To formulate and investigate the influence of noise from the power supply on clock output, power supply induced jitter is a common variable quantity used to describe the time-domain's influence [11], [12]. Detailed information on the circuit design is required to estimate the power supply induced jitter performance. However, the circuit design for products is usually a "black box," and therefore is confidential, with only the input and the output available. To evaluate the performance of the black box, a behavioral model in the frequency domain based on the phase noise sensitivity (PNS) extracted from measurements of the input and output is proposed. With the extracted model, the performance in both the frequency domain and the time domain can be evaluated with the phase noise and the jitter, respectively.

The method is applied in different buffer types, including low-voltage differential signal (LVDS), high-speed current steering logic (HCSL), low-voltage positive emitter-coupled logic (LVPECL), and low-voltage complementary metal-oxide-semiconductor (LVCMOS). To evaluate the performance of each buffer, the PNS of each type of buffer is extracted and compared under the same ac-coupled termination scheme. With the extracted PNS, the phase noise and the jitter can be predicted. Furthermore, the transfer function of the power supply noise to the clock output can be generated.

This article is organized as follows. The phase noise measurement is introduced in Section II. Then the root cause of the

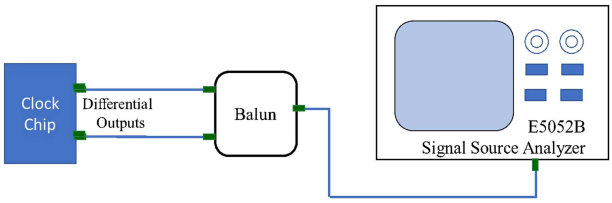

Fig. 1. Measurement setup diagram of the clock output phase noise.

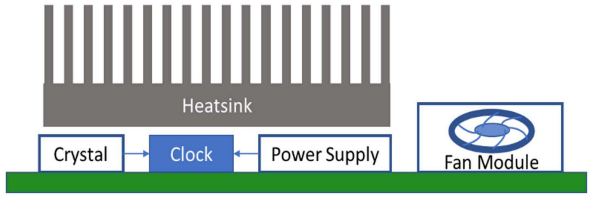

Fig. 2. Simplified illustration of the adjacent components near the clock generator IC.

measurement results is analyzed in Section III. The solution to suppress the phase noise of the clock generator output is also proposed in this section. Section IV discusses the influence of power supply noise on the clock output. The PNS is proposed and extracted from the measurements. The effects of different buffer types are compared and evaluated in Section V. Finally, Section VI concludes this article.

II. Phase Noise Measurements

In a high-speed serial link, the jitter of the transmitter is directly associated with the quality of the reference clock. The quality of the clock can be measured by the phase noise. The lower the phase noise, the more stable the clock, and thus, the less jitter of the transmitter.

Phase noise is a frequency-domain quantity representing the noise spectrum around the oscillator signal. Phase noise is typically described as a single sideband phase noise. It can be expressed as the ratio of the noise in a 1 Hz bandwidth at a specified frequency to the amplitude of the carrier signal [13]. The amplitude of the phase noise specification is expressed in dB relative to the carrier, which is denoted dBc

$$L(f)\,[\text{dBc}] \;=\; P(f)\,[\text{dBm}] - P_c\,[\text{dBm}] \tag{1}$$

Here, P represents the power density in the upper sideband of the carrier signal at frequency f.

Phase noise can be integrated over frequency bands to provide an rms phase jitter. A common bandwidth for the integration is 12 kHz to 20 MHz. The phase noise plot relates the time-domain jitter to the frequency-domain spectrum. The phase noise plot indicates the performance at each frequency point, and the rms jitter provides the total noise level in the time domain. The rms jitter at frequency f_c can be obtained by integrating the phase noise power over the sideband frequency range

$$\text{RMS Jitter}\;\;(s) = \sum \frac{\sqrt{2 \cdot A(f)}}{2\pi f_c} \tag{2}$$

where A is the area of the phase noise curve over each frequency segment

$$A\;(f) = \;\Delta f \cdot 10^{L(f)/10}. \tag{3}$$

Then, the rms jitter can be determined by integrating the rms jitter at each frequency within the frequency range.

Fig. 1 demonstrates the general setup of the phase noise measurement. The clock generator IC being tested belongs to a completed printed circuit board design with related circuits and accessory components (see Fig. 2). An E5052B signal source analyzer provides the phase noise function with a low noise floor, which is suitable for the measurement. The carrier frequency of the clock is 156.25 MHz. The differential outputs of the clock are soldered with semirigid coaxial cables at the pins and connected to a balun transformer. The single-ended output of the balun is connected to the signal analyzer.

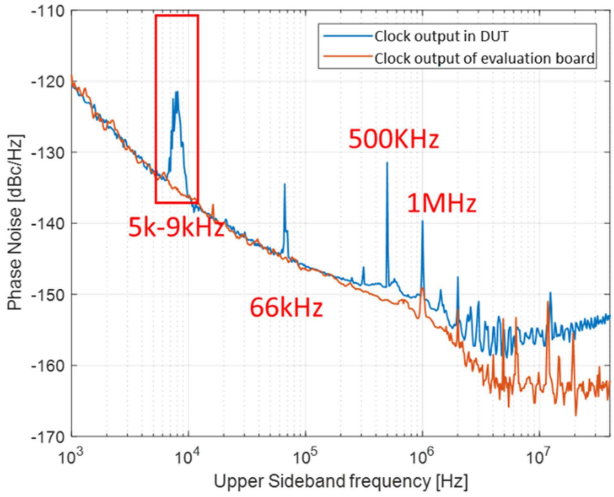

Fig. 3. Phase noise measurement results of the clock output.

The phase noise of the clock in the device under test (DUT) and that of the evaluation board is shown in Fig. 3. The rms jitter of the clock output from 12 kHz to 20 MHz is measured to be 135.8 fs. The total spurious noise in this range contributes 7 fs. The spurious noise in this measurement is defined as the peak exceeding three standard deviations. Furthermore, 5–9 kHz resonance contributes to a 38.8 fs rms jitter based on the phase noise measurement integrated by (2).

An evaluation board for the clock chip is measured as a clean reference. The evaluation board is designed with simpler circuit charged by USB driver while the DUT is a complicated circuit for a complicated system, as is shown in Fig. 2. The rms jitter of the evaluation board output is 80.7 fs. Compared with the results for the evaluation board, the DUT rms jitter is 55 fs higher, and more spurious noise is observed. Furthermore, the DUT contains a low-frequency resonance from 5 to 9 kHz. The root cause of the noise is investigated in the next section.

III. Root Cause Analysis

According to the phase noise measurement results, the power supply, heatsink, and external crystal are the potential sources

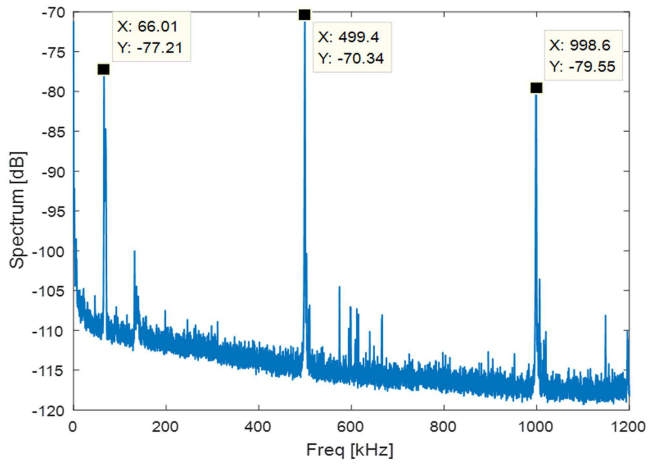

Fig. 4. Measured spectrum of the power net VDD1 V8.

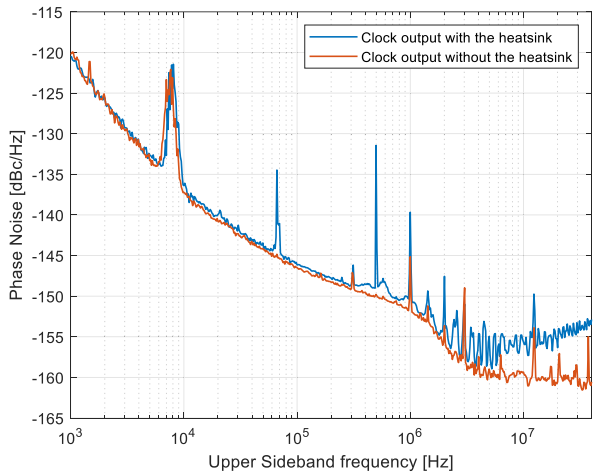

Fig. 5. Phase noise measurement results from the clock output measurement.

of the noise for the clock. Detailed explanations are provided in the following.

A. Power Supply

The voltage regulator module of the power supply for the clock switches at 500 kHz, thus further causing spurious phase noise. Furthermore, from the spectrum of the power supply, as shown in Fig. 4, 66 kHz is confirmed to be caused by the PDN. Nevertheless, all spurious noise is responsible for only 7 fs in the total rms jitter.

B. Heatsink

The heatsink is an indispensable component in electronic devices, which usually results in emissions or conductive coupling to the sensitive circuit. In this DUT, a 20 cm $\times$ 10 cm heatsink is placed above the circuits and connected to the reference ground by a screw, which is a potential radiation source to the circuit. Noise from the IC package and the microstrip traces can be coupled to the board-heatsink structure, thus causing radiated emissions [14], [15].

After removal of the heatsink, the total rms jitter from 12 kHz to 20 MHz decreases to 84.6 fs (see Fig. 5). Meanwhile, the spurious noise is also eliminated. The heatsink not only increases the noise level after 2 MHz but also induces the coupling of spurious noise from the power rail to the clock.

The heatsink is an indispensable component for thermal control, particularly in the design of high-speed circuits. Work has been conducted to provide guidelines for decreasing heatsink radiation, such as by adding an absorbing material or improving the structure of the heatsink [16].

C. External Crystal

Given that the resonance occurs from 5 to 9 kHz, it is usually considered as a random walk region [17]. In this frequency range, the noise source is usually considered the intrinsic source within the crystal quartz or the electrode structure [17], as shown in Fig. 6. Consequently, the noise in the 5–9 kHz range is suspected

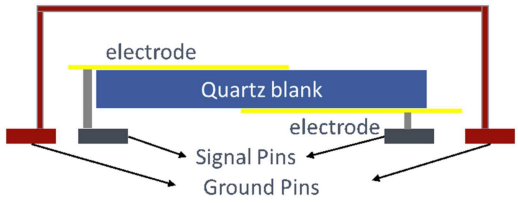

Fig. 6. Diagram of the four-port passive crystal chip structure.

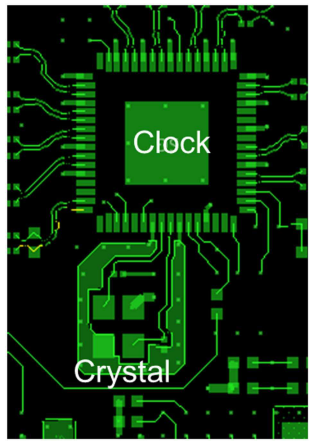

Fig. 7. Original design of the clock layout with an external crystal.

to be associated with the crystal. The quality of the crystal output determines the quality of the clock signal. An external quartz crystal is used in this DUT as the frequency-determining device to produce a stable oscillator.

A preliminary test is implemented for validation of this possibility. The original printed circuit board layout is shown in Fig. 7. By soldering the ground pin of the crystal to the surrounding ground pads, as shown in Fig. 8, the low-frequency shifts from 5–9 kHz to 10–14 kHz; the plot of the phase noise with such a connection is shown in Fig. 9. The results indicate that the resonance is associated with the crystal design.

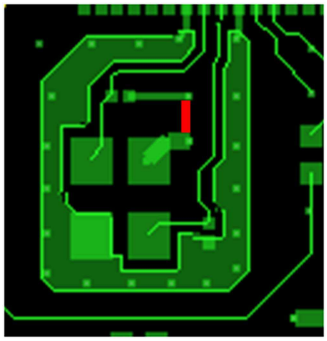

Fig. 8. Addition of a connection between the ground pin of the crystal and the surrounding ground pad in a preliminary test.

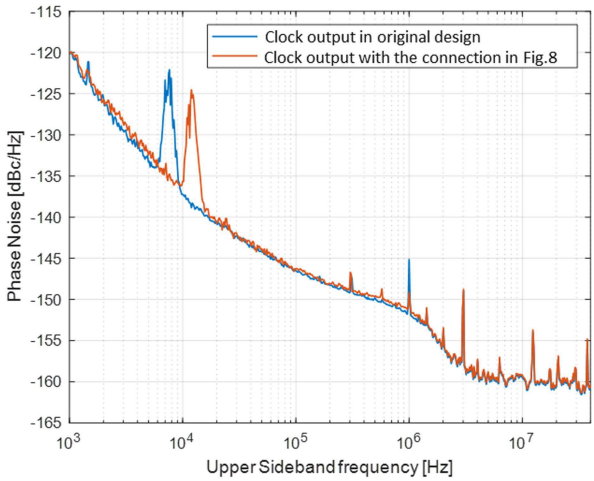

Fig. 9. Phase noise measurement results with the connection in Fig. 8.

As shown in the cross section of the crystal (see Fig. 6), the four-pin passive crystal chip consists of a quartz blank with two layers of electrodes where the grounding pins are connected to the metal lid. According to prior studies [18], [19], [20], the ratio between the dynamic capacitance and the static capacitance of the crystal affects the spurious vibrational noise. The change in the ground pin connection may affect the parasitic capacitance inside the crystal, thereby influencing the quality of the resonance signals.

For further investigation of the influence of the grounding connection, 3-D simulations of the crystal model with and without the connection are implemented. From the S-parameters of the models, the loop inductance between ground pins is calculated. The inductance of the model in Fig. 10(a) is 2.85 nH. The inductance of the model in Fig. 10(b) is 2.76 nH. The inductance difference caused by the connection is in nanohenry. The loop inductance change is excluded from the root cause of the noise source in the frequency range from 5 to 9 kHz. The possible cause in this frequency range is consequently identified as intrinsic sources within the crystal quartz or the electrode structure.

Adding copper tape to connect the crystal ground pins (see Fig. 11) suppresses the low-frequency noise (see Fig. 12). The

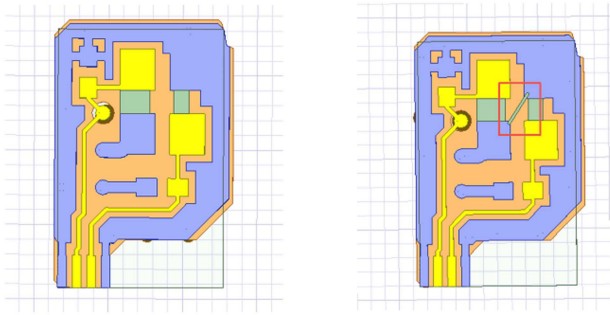

Fig. 10. 3-D simulation of the crystal layout (a) without and (b) with the grounding connection.

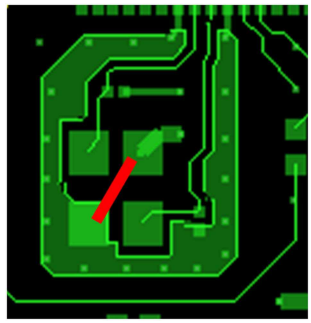

Fig. 11. Connection between ground pins.

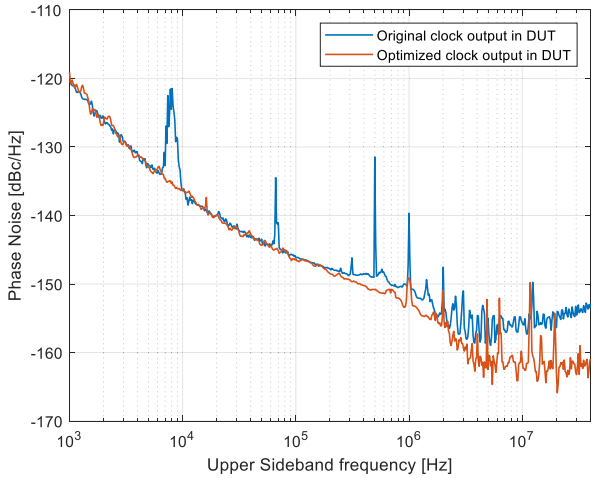

Fig. 12. Phase noise measurement results with the connection in Fig. 11 without the heatsink.

total jitter in this optimized condition is found to be 82.9 fs. All the main noise sources are thus identified and mitigated.

In summary, spurious vibrational noise can result in additional noise in the signal. Connecting the two ground pins in the layout design with traces for the four-port passive crystal is critical to avoid this noise.

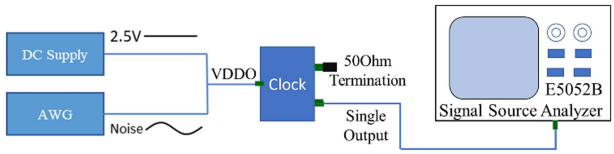

Fig. 13. Setup for measurement of clock phase noise with power supply noise injection.

IV. Power Supply Noise Analysis

To investigate the effects of power supply noise on the clock output, the sensitivity of the phase noise is proposed to model the black box. The PNS can be extracted from the measured phase noise and can help predict the phase noise and jitter with different power supply noises. To further compare the performance of different circuit designs, the transfer function is proposed. This function can be obtained from the extracted PNS and used to evaluate the noise rejection performance of the circuit.

A. Phase Noise Sensitivity

The measurement setup is shown in Fig. 13. The noise generated from an arbitrary waveform generator is injected into the output buffer supply to the clock generator. The original power supply for the clock buffer is 2.5 V. The signal source analyzer measures the phase noise of the clock output. To investigate the broad frequency characteristics of the phase noise performance, white Gaussian noise is injected from the power supply.

The PNS is defined by the signal-to-noise ratio (SNR) of the output supply $r_{V_{\text{out}}}$ and that of power supply $r_{V_{dd}}$ as

$$\text{PNS}\ (f) = \text{dB}\left(\frac{r_{V_{\text{out}}}}{r_{V_{dd}}}\right) = \text{dB}\left(r_{V_{\text{out}}}\right) - \text{dB}\left(r_{V_{dd}}\right) \quad (4)$$

where

$$r_{V_{dd}} = \frac{\Delta V_{dd}}{V_{dd\ \text{clean}}} \quad (5)$$

$$r_{V_{\text{out}}} = \frac{\Delta V_{\text{out}}}{V_{\text{out clean}}}. \quad (6)$$

Here, $V_{dd\ \text{clean}}$ is the dc voltage of 2.5 V, and $V_{\text{out clean}}$ is the clock output voltage without noise injection. ΔV_{dd} is the noise level injected from the arbitrary waveform generator. The measurement results from the signal analyzer in dBc are as in (1). The voltage of the output signal is then expressed with the phase noise result as

$$\begin{aligned}\text{dB}(V_{\text{out}}(f)) &= P(f)\,[\text{dBm}] - 10\log(R)\\ &= L(f)\,[\text{dBc}] + P_c\,[\text{dBm}] - 10\log(R).\end{aligned} \quad (7)$$

Here, R is the load impedance of the output.

To express the output difference caused by the power supply noise, first the output is expressed linearly as

$$V_{\text{out}}\ (f) = 10^{\frac{L_{\text{noisy}}(f)[\text{dBc}]+P_c[\text{dBm}]-10\log(R)}{20}}. \quad (8)$$

Then the difference is calculated as

$$\begin{aligned}\text{dB}(\Delta V_{\text{out}}(f)) &= \text{dB}\left(V_{\text{out}}\ (f) - V_{\text{out clean}}(f)\right)\\ &= \text{dB}\left(10^{\frac{L_{\text{noisy}}(f)[\text{dBc}]+P_c[\text{dBm}]-10\log(\text{R})}{20}}\right.\\ &\quad \left. - 10^{\frac{L_{\text{clean}}(f)[\text{dBc}]+P_c[\text{dBm}]-10\log(\text{R})}{20}}\right)\\ &= P_c\,[\text{dBm}] - 10\log(R)\\ &\quad + \text{dB}\left(10^{\frac{L_{\text{noisy}}(f)[\text{dBc}]}{20}} - 10^{\frac{L_{\text{clean}}(f)[\text{dBc}]}{20}}\right).\end{aligned} \quad (9)$$

The SNR of the output $r_{V_{\text{out}}}$ is then reformed as

$$\begin{aligned}\text{dB}\ (r_{V_{\text{out}}}) &= \text{dB}\left(\frac{\Delta V_{\text{out}}}{V_{\text{out clean}}}\right)\\ &= \text{dB}\left(\Delta V_{\text{out}}\ (f)\right) - \text{dB}\left(V_{\text{out clean}}(f)\right)\\ &= \text{dB}\left(10^{\frac{L_{\text{noisy}}(f)[\text{dBc}]}{20}} - 10^{\frac{L_{\text{clean}}(f)[\text{dBc}]}{20}}\right)\\ &\quad - L_{\text{clean}}(f)\,[\text{dBc}].\end{aligned} \quad (10)$$

With (9), the PNS in (3) can be expressed with the measured results as

$$\begin{aligned}\text{PNS}\ (f) &= \text{dB}\left(10^{\frac{L_{\text{noisy}}(f)[\text{dBc}]}{20}} - 10^{\frac{L_{\text{clean}}(f)[\text{dBc}]}{20}}\right)\\ &\quad - L_{\text{clean}}(f)\,[\text{dBc}] - \text{dB}\left(\frac{\Delta V_{dd}}{V_{dd\ \text{clean}}}\right).\end{aligned} \quad (11)$$

The PNS describes the influence of power supply noise on the clock output in the frequency domain and can be extracted from the measurement curves. Single-ended and differential outputs are under testing and analysis. The output signal is in LVDS mode, which is a widely used technique with low power consumption, low emissions, and low jitter for the clock logic design [21].

1) Single-Ended Output: In the measurement setup in Fig. 13, the single-ended output is connected to the signal source analyzer. Fig. 14 shows the phase noise result. The black curve labeled "No noise" represents the noise floor of the clock output when no additional noise is injected into the power supply. The colored curves show the phase noise resulting from different levels of white Gaussian noise. The power at the carrier frequency of 156.25 MHz is −1.60 dBm.

Fig. 15 demonstrates the PNS achieved from (10). As the frequency increases, the sensitivity increases. This increasing trend can be approximately described with a linear function. A binary linear fitted curve is extracted in a least-squares manner from the PNS with 0.5 V noise in Fig. 16. By using the fitted PNS extracted from the injected noise at 0.5 V, the phase noise can be solved from (11) as

$$L_{\text{predict}}\ (f) = \frac{\Delta V_{dd}}{V_{dd\ \text{clean}}} 10^{\frac{\text{PNS}\ (f)+L_{\text{clean}}(f)}{20}} + 10^{\frac{L_{\text{clean}}(f)[\text{dBc}]}{20}}. \quad (12)$$

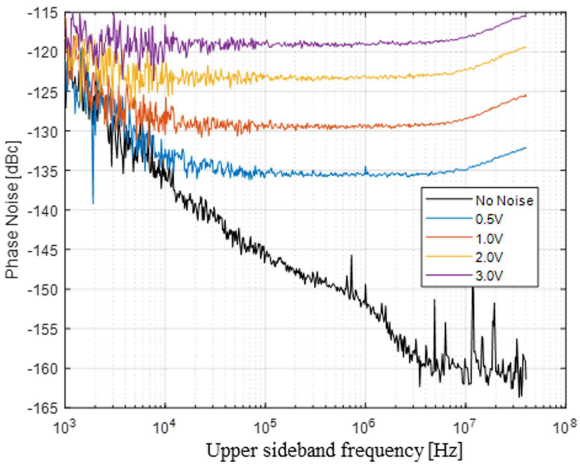

Fig. 14. Phase noise results from the single-ended clock output with different noise injection levels.

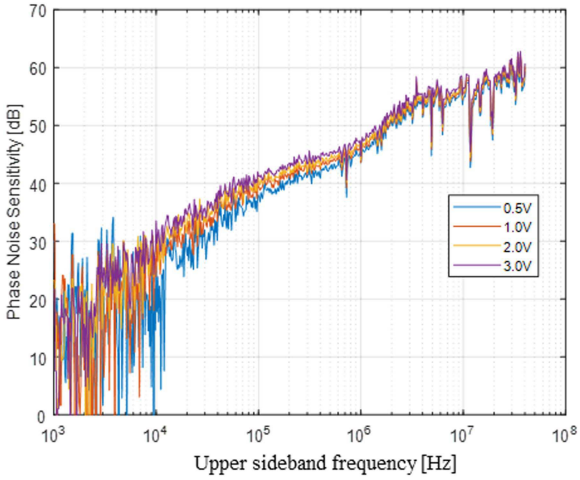

Fig. 15. PNS of the single-ended clock output with different noise injection levels.

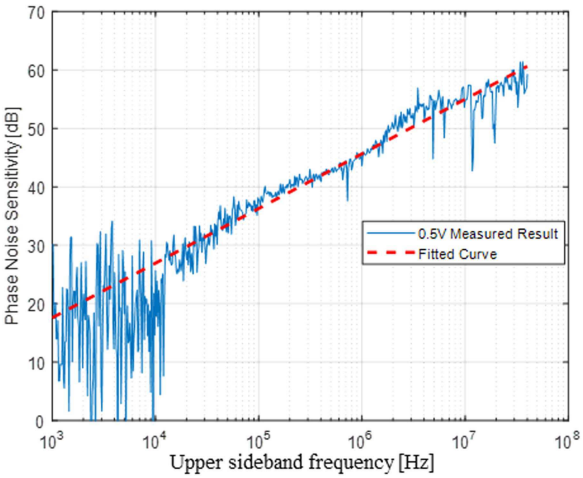

Fig. 16. Comparison of the PNS between the measured results and the fitted curve.

TABLE I
COMPARISON OF RMS JITTER BETWEEN MEASURED AND PREDICTED SINGLE-ENDED RESULTS

White Noise Amplitude (V)	Measured Jitter [fs]	Predicted Jitter [fs]	Error
0.5	1209.4	1310.7	8.3%
1.0	2507.9	2543.0	1.4%
2.0	5093.4	5249.5	3.1%
3.0	8175.0	8016.3	2.0%

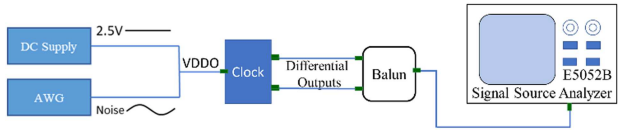

Fig. 17. Measurement setup of differential clock phase noise with power supply noise injection.

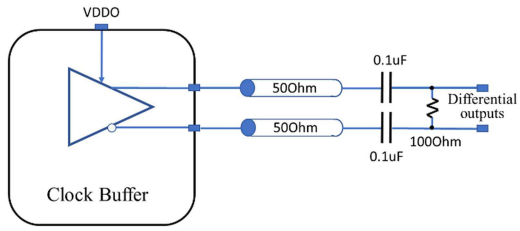

Fig. 18. AC-coupled termination at the clock output in the evaluation board.

Then with (2), the predicted jitter can be calculated with the predicted phase noise. Table I tabulates the comparison between the predicted and measured results. The prediction has less than 10% measurement error.

2) Differential Output: In the measurement setup in Fig. 17, the phase noise of the differential clock output is measured with a signal source analyzer through the balun. The ac-coupled termination is implemented on the clock evaluation board, as shown in Fig. 18.

The power at the carrier frequency of 156.25 MHz is −2.25 dBm. Fig. 19 shows the phase noise results, including the noise floor of the clock output and the phase noise results under different levels of white Gaussian noise. The differential design helps filter out the noise in the lower frequency range from 1 to 100 kHz. As a result, the extracted curve is fitted starting from 100 kHz from the PNS results shown in Fig. 20. The extracted PNS results are shown in Fig. 21.

Fig. 22 shows a comparison between the measured and predicted results by using (12). In reality, >1 V noise in the power supply is rare, with respect to the 2.5 V dc voltage level. The largest difference in the 1 V noise results between the measured

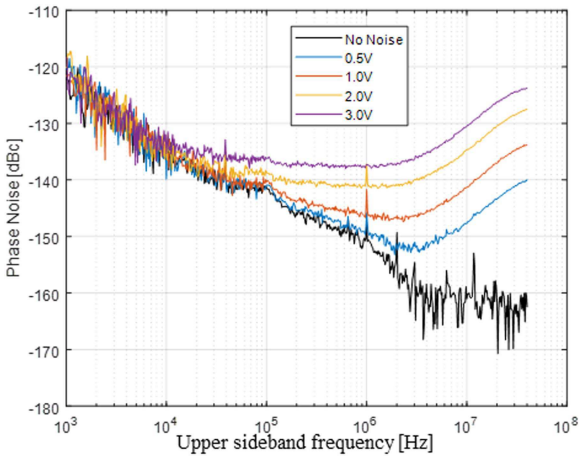

Fig. 19. Phase noise results from differential clock output with different noise injection levels.

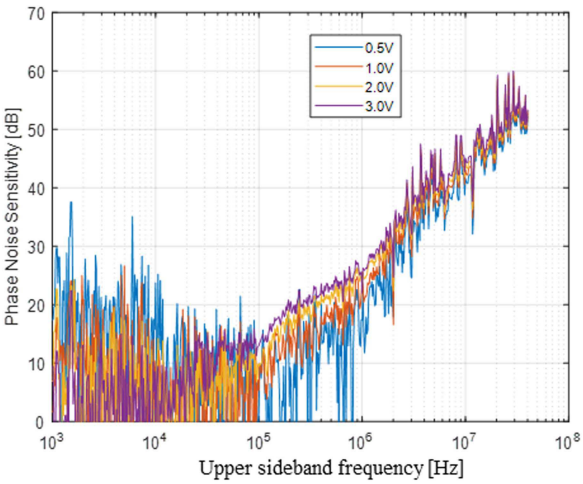

Fig. 20. PNS of differential clock output with different noise injection levels.

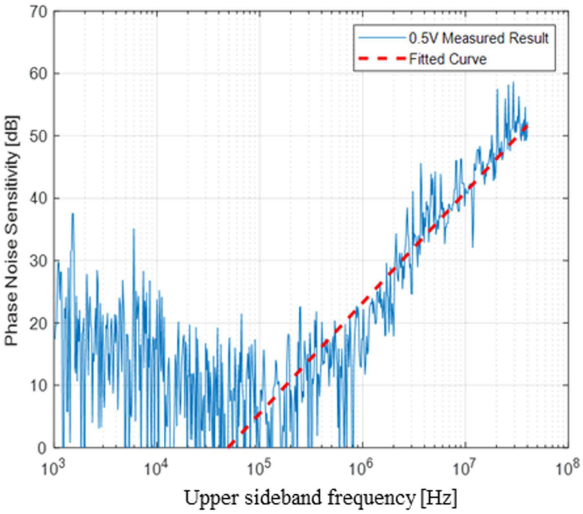

Fig. 21. Comparison of the PNS between the measured results and the fitted curve of differential output.

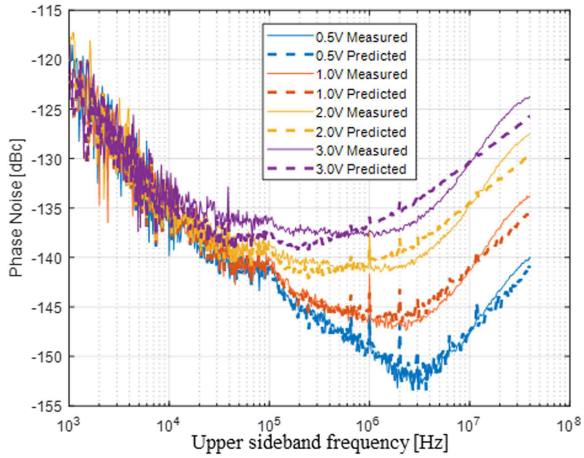

Fig. 22. Comparison of the phase noise between the measured and predicted results of differential output.

TABLE II
COMPARISON OF RMS JITTER BETWEEN MEASURED AND PREDICTED SINGLE-ENDED RESULTS

White Noise Amplitude (V)	Measured Jitter [fs]	Predicted Jitter [fs]	Error
0.5	308.5	303.3	1.6%
1.0	642.8	617.3	3.9%
2.0	1285.0	1183.3	7.9%
3.0	2100.5	1890.9	9.9%

and predicted values is 2 dBc at 40 MHz. Table II tabulates a comparison between the predicted and measured results. The prediction has less than a 10% measurement error. The error increases with increasing noise level because the predicted curve is generated from the 0.5 V noise result. The gradient for the results with different noise levels varies slightly (see Fig. 20).

V. COMPARISON OF THE EFFECTS OF DIFFERENT DRIVER TYPES ON POWER SUPPLY NOISE

LVDS, HCSL, LVPECL, and LVCMOS are common types of clock logic [22], [23]. The benefits and tradeoffs of the four different types have been compared in prior studies [24], [25] and are listed in Table III. According to the table, LVDS and LVPECL share the same advantages. Comparison of the two designs indicates that LVPECL requires external resistors for both transmitter and receiver terminals, whereas LVDS requires only single termination at the receiver.

For evaluating the performance of power supply noise rejection, the differential clock design is tested for the four types of logic on a given design. White noise (1 V) is injected into the power supply (see Fig. 23). All dashed lines in Fig. 23 represent the noise floor without noise injection. All solid lines represent the results of injection of 1 V white noise. The power of the carrier frequency of each design is listed in Table IV.

TABLE III
COMPARISON OF THE CHARACTERISTICS OF DIFFERENT DESIGNS

	Power Consumption	Speed
LVDS	Low (~20mW)	Fast (>GHz)
HCSL	High (~50mW)	Fast (>GHz)
LVPECL	High (~100mW)	Fast (>GHz)
LVCMOS	Low (~10mW)	Slow (~100MHz)

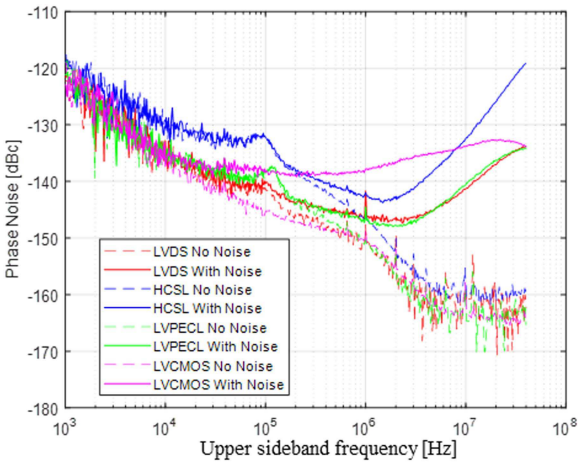

Fig. 23. Phase noise measurement results of the four designs.

TABLE IV
MEASURED AND PREDICTED JITTER FOR THE FOUR DESIGNS

	White Noise: 0.5 V		White Noise: 1 V	
	Measured Jitter [fs]	Predicted Jitter [fs]	Measured Jitter [fs]	Predicted Jitter [fs]
LVDS	308.5	303.3	642.8	617.3
HCSL	928.4	923.3	1920.1	1908.9
LVPECL	299.5	331.8	630.8	667.2
LVCMOS	577.1	633.9	1180.9	1299.2

The PNS of each design is plotted in Fig. 24 with solid lines, as calculated from the measurement results in Fig. 23. The extracted PNS from the measurements is plotted with dashed lines. With the extracted PNS, the jitter can be predicted for different injected noise levels. Table IV tabulates the comparison between the measured and predicted jitter calculated from the extracted curve. Furthermore, the extracted PNS can also help estimate the phase noise level of the sinusoidal noise, which is common in real products. A 1-V sinusoidal noise at 3 MHz is

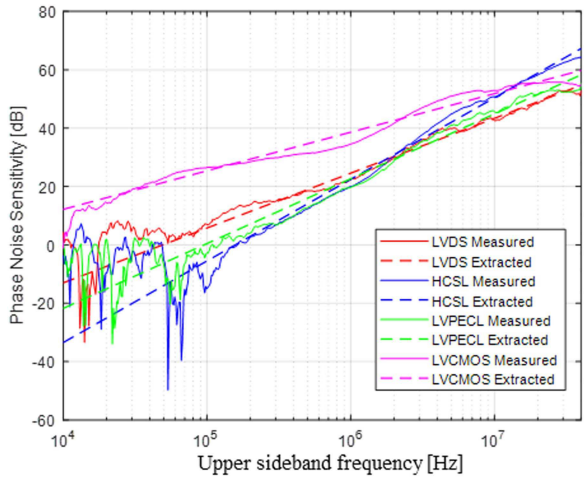

Fig. 24. Measured and extracted PNS for the four designs.

TABLE V
MEASURED AND PREDICTED PHASE NOISE PEAK VALUES FOR THE FOUR DESIGNS

	Measured result [dBc]	Predicted result [dBc]	Error
LVDS	-112.5	-110.4	2.0%
HCSL	-103.8	-103.1	0.7%
LVPECL	-98.7	-97.8	1.0%
LVCMOS	-109.8	-109.1	0.6%

injected into the power supply for validation. Table V tabulates a comparison between the predicted peak value of the phase noise and that of the measured results.

VI. CONCLUSION

Herein, the root causes of the phase noise of the clock output at the carrier frequency have been analyzed and identified. The total rms jitter measured from 12 kHz to 20 MHz at the carrier frequency is 135.8 fs. The power supply, heatsink, and external crystal are the relevant sources of phase noise. Spurious noise occurs at the frequency of the power supply module in the phase noise results. The heatsink over the clock induces conductive coupling noise in the clock signal with a 50 fs rms jitter. The low-frequency resonance with a 38 fs rms jitter is induced by the external crystal of the clock but can be suppressed by improving the ground routing of the crystal.

To further investigate the effects of power supply noise on the clock output, the PNS is proposed and analyzed. The steps to implement the PNS for the black box evaluation are as follows:

1) inject 0.5 V power supply noise into the DUT;
2) measure the phase noise of the clock output;
3) extract PNS from the measured results;
4) estimate the phase noise and jitter of the DUT with different power noise.

With the extracted PNS, the phase noise and jitter can be predicted with different injected noise, including sinusoidal noise and white Gaussian noise.

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