An Empirical Modeling of Far-End Crosstalk and Insertion Loss in Microstrip Lines

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***Abstract*—The difference in the dielectric permittivity of the different dielectric layers (including air) surrounding the microstrip is one of the major contributors to the far-end crosstalk (FEXT) in microstrip lines. The dielectric of the microstrip in printed circuit boards (PCBs) fabrication usually consists of two layers: the solder mask layer and the substrate layer. The characterization of the relative permittivity (ε_r) and dielectric dissipation factor ($\tan\delta$) for the dielectric layers of the microstrip are important parameters for board-level electronic system designs. In addition, the foil surface roughness cannot be ignored for the conductor loss modeling. In this work, an extraction method with high accuracy is proposed to characterize the dielectric material and foil surface roughness properties from the measured S-parameters with known cross-sectional geometry up to 20 GHz. With the extracted properties, the FEXT and insertion loss of the microstrip can be estimated more accurately, providing design guidelines for PCB design and the material selection of the microstrip.**

***Index Terms*—Delta-L, dielectric material characterization, extended unterminated line (EUL), far-end crosstalk (FEXT).**

I. Introduction

THE microstrip line is a commonly used transmission line structure in RF and microwave designs for its low fabrication cost and high layer utilization. However, compared with striplines, microstrip lines suffer from relatively higher FEXT compared to stripline because of the air dielectric which surrounds the microstrip line [1], [2], [3]. Hence, it is important to accurately control and predict the FEXT of the microstrip. Therefore, an accurate estimation of the parameters of the microstrip line is critical for circuit performance modeling, including the loss and the FEXT.

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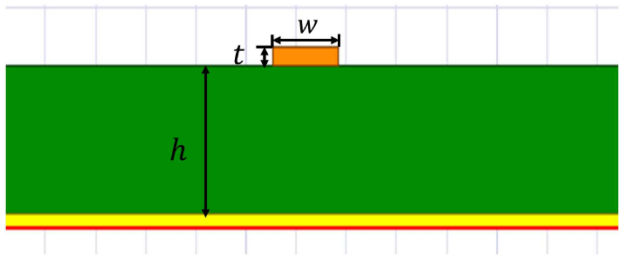

Fig. 1. Cross-sectional geometry of a simplified microstrip.

Many techniques were developed to characterize the material properties of printed circuit board (PCBs), such as the new rapid plane solver [4], the short-pulse propagation technique based on time-domain reflectometry measurements [5], and the ring resonator method [6]. However, these methods require a special design or additional measurement to extract the dielectric material properties. S-parameters, which describe the electrical behavior of electrical networks, are widely used in electronics, communication systems design, and microwave engineering. Meanwhile, the material properties may vary from the raw material after fabrication. Therefore, the extraction based on S-parameters measured on fabricated microstrip is more accurate and practical in actual design.

A new approach to the extraction process is proposed in the previous paper [7]. The per-unit-length (PUL) inductance and capacitance of the air-filled line are obtained using an accurate 2-D solution of the transmission line cross-section, and the approximated analytical expression is used only to relate the effective permittivity of the transmission line to the actual permittivity of the dielectric layer. However, this proposed method is limited to a simplified microstrip structure as shown in Fig. 1, without considering the effects of the solder mask.

The dielectric of the microstrip in PCB fabrication usually consists of two layers: the solder mask layer and the substrate layer. Yong et al. [8] and Liu et al. [9] proved that the inhomogeneity between the dielectric layers is a critical reason for the FEXT. In practice, the permittivity of the solder mask is generally higher than that of the substrate [2]. As a result, aside from the inhomogeneity between the air and the substrate in the simplified microstrip structure, the solder mask layer will help reduce the FEXT by introducing additional (with opposite effects on crosstalk polarity) inhomogeneity between

TABLE I
SUMMARY OF THE MICROSTRIP CHARACTERIZATION METHODS

Method	Cons	Pros
Rapid plane solver	Requires special test fixture design and/or multiple measurements	Extraction of the pure dielectric properties without de-embedding error
Short-pulse propagation		
Ring resonator		
Insertion loss measurement only	Only effective permittivity dielectric substrate can be extracted, resulting in low FEXT prediction accuracy	Minimal Number of Measurements
Insertion loss and FEXT measurement (proposed)	Requires one additional EUL structure for accurate FEXT measurement	Permittivity of the substrate and solder mask layer can be separated from S-parameter measurement

the dielectric layers [2], [3]. Previous models use only provide one effective dielectric constant value for surrounding dielectric layers, neglecting the impact of a thin solder mask between the air dielectric layer and substrate dielectric layer. As a result, an accurate estimation of the permittivity of each dielectric layer is critical for FEXT modeling. The comparison between the existing microstrip characterization methods to the proposed method is shown in Table I.

The extended unterminated line (EUL) structure was proposed in [10] and [11] to achieve convenient and accurate FEXT measurements. It is widely used for high-volume PCB tests because the EUL structure reduces the required ports by half while eliminating the requirement for expensive test equipment with additional ports. In addition, the structure is proven to eliminate the impact of FEXT due to mismatched terminals in the time domain [10]. Delta-L structures are differential transmission lines with different lengths [12]. With the de-embedding procedure [13], [14], the vias and fixture effect can be removed so that S-parameters of the transmission line are obtained. To accurately characterize the inhomogeneous dielectric material of microstrip, the dielectric permittivity (ε_r) is extracted for solder mask and substrate using measured S-parameters and cross-sectional geometry of both Delta-L and EUL structures.

To accurately model the loss, the dielectric dissipation factor and the surface roughness are critical factors. To model additional conductor loss due to foil surface roughness, various empirical or physical models have been brought up to provide surface roughness correction factors for the PUL resistance assuming certain roughness of foil conductors. The dielectric dissipation factor can also be extracted with the measured S-parameters. With all the extracted parameters: the dielectric permittivity ($\boldsymbol{\varepsilon_r}$) of the dielectric layers, the dissipation factor, and the foil surface roughness, the performance characteristics like the FEXT and the loss of the microstrip can be estimated.

As part of the paper organization, in Section II, the algorithm of the $\boldsymbol{\varepsilon_r}$ extraction for different layers is introduced. Both the simplified microstrip that only contains the substrate layer and the practical microstrip model with solder mask layer is extracted. Section III provides the extraction of the foil surface roughness and the correction factor for the resistance caused by that. Section IV shows the dissipation factor extraction for the insertion loss modeling. In Section V, the design guideline to mitigate the FEXT of the microstrip is provided. Finally, Section VI concludes this article.

II. PERMITTIVITY EXTRACTION METHODOLOGY

A. Homogeneous Model Extraction

The simplified cross-sectional geometry of the microstrip line is shown in Fig. 1. A conductor of thickness t and width w is fabricated on a dielectric substrate of thickness h above a ground plane. The dielectric constant of the homogeneous medium that equivalently replaces the air and dielectric regions of the microstrip are defined as the effective permittivity (dielectric constant) [15].

The propagation constant γ of a single-ended transmission line can be expressed through the PUL parameters as

$$\gamma = \sqrt{(R + j\omega L)(G + jwC)} \tag{1}$$

where R, L, G, and C represent the per-unit length resistance, inductance, conductance, and capacitance of the transmission line. For practical low-loss transmission lines, the following conditions are true: $R \ll j\omega L$ and $G \ll j\omega C$. Using Taylor series expansion, the attenuation factor α and phase constant β, in this case, can be approximated as [15]

$$\alpha = \text{real}(\gamma) \approx \frac{1}{2}R\sqrt{\frac{C}{L}} + \frac{1}{2}G\sqrt{\frac{L}{C}} \tag{2}$$

$$\beta = \text{image}(\gamma) \approx \omega\sqrt{CL}\,. \tag{3}$$

Due to the definition of the effective dielectric constant, the capacitance C can be calculated by scaling the capacitance of the air-filled transmission line C_{air} (i.e., the capacitance calculated from the geometry only) by the effective dielectric relative permittivity ($\varepsilon_{r\_\text{eff}}$) in [16], eq. (4.36)

$$C = C_{\text{air}}\,\varepsilon r_{\text{eff}}. \tag{4}$$

Considering that the inductance L is not affected by the dielectric material (its relative permeability is assumed to be equal to 1), the inductance of the air-filled transmission line L_{air} is the same as L. Then, the phase constant β can be expressed as

$$\beta \approx \omega\sqrt{C_{\text{air}}\varepsilon_{r_{\text{eff}}}L_{\text{air}}}\,. \tag{5}$$

If the cross-sectional dimensions of the transmission line are known, C_{air} and L_{air} can be calculated by solving the 2-D cross-sectional problem using an appropriate solver (Ansys Q2D in our case).

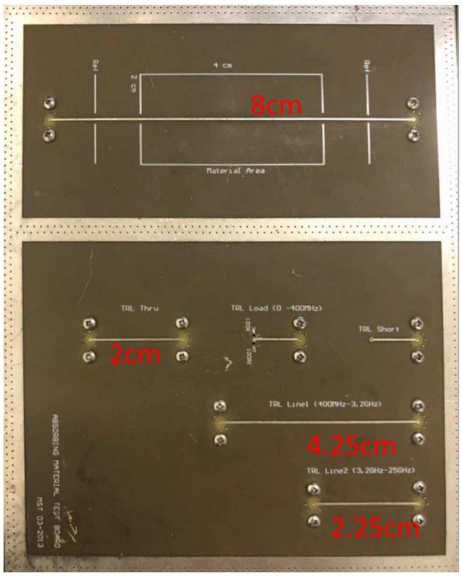

Fig. 2. Microstrip test coupon. The trace thickness t is 0.046 mm. The trace width w is 0.4318 mm. The thickness of the dielectric h is 0.24 mm.

When the S-parameters of the line are measured with the impedance of the ports perfectly matched to the characteristic impedance of the line, the phase constant can be expressed as

$$\beta = \left| \frac{\arg(S_{21})}{l} \right|. \tag{6}$$

In the practical measurement by a vector network analyzer (VNA), the de-embedding procedure (such as TRL and 2X-Thru) is essential to eliminate the impedance mismatch.

In [17], Bahl and Bhartia proposed an analytical expression for the effective dielectric constant of a microstrip line as

$$\varepsilon_{r\_\text{eff}} = \begin{cases} \frac{\varepsilon_r+1}{2} + \frac{\varepsilon_r-1}{2}\left[\left(1+\frac{12h}{w}\right)^{-\frac{1}{2}} + 0.04\left(1-\frac{w}{h}\right)^2\right] \\ \qquad -\frac{\varepsilon_r-1}{4.6}\frac{\frac{t}{h}}{\sqrt{\frac{w}{h}}} & \frac{w}{h} \le 1 \\ \frac{\varepsilon_r+1}{2} + \frac{\varepsilon_r-1}{2}\left(1+\frac{12h}{w}\right)^{-\frac{1}{2}} - \frac{\varepsilon_r-1}{4.6}\frac{\frac{t}{h}}{\sqrt{\frac{w}{h}}} & \frac{w}{h} > 1 \end{cases}. \tag{7}$$

By inverting (7) and combining it with (5) and (6), the dielectric constant of the substrate ε_r can be extracted from the S-parameter and the cross-sectional geometry. The final formula of ε_r expressed with measured S-parameter and 2-D solver result is

$$\varepsilon_r = \begin{cases} \frac{\frac{2}{C_{\text{air}}L_{\text{air}}}\left(\frac{\arg(S_{21})}{l\omega}\right)^2 - 2}{1+\left(1+\frac{12h}{w}\right)^{-\frac{1}{2}} + 0.04\left(1-\frac{w}{h}\right)^2 - \frac{\frac{t}{h}}{2.3\sqrt{\frac{w}{h}}}} + 1 & \frac{w}{h} \le 1 \\ \frac{\frac{2}{C_{\text{air}}L_{\text{air}}}\left(\frac{\arg(S_{21})}{l\omega}\right)^2 - 2}{1+\left(1+\frac{12h}{w}\right)^{-\frac{1}{2}} - \frac{\frac{t}{h}}{2.3\sqrt{\frac{w}{h}}}} + 1 & \frac{w}{h} > 1 \end{cases}. \tag{8}$$

A microstrip test coupon designed with FR4 as a substrate is shown in Fig. 2. There is no solder mask over the microstrip. Four microstrips traces on the PCB have different lengths. The SMA connectors are attached to the backside of the PCB.

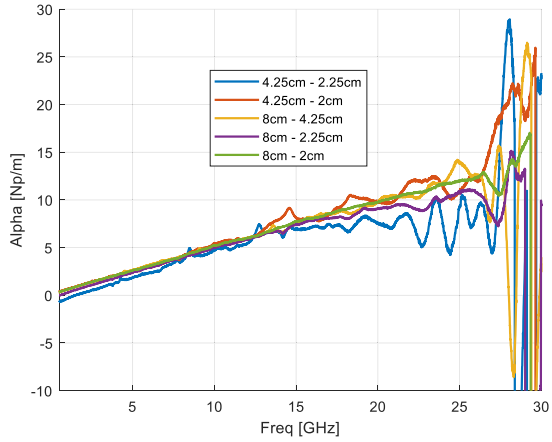

Fig. 3. Measured attenuation factor.

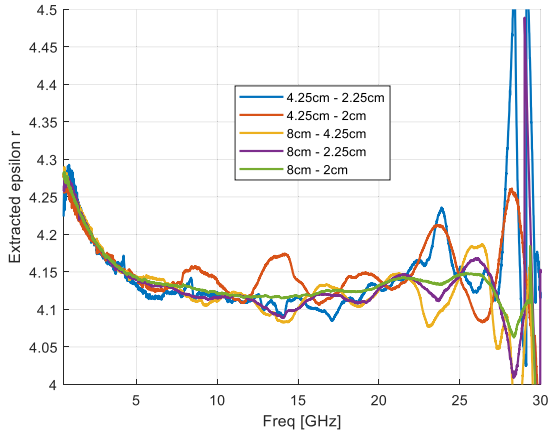

Fig. 4. Extracted permittivity of the test coupon substrate.

To obtain the S-parameter, the transmission coefficients of the microstrips are measured with a VNA. The following five pairs are created for de-embedding by the 2X-Thru SFD method [13].

1) Total: 4.25 cm; Thru: 2.25 cm.
2) Total: 4.25 cm; Thru: 2 cm.
3) Total: 8 cm; Thru: 4.25 cm.
4) Total: 8 cm; Thru: 2.25 cm.
5) Total: 8 cm; Thru: 2 cm.

The attenuation factor for all five pairs calculated from the de-embedded s-parameters as (2) is shown in Fig. 3. The differences between the curves are due to the de-embedding errors because of the nonidentical coaxial-to-microstrip transitions of the lines in the pairs (the reasons are mainly manufacturing and connector tolerances).

As demonstrated in [18], selecting standards with the largest length difference allows for reducing the de-embedding error. As can be seen in Fig. 3, the green line which corresponds to the pair with the largest length differences (Total: 8 cm; Thru: 2 cm) is the smoothest one and is expected to provide more accurate extraction results up to 20 GHz. The extracted permittivity for different combinations is shown in Fig. 4 and has similar values. The difference between the results is mostly due to the de-embedding errors. At the same time, as can be

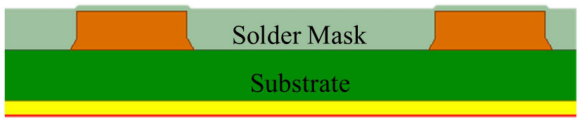

Fig. 5. Cross-sectional geometry of microstrip with solder mask.

seen, the green line (Total: 8 cm, Thru: 2 cm) is the smoothest of all five as expected.

B. Inhomogeneous Model Extraction

1) Extraction Algorithm: In the fabrication of the microstrip in PCB, the solder mask is a crucial layer to protect the traces against corrosion and oxidation. A simplified structure of the microstrip in fabricated PCB is shown in Fig. 5. For the insertion loss modeling, the dielectric layer of the microstrip can be considered a homogeneous layer with the equivalent primitivity. However, due to the that the solder mask will affect the FEXT level of the microstrip, the homogeneous model cannot describe the FEXT caused by the material inhomogeneity between the solder mask and the substrate. To better model the microstrip in PCB, the extraction for the permittivity of both the solder mask and the substrate layer is essential.

FEXT noise is caused by the coupling between transmitting lines when the signal propagates from the transmit end to the receiving end. The modal analysis for the FEXT [8] separates the aggressor signal into even and odd modes that propagate through the coupled pair with different velocities

$$V_{\text{fext}}(t) = V_{\text{even}}(t) + V_{\text{odd}}(t). \tag{9}$$

The odd and even phase velocities ($v_{p,\text{odd}}$, $v_{p,\text{even}}$) can be expressed using the PUL modal inductance (L_m) and capacitance (C_m)

$$v_{p,m} = \frac{1}{\sqrt{L_m C_m}} \tag{10}$$

where m represents the even or odd mode. The FEXT is generated during the time interval between the arrival of the odd-mode signal and the arrival of the even-mode signal [8, eq. (3)] as:

$$V_{\text{fext}} = \frac{V_1 l}{2t_r}\left(\frac{1}{v_{p,\text{odd}}} - \frac{1}{v_{p,\text{even}}}\right) \tag{11}$$

where V_1 is the magnitude of the aggressor signal with the rise time of t_r. To describe the difference between different modes, the FEXT is expressed with variable Δ_{LC} as (11), which is the dominant contributor compared to the parameters with lower-order terms

$$V_{\text{fext}} = \frac{V_1 l}{2t_r\left(\sqrt{L_{\text{odd}}C_{\text{odd}}} + \sqrt{L_{\text{even}}C_{\text{even}}}\right)}\Delta_{LC}. \tag{12}$$

Δ_{LC} is defined in [9] as

$$\Delta_{LC} = L_{\text{odd}}\,C_{\text{odd}} - L_{\text{even}}\,C_{\text{even}} = 2\left(L_{11}\,|C_{21}| - C_{11}L_{21}\right). \tag{13}$$

To separate the contribution of solder mask and substrate layers to the Δ_{LC}, the capacitance is decomposed according to [19]. Based on the decomposition of a simplified model in [19],

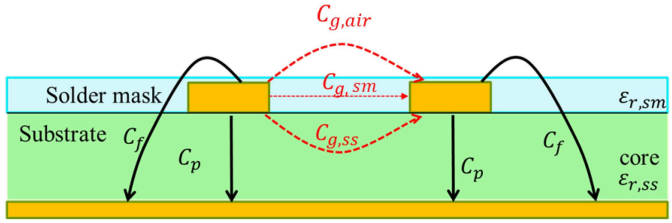

Fig. 6. Illustration of the capacitance components for the coupled microstrip pair.

TABLE II
DEFINITION OF THE DECOMPOSED CAPACITANCE

Capacitance	Definition
C_f	Fringe capacitance on the outer side of the trace, including the top, side, and bottom of the trace, is contributed by the air ($C_{f,air}$), solder mask ($C_{f,sm}$), and substrate ($C_{f,ss}$) regions.
C_p	Parallel plate capacitance of the trace, contributed by the substrate region.
C_g	Mutual capacitance across the gap, contributed by the air ($C_{g,air}$), solder mask ($C_{g,sm}$), and substrate ($C_{g,ss}$) regions.

the capacitance of the structure with three dielectric layers (air, solder mask, and substrate) is decomposed as is shown in Fig. 6. The four categories of the PUL capacitances in the three-layer model are explained in Table II.

The mutual capacitance across the gap $C_g$can be expressed as

$$\begin{aligned} C_g &= C_{g,air} + C_{g,sm} + C_{g,ss} \\ &= C_{g,air} + \varepsilon_{r,sm}C^a_{g,sm} + \varepsilon_{r,ss}\,C^a_{g,ss}. \end{aligned} \tag{14}$$

This capacitance is expressed by the product of the capacitances in the air-filled structure (denoted by the superscript "a") and the permittivity of the dielectric material [16].

The self-capacitance in the nodal capacitance matrix can be expressed as

$$\begin{aligned} C_{11} = C^a_{f,\text{air}} + \varepsilon_{r,sm}\cdot C^a_{f,sm} + \varepsilon_{r,ss}\cdot C^a_{f,ss} + \varepsilon_{r,ss}\cdot C^a_p \\ + C_g. \end{aligned} \tag{15}$$

The mutual capacitance in the nodal capacitance matrix

$$|C_{21}| = C_g = C_{g,air} + \varepsilon_{r,sm}C^a_{g,sm} + \varepsilon_{r,ss}\,C^a_{g,ss}. \tag{16}$$

According to [18, eq. (14)], the self-inductance and mutual inductance can be estimated using capacitances of the air-filled line as

$$\begin{aligned} L_{11}\left[\frac{\text{nH}}{\text{cm}}\right] &\approx \frac{10C^a_{11}}{9\Delta C^a} \\ &= \frac{10\left(C^a_{f,\text{air}} + C^a_{f,sm} + C^a_{f,ss} + C^a_p + C_g\right)[\text{pF/cm}]}{9\Delta C^a\left[(\text{pF/cm})^2\right]} \end{aligned} \tag{17}$$

$$L_{21}\left[\frac{\text{nH}}{\text{cm}}\right] \approx \frac{10\,|C^a_{21}|}{9\Delta C^a} = \frac{10\left(C^a_{g,pg}+C^a_{g,co}+C^a_{g,sm}\right)[\text{pF/cm}]}{9\Delta C^a\left[(\text{pF/cm})^2\right]} \quad (18)$$

where $\Delta C^a = (C^a_{11})^2 - (C^a_{21})^2$. Then, Δ_{LC} as defined by (13) and using the L and C given by (14)–(18) is expressed as

$$\begin{aligned}\Delta_{LC} &= C_{11}\,L_{21} - L_{11}\,|C_{21}| \\ &\frac{10}{9\Delta C^a}\cdot[(\varepsilon_{r,sm}-1)\left(C_{g,\text{air}}\cdot C^a_{f,sm} - C^a_{g,ss}\cdot C_{f,\text{air}}\right. \\ &+\ C^a_{g,ss}C^a_{f,sm} - C^a_{g,sm}C^a_{f,ss} - C^a_{g,sm}C^a_{p,ss}\left.\right) \\ &(\varepsilon_{r,ss}-1)\left(C_{g,\text{air}}\cdot C^a_{f,ss} - C^a_{g,sm}\cdot C_{f,\text{air}} + C_{g,\text{air}}\cdot C^a_{p,ss}\right. \\ &-\ C^a_{g,ss}C^a_{f,sm} + C^a_{g,sm}C^a_{f,ss} + C^a_{g,sm}C^a_{p,ss}\left.\right)] \\ &= k_1\,\varepsilon_{r,sm} + k_2\varepsilon_{r,ss} + b. \end{aligned} \quad (19)$$

The coefficients k_1, k_2, and b are related to the air-filled structure, which can be determined by solving three simulation cases with a fixed structure to achieve the three unknowns. Then, the FEXT peak value in (12) can be expressed as a function of $\varepsilon_{r,sm}$ and $\varepsilon_{r,ss}$

$$V_{\text{FEXT}} = K_{\text{FEXT}}\,\Delta_{LC} \sim k_1\varepsilon_{r,sm} + k_2\varepsilon_{r,ss} + b \quad (20)$$

where $K_{\text{FEXT}} = \frac{V_1}{2t_r(\sqrt{L_{\text{odd}}C_{\text{odd}}}+\sqrt{L_{\text{even}}C_{\text{even}}})}$.

The effect of dielectric changes on K_{FEXT} is assumed to be minor compared to that on Δ_{LC}. Since the FEXT level of the modeled microstrip is achieved by the 2-D solver, the error caused by the assumption can be compensated in the extraction procedure.

For a microstrip, the capacitances in the prepreg and core are in parallel [19]

$$C_{dd} = C_{dd,\text{air}} + C_{dd,sm} + C_{dd,ss}. \quad (21)$$

Thus, β_{dd} should have a strong sensitivity to the sum of $\varepsilon_{r,sm}$ and $\varepsilon_{r,ss}$, since $C_{dd,ss}$ and $C_{dd,sm}$ in (5) are scaled by $\varepsilon_{r,ss}$ and $\varepsilon_{r,sm}$. Then, β_{dd} is expressed as

$$\beta_{dd} = f(\varepsilon_{r,ss}, \varepsilon_{r,sm}). \quad (22)$$

To extract the inhomogeneous dielectric permittivity ($\varepsilon_{r,pg}$, $\varepsilon_{r,co}$), a target function (T) is defined as

$$T = \sqrt{(v'_{\text{Fext}} - v_{\text{FEXT0}})^2 + \text{weight}\left[\left(\frac{\beta'_{dd}}{\omega} - \frac{\beta_{dd0}}{\omega}\right)\right]^2} \quad (23)$$

where v'_{FEXT} and β'_{dd} are the FEXT peak value in the time domain waveform and phase of the modeled result. The parameter weight is introduced to make $(\beta'_{dd}/\omega - \beta_{dd0}/\omega)$ and $(v'_{\text{FEXT}} - v_{\text{FEXT0}})d$ have a comparable impact to the target function (T). Normally, the PUL inductance of the microstrip is in the order 100 nH and the PUL capacitance is in the order of pF, $(\beta'_{dd}/\omega - \beta_{dd0}/\omega)$ is in the order of $1e^{-16}$ according to (5). As a result, the value of the weight is assigned as $1e^{16}$.

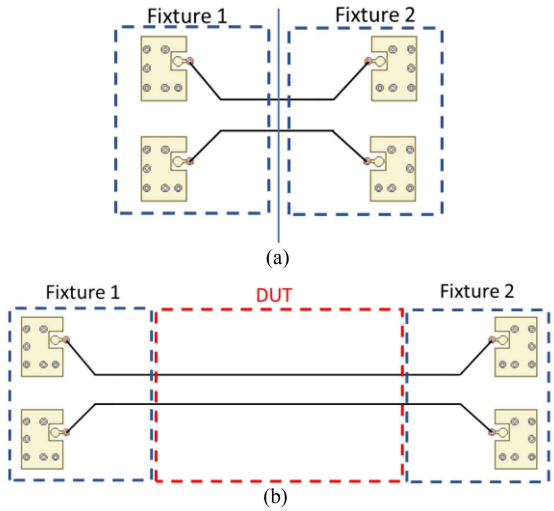

Fig. 7. Illustration of a Delta-L structure. (a) Thru. (b) Total.

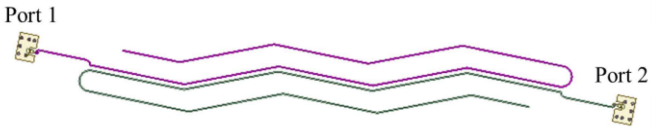

Fig. 8. Illustration of striplines with EUL structures.

2) Application on Test Coupon: To investigate the FEXT and insertion loss of the PCB, boards with multiple striplines with EUL structure and Delta-L lines are fabricated. The test coupon used in the measurement is designed with Delta-L and EUL structures.

The Delta-L structures are differential striplines with different lengths, as shown in Fig. 7. The "Thru" is with a shorter length, and the "Total" is with a longer length. The unwanted fixtures are composed of connectors, pads, vias, and transition sections. After 2X-thru de-embedding [13], the S-parameters of the "device under test" (DUT) is obtained.

The microstrip with EUL structures is illustrated in Fig. 8. The DUT is a pair of coupled striplines, and the striplines are intentionally extended. The extended parts are unterminated (open) without any coupling to the other pair. With a matched long transmission line termination, the impact from FEXT due to mismatched terminals can be excluded in the time domain [8]. The measurement is performed with differential microprobes (D-probes) [20]. Compared to the traditional measurement methods based on SMA connectors, more efficient tests can be performed with smaller landing spaces for high-volume PCB manufacturing validation.

The S-parameters measurement is performed using Keysight N5244A 4-port Network Analyzer. Using the measured S-parameters, with the amplitude and rise time of the incident step signal on the aggressor line set to +1 V and 50 ps, the FEXT waveform was calculated by Keysight ADS [21], as shown in Fig. 9.

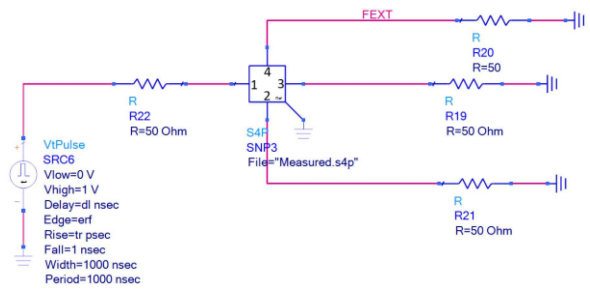

Fig. 9. Schematic for FEXT calculation in ADS.

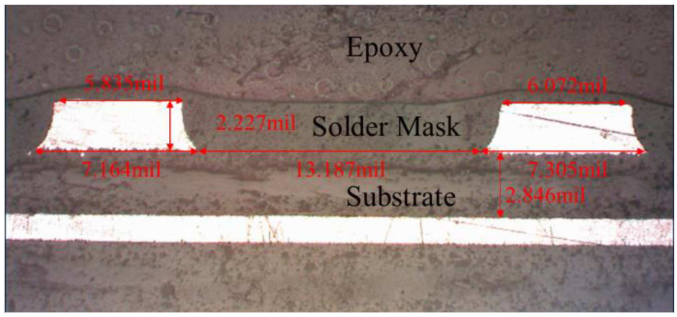

Fig. 10. Cross-sectional geometry information for the microstrip. The epoxy is filled above the sample for fixation in the polishing procedure.

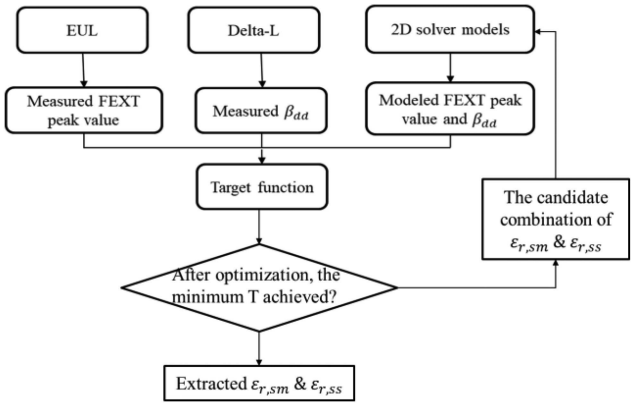

Fig. 11. Flow chart of the proposed $\varepsilon_{r,sm}$ and $\varepsilon_{r,ss}$ extraction method.

The entire extraction procedure is illustrated in the flow chart in Fig. 11. In the extraction procedure, the measurements result of Delta-L and EUL are acquired first from the traces on the same layer of the same board. As a result, the dielectric properties of the same layer are assumed to be the same. The EUL S-parameters provide the measured FEXT level and the Delta-L S-parameters after de-embedding, provide β_{dd}. With the cross-section geometry, the simulation models of both EUL and Delta-L structures are created by a 2-D solver. Intel IMLC [22] (a 2-D field solver) is the tool used to model the EUL and Delta-L lines.

After the S-parameters are measured, the samples of the traces are cut out from a fabricated PCB and encapsulated in an epoxy-based compound. Then the cross-section of the copper layer of interest is polished so that the profile perpendicular to the plane of view can be achieved. Fig. 10 shows an example of the cross-sectional geometry for the microstrip case with solder mask and substrate layers. The epoxy is filled above the sample for fixation in the polishing procedure. The extraction procedure

TABLE III
PERMITTIVITY OF SOLDER MASK AND SUBSTRATE LAYERS AT 1 GHZ

	DK nominal	DK extracted
Solder mask	4.25	4.0
Substrate	3.6	3.3

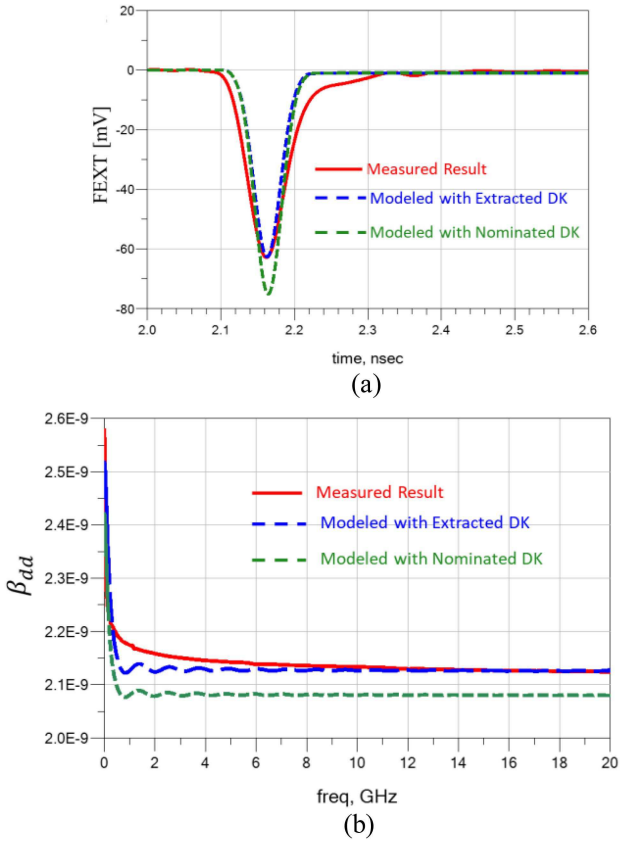

Fig. 12. Comparison between the measured and modeled (a) FEXT and (b) β_{dd}.

is shown in Fig. 11. The initial value of the combination of $\varepsilon_{r,ss}$ and $\varepsilon_{r,sm}$ is set based on datasheets from the vendor. Then the gradient descent is applied as the optimization with 0.1 sweeping steps. After the iterations, the value is optimized and the $\varepsilon_{r,ss}$ and $\varepsilon_{r,sm}$ are updated as the final extracted results.

Table III lists the nominal permittivity value provided by the PCB vendor and the extracted values. Fig. 12 demonstrates the comparison between the measured, the modeled result with the extracted value, and the modeled result with the nominal value. The extracted model result matches the measured result well and improves the accuracy of the nominal model.

III. SURFACE ROUGHNESS EXTRACTION

For the Delta-L structure, after de-embedding, the α_{dd}, which is the real part of the differential propagation constant that can be calculated from the measured S-parameters. Information about the dielectric loss is contained in the PUL conductance G [23]. Then, the other differential parameters are determined from the previous sections as

$$\alpha_{dd} = \frac{-\ln\left[|S_{dd21}|\right]}{l} \tag{24}$$

Fig. 13. Cross-sectional geometry for the microstrip.

where l is the length of the transmission line after de-embedding.

$$\alpha_{dd} = \frac{1}{2}\left(R_{dd}\sqrt{\frac{C_{dd}}{L_{dd}}} + G_{dd}\sqrt{\frac{L_{dd}}{C_{dd}}}\right). \tag{25}$$

To model the total insertion loss of the microstrip, conductor loss caused by the surface roughness needs to be extracted accurately [24]. Various approaches have been proposed to calculate the frequency-dependent surface roughness correction factor using the cross-sectional profile [25], [26] or the root-mean-square (rms) roughness levels [27]. The surface roughness correction factor (K) can be expressed with the PUL resistance as

$$K = \frac{R_{dd\text{rough}}}{R_{dd\text{smooth}}}. \tag{26}$$

The surface of the microstrip does not have the same roughness level for each edge. As is shown in Fig. 13, the bottom edge of the trace is much rougher than the upper edge of the trace and the top side of the reference plane beneath the trace. It is no longer accurate if one considers all the surface roughness to be at the same level [27]. As the result, the edges of the microstrip should be assigned with different roughness to ensure the accuracy of the model.

After achieving the SEM picture of the traces, the contrast of the image is optimized so that the roughness profile can be extracted. The procedure is shown in Fig. 14. Then, the rms value of the surface can be calculated for each zoomed-in area. The rms surface roughness level of the lower edge is extracted as 0.6 μm in the rms value. The other surface is assumed to be smooth. The conductor edges in the model created in Q2D with the geometry is assigned different roughness level. In Q2D, the roughness level is added as the finite conductivity boundary of the Hammerstad model. Fig. 15 shows the resistance solved from the simulation. The equivalent correction factor is calculated by (26), shown in Fig. 16.

IV. Dielectric Dissipation Factor Extraction

Then by solving the equation for each frequency point in (27), the dielectric loss tangent can be achieved. The loss tangent can only affect the insertion loss. As a result, the effective value can represent the performance of the two dielectric layers. Table IV shows the extraction result of the example in

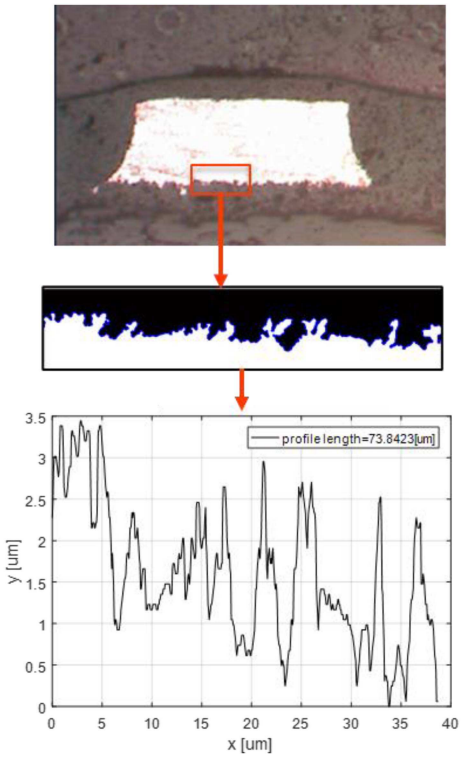

Fig. 14. Roughness level extraction for one area. The contrast of the cross-section image is optimized for each area. Then, the profile of the surface roughness is extracted, and the rms value is calculated for all the areas along the surface.

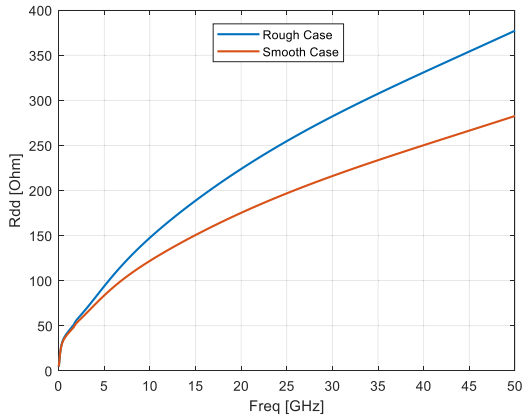

Fig. 15. PUL resistance of the rough and smooth cases, solved by the Q2D microstrip model.

Fig. 10. The extracted value is between the nominal tangent delta of the solder mask and substrate layers as expected. Fig. 17 demonstrates the attenuation factor comparison between the measured result and the modeled result with the extracted value. The error is introduced from the S-parameter measurement by the instrument, PUL parameters calculation by the 2-D solver, and the manufacturing variations of the fixture which affects the de-embedding procedure to obtain attenuation factors [14]. Besides, the sensitivity of the surface roughness in (26) is shown in Table V.

$$G_{dd} = \omega \cdot C_{dd} \cdot \tan\delta. \tag{27}$$

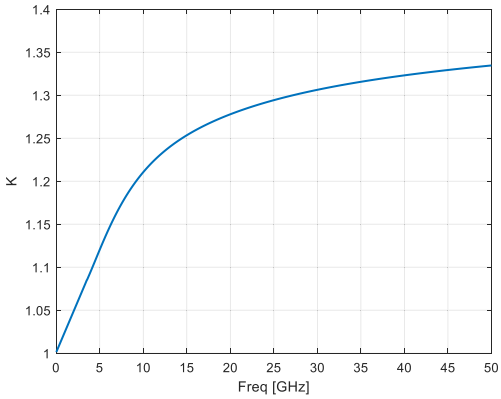

Fig. 16. Correction factor of the surface roughness calculated from the Q2D microstrip model.

TABLE IV
TANGENT DELTA OF SOLDER MASK AND SUBSTRATE LAYERS AT 1 GHZ

	Tangent delta Nominal	Tangent delta Extracted
Solder mask	0.0267	0.0170
Substrate	0.004	

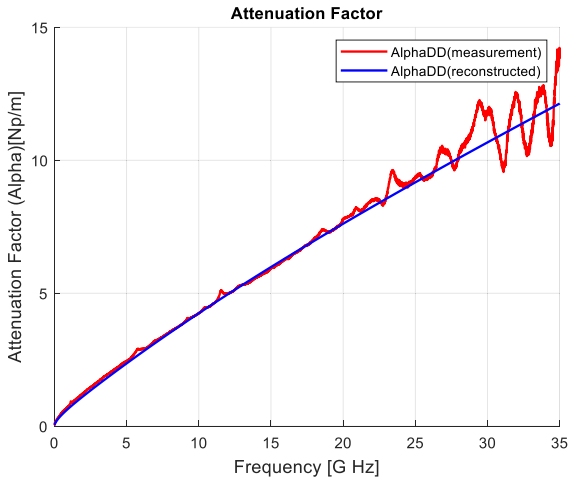

Fig. 17. Comparison between the measured and modeled attenuation factor.

TABLE V
TANGENT DELTA SENSITIVITY TO THE SURFACE ROUGHNESS

DF without roughness error	DF with 5% error in K	DF with 10% error in K
0.0170	0.0174	0.0178

V. DESIGN GUIDELINE

In practice, to improve the signal integrity performance in high-speed systems, FEXT mitigation is always a key design factor. As the frequency of the system gets higher, the difference of the phase velocity increases, which in turn results in higher FEXT. In the design procedure of the microstrip, the design guideline for the key design parameters is of great use. Using the extracted model and the analysis of the FEXT of the microstrip, some general design guidelines are established based on the

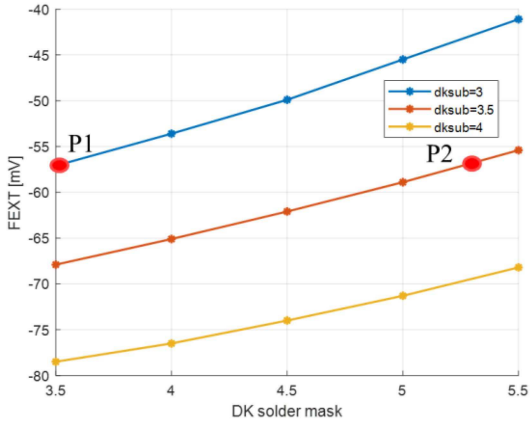

Fig. 18. Relationship between the dielectric constant and the FEXT.

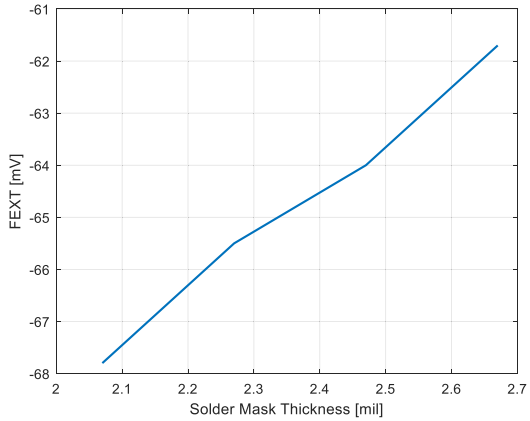

Fig. 19. Relationship between solder mask thickness and FEXT.

contribution of each parameter, which is validated by sweeping the parameters.

For the simplified microstrip model in Fig. 1, The FEXT of the simplified microstrip is mainly caused by the inhomogeneity between the dielectric layer and the air. To reduce the FEXT level, it is well known that we can either decrease the thickness of the substrate or decrease $\varepsilon_{r,ss}$.

For the microstrip model with both the solder mask and the substrate layers in Fig. 5, Fig. 18 shows the FEXT level with the geometry in Fig. 10 with different $\varepsilon_{r,sm}$ and $\varepsilon_{r,ss}$ from commercial 2-D field solver (Ansys Q2D) simulation. The higher the negative FEXT peak value shows, the better the design will be. The decrease of the $\varepsilon_{r,ss}$ and the increase of the $\varepsilon_{r,sm}$ help improve the FEXT result. To compensate for the FEXT caused by the change of $\varepsilon_{r,ss}$, $\varepsilon_{r,sm}$ needs larger change. For example, in Fig. 18, P1 and P2 share the same FEXT value. P1 represents the case that $\varepsilon_{r,sm}$ is 3.5 and $\varepsilon_{r,ss}$ is 3, while P2 represents the case that $\varepsilon_{r,sm}$ is 5.3 and $\varepsilon_{r,ss}$ is 3.5. The 0.5 increase of the $\varepsilon_{r,ss}$ needs 1.7 increase of the $\varepsilon_{r,sm}$ to compensate.

Besides, the increase of the solder mask thickness will help reduce the inhomogeneity between the substrate and the solder mask, and in turn helps immigrate the FEXT, validated by the simulation as is shown in Fig. 19.

In summary, to mitigate the FEXT of the practical microstrip model, one can:

1) Decrease $\varepsilon_{r,ss}$;
2) Increase $\varepsilon_{r,sm}$;
3) Increase the dielectric constant of the solder mask to compensate for the FEXT increasing due to the increased dielectric constant of the substrate;
4) Decrease the thickness of the substrate;
5) Increase the thickness of the solder mask;
6) Increase the number of solder masks to two or greater to reduce FEXT by increasing the thickness of the total solder mask.

VI. Conclusion

An empirical modeling approach to microstrip FEXT and insertion loss is proposed in this paper. Both the simplified model with one dielectric layer and the practical model with solder mask and substrate layers are studied. To model the FEXT and insertion loss, the relative permittivity (ε_r), dielectric dissipation factor (tanδ), and surface roughness are extracted and verified up to 20 GHz. With the extracted properties, the FEXT and insertion loss of the microstrip can be characterized more accurately, which can guide the PCB design and the material selection of the microstrip.

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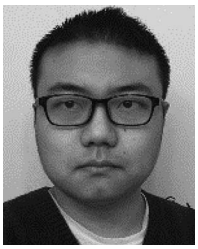

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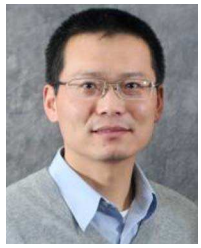

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