Prediction of Power Supply Induced Jitter With PDN Design Parameters

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***Abstract*—This article proposes a method to predict power supply induced jitter (PSIJ) at the inverter chain buffer output with the design parameters of power distribution network (PDN). The PDN is assumed to contain multiple decoupling capacitors with sufficiently different values for each branch. The relationship between PSIJ and PDN design parameters is derived analytically by convoluting the time-domain voltage ripple with the buffer time-domain PSIJ sensitivity, given the triangular noise current information. The analytical formula is validated through measurement by using an in-house designed CMOS buffer circuit and a controllable aggressor circuit based on 180 nm technology. The buffer output PSIJ under the operation of the aggressor circuit and the corresponding switching noise current are characterized. The *R–L–C* design parameters of PDN are extracted through impedance measurement. With the PDN parameters, the output jitter is calculated with the derived formulation. Compared with the measurements, the prediction error of the proposed method is within 8.1% when the voltage ripple amplitude is no larger than 10% of the supply voltage.**

***Index Terms*—CMOS buffer, jitter transfer relationship, measurement, power distribution network (PDN), power supply induced jitter (PSIJ), voltage ripple.**

I. Introduction

As THE operation speed of integrated circuits (ICs) continues to increase, and the consumed current reaches hundreds of amperes, the power distribution network (PDN) in real designs tends to lead to significant voltage decreases and voltage ripple on the power rail [1], [2], [3], [4], [5]. The fluctuation on the power rail can give rise to severe functionality issues, such as logic malfunction and timing jitter. As timing budgets continue to shrink, design becomes more challenging. Power supply induced jitter (PSIJ) is one of the most important concerns in high-speed system design.

PSIJ is best evaluated during the design stage. PDN is the most critical portion influencing the PSIJ because the existence of realistic PDN impedance is a root cause of power supply fluctuation. Many studies on PSIJ have focused on driver PSIJ sensitivity [6], [7], [8], [9], [10], a property of the circuit itself. In [6] and [7], the PSIJ sensitivity is analyzed on the basis of the piecewise transistor current–voltage relationship. Some researchers have proposed to model the inverter chain as a voltage-controlled delay line and derive the PSIJ sensitivity property [8]. In [9], the PSIJ sensitivity for a current-mode differential driver is studied with a numerical method, whereas in [10], a power supply rejection ratio response-based frequency-domain analysis is presented. Total system PSIJ has been described in many studies. A system-level model for PSIJ has been proposed in [11] in which a jitter tracking mechanism is included and validated for a DDR system. In [12], system PSIJ is analyzed by dividing the system into separate blocks for simulation and then combining the results analytically. However, in the above-mentioned work, the relationship between PDN and PSIJ performance is not specified. In [13] and [14], a target impedance with PSIJ as criteria is proposed; however, the influence of the phases of different frequency components is not considered, and the correlation of PDN parameters with PSIJ is not explicitly provided. In [13] and [15], an analytical expression is derived to link the time-domain total PSIJ with PDN parameters. However, the derivation is limited to the case in which the triangular switching current is dominant by one decoupling capacitor branch, and no measurement validation is reported.

In this work, a method to predict the inverter chain buffer output total PSIJ during the PDN design stage is proposed. The relationship between the PDN *R—L–C* parameters and buffer PSIJ is analytically deduced. The derived formulation can account for cases where a triangular switching current is drawn from either one or multiple decoupling capacitor branches, provided that the capacitance of each branch is sufficiently different. In common PDN designs, this criterion is usually satisfied [16]. With the obtained expression, given the PDN *R–L–C* parameters, the PSIJ of the inverter chain buffer attached to the PDN can be estimated. The analytical formulation correlating jitter and PDN design parameters can be further applied to develop PDN design guidelines using jitter as a criterion, which is helpful for effective design in consumer electronics. The proposed method is validated through measurements on an in-house designed chip. The inverter chain buffer PSIJ caused by triangular noise current is correctly evaluated with the PDN *R–L–C* parameters through the derived formulation.

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II. Relationship Between PSIJ and PDN Design Parameters

To predict the buffer total PSIJ with the PDN design parameters, the relationship between PSIJ and PDN *R–L–C* parameters is derived. The buffer PSIJ behavior is commonly described using PSIJ sensitivity, which is the ratio of output jitter when a single frequency supply noise is applied on the power rail to the amplitude of that noise. The PSIJ_sensitivity(*f*) is a linear relationship, assuming that the magnitude of the voltage ripple is small enough (usually within 10% of the nominal supply voltage) [5], [6], [7], [8], [9], [10]. The total PSIJ in the frequency domain can be written as

$$\text{PSIJ}(f) = \Delta v(f) \cdot \text{PSIJ\_sensitivity}(f) \tag{1}$$

where $\Delta v(f)$ is the supply voltage noise in the frequency domain, and PSIJ_sensitivity *(f)* is the buffer PSIJ sensitivity. The time-domain correspondence of PSIJ(*f*) is the continuously defined time interval error (CTIE), which is introduced to describe the time difference between the ideal and the actual edges at any arbitrary switching time [6]. The CTIE is expressed as the convolution of the time-domain voltage ripple $\Delta v(t)$ and the time-domain jitter transfer relationship PSIJ_sensitivity(t)

$$\begin{aligned}\text{CTIE\_PSIJ}(t) &= \Delta v(t) * \text{PSIJ\_sensitivity}(t) \\ &= \int \Delta v(\tau)\text{PSIJ\_sensitivity}(t-\tau)d\tau. \end{aligned} \tag{2}$$

The total time-domain jitter is then determined from the peak-to-peak value of the CTIE curve. Given the triangular IC switching noise current, the information on the relationship between supply voltage noise and PDN is embedded in the derivation of $\Delta v(t)$. The relationship between supply voltage noise and jitter is included in PSIJ_sensitivity(t). The jitter is linked with PDN parameters through the convolution process.

A. On-Die PDN Voltage Ripple Expressions

The time domain for on-die PDN voltage ripple is derived analytically, given proper assumptions regarding the PDN structure and IC switching noise current. The PDN can reasonably be described as a cascaded lumped element circuit [17], as shown in Fig. 1. The bulk decoupling capacitor, local decoupling capacitor, and on-die decoupling capacitor are used to decrease the PDN impedance in different frequency ranges. The series inductance and resistance on the decoupling capacitor branch mainly originate from the equivalent series inductance (ESL) and the equivalent series resistance (ESR) of the capacitor package. The other series inductance and resistance between the IC power net and decoupling capacitors come from the interconnects, such as bonding wires, PCB planes/traces, and vias. The VRM is the ultimate provider of the charge required by all switching events and can be modeled as an ideal voltage source in series with an inductor and a resistor.

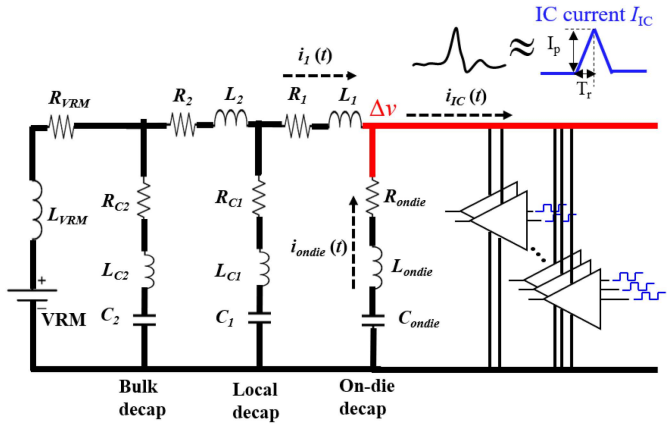

Fig. 1. PDN equivalent circuit and current distribution.

The transient IC switching noise current waveform can be approximated with a triangular pulse [16] as

$$i_{\text{IC}}(t) = \frac{I_p}{T_r}(tu(t) - 2(t-T_r)u(t-T_r) + (t-2T_r)u(t-2T_r)) \tag{3}$$

where I_p represents the triangular pulse peak value, T_r represents the pulse rise time, and $u(t)$ represents the step function. The triangular-shaped noise currents are very common in practical digital designs, such as the shoot-through currents [18], [19], [20].

With the IC switching noise current $i_{\text{IC}}(t)$ drawn from the on-die node of the buffer power pins, the VRM need to provide required charges for the switching events. The existence of PDN circuit will then lead to noise voltage $\Delta v(t)$ at the on-die node, as shown in Fig. 1. The rigorous expressions for $i_{\text{ondie}}(t)$, $i_1(t)$, and $\Delta v(t)$ are given as solutions of the sixth-order differential equation, which are very complicated and not suitable for practical application. Nonetheless, if the decoupling capacitor at the next downstream branches can be approximated as a short circuit, the analytical expression can be derived [16]. The short-circuit assumption indicates that the capacitor in the next downstream can be treated as a short and the voltage change across the next downstream capacitor is negligible. For example, when an IC noise current is drawn at the on-die power node, it is divided into $i_1(t)$ and $i_{\text{ondie}}(t)$. To analyze the divided two currents, the capacitor at the next downstream (C_1) is assumed to be a short. Consequently, C_2 can also be regarded as a short since bulk decap is designed to be larger than the local decap. The short-circuit assumption has little effect on currents $i_1(t)$ and $i_{\text{ondie}}(t)$, as long as the ratio of adjacent decoupling capacitors is sufficiently large (ten times larger). With this assumption, $i_1(t)$ and $i_{\text{ondie}}(t)$ resulting from $i_{\text{IC}}(t)$ can be calculated analytically from a second-order differential equation. The detailed validation has been provided in [16]. For common PDN designs, resonance frequencies introduced by multiple decoupling capacitors are sufficiently separated to maintain a low PDN impedance in a broad frequency range; therefore, the criterion for short-circuit approximation can be satisfied in general design [16], [17], [21].

According to the above assumptions, the currents $i_{\text{ondie}}(t)$ and $i_1(t)$ flowing into the IC power node, as indicated in Fig. 1, are analytically solved [16] as

$$i_{\text{ondie}} = \frac{I_p}{T_r}\frac{L_1'}{(L_{\text{ondie}}+L_1')}\frac{1}{\omega} \begin{pmatrix} \sin(\omega t)\, e^{-\alpha t}u(t) \\ -2\sin(\omega(t-T_r))\, e^{-\alpha(t-T_r)}u(t-T_r) \\ +\sin(\omega(t-2T_r))\, e^{-\alpha(t-2T_r)}u(t-2T_r) \end{pmatrix} \quad (4)$$

$$\begin{aligned} i_1 &= i_{\text{IC}} - i_{\text{ondie}} \\ &= \frac{I_p}{T_r}(tu(t)-2(t-T_r)u(t-T_r)+(t-2T_r)u(t-2T_r)) \\ &\quad - \frac{I_p}{T_r}\frac{L_1'}{(L_{\text{ondie}}+L_1')}\frac{1}{\omega} \begin{pmatrix} \sin(\omega t)\, e^{-\alpha t}u(t) \\ -2\sin(\omega(t-T_r))\, e^{-\alpha(t-T_r)}u(t-T_r) \\ +\sin(\omega(t-2T_r))\, e^{-\alpha(t-2T_r)}u(t-2T_r) \end{pmatrix} \end{aligned} \quad (5)$$

where ω denotes the angular frequency and is given as

$$\omega = \sqrt{1/\left(\left(L_{\text{ondie}}+L_1'\right)C_{\text{ondie}}\right)}. \quad (6)$$

α represents the attenuation constant and is expressed with

$$\alpha = (R_{\text{ondie}}+R_1')/(2\,(L_{\text{ondie}}+L_1')). \quad (7)$$

Here, $L_1{}' = L_1 + L_{C1} \parallel (L_2 + L_{C2} \parallel L_{\text{VRM}})$ and $R_1{}' = R_1 + R_{C1} \parallel (R_2 + R_{C2} \parallel R_{\text{VRM}})$. $L_1{}'$ and $R_1{}'$ are the PDN circuit equivalent inductance and resistance looking at the on-die power node to the VRM side, respectively.

The supply voltage fluctuation at the IC power node induced by the triangular switching currents is then calculated with

$$\Delta v = -R_{\text{ondie}}i_{\text{ondie}} - L_{\text{ondie}}\frac{di_{\text{ondie}}}{dt} - \frac{1}{C_{\text{ondie}}}\int i_{\text{ondie}}dt. \quad (8)$$

It is the voltage drop when the on-die current $i_{\text{ondie}}(t)$ goes through the on-die branch component C_{ondie}, R_{ondie}, and L_{ondie}. The on-die parasitic inductance can be neglected because of the very short length of the on-die metal power grid structure. The voltage ripple is derived as (9). With the on-die power node noise $\Delta v(t)$, the buffer jitter can then be derived using (2).

The first and second terms in (9) on the right side correspond to the noise components caused by R_{ondie} and C_{ondie}, respectively. It can also be observed that $\Delta v(t)$ will relate to ω, which is the resonance frequency determined by C_{ondie} and the sum of L_{ondie} and $L_1{}'$. $\Delta v(t)$ will also relate to α, which is determined by R_{ondie}, $R_1{}'$, L_{ondie}, and $L_1{}'$. In summary, the voltage ripple can be determined by the IC noise current and PDN *R–L–C* parameters.

$$\begin{aligned} \Delta v = &-\frac{I_p}{T_r}\frac{R_{\text{ondie}}L_1'}{(L_{\text{ondie}}+L_1')}\frac{1}{\omega} \begin{pmatrix} \sin(\omega t)\, e^{-\alpha t}u(t) \\ -2\sin(\omega(t-T_r))\, e^{-\alpha(t-T_r)}u(t-T_r) \\ +\sin(\omega(t-2T_r))\, e^{-\alpha(t-2T_r)}u(t-2T_r) \end{pmatrix} \\ &- \frac{1}{C_{\text{ondie}}}\frac{I_p}{T_r}\frac{L_1'}{(L_{\text{ondie}}+L_1')}\frac{1}{\omega} \begin{pmatrix} \frac{-e^{-\alpha t}(\alpha\sin(\omega t)+\omega\cos(\omega t))+\omega}{\omega^2+\alpha^2}u(t) \\ -2\frac{-e^{-\alpha(t-T_r)}\begin{pmatrix}\alpha\sin(\omega(t-T_r)) \\ +\omega\cos(\omega(t-T_r))\end{pmatrix}+\omega}{\omega^2+\alpha^2}u(t-T_r) \\ +\frac{-e^{-\alpha(t-2T_r)}\begin{pmatrix}\alpha\sin(\omega(t-2T_r)) \\ +\omega\cos(\omega(t-2T_r))\end{pmatrix}+\omega}{\omega^2+\alpha^2}u(t-2T_r) \end{pmatrix}. \end{aligned} \quad (9)$$

B. PSIJ Derivation

With (9), given the IC noise current information, the voltage ripple can be analytically calculated on the basis of the PDN design parameters. If the relationship between the time-domain jitter and supply voltage ripple is available, the jitter can be further associated with the PDN design parameters by using (2). The correlation of jitter and supply voltage noise is described by jitter sensitivity, as described Section II-A. The PSIJ sensitivity of the inverter chain buffers is used for derivation. They are commonly applied as clock delay lines and can be distributed in the entire design [22]. For an inverter type CMOS buffer, the PSIJ sensitivity is characterized by [8]

$$\text{PSIJ\_sensitivity}(f) = \frac{T_{p\max\text{DC}} - T_{p\min\text{DC}}}{\text{VDD}_{\max} - \text{VDD}_{\min}}\,\text{sin c}\,(\pi f T_{p0}) \quad (10)$$

where $T_{p\text{maxDC}}$ and $T_{p\text{minDC}}$ are the propagation delays of the buffer with minimum and maximum dc supply voltage $\text{VDD}_{\min}$ and $\text{VDD}_{\max}$. T_{p0} is the propagation delay with nominal dc supply voltage. The ratio $(T_{p\text{maxDC}} - T_{p\text{minDC}})/(\text{VDD}_{\max} - \text{VDD}_{\min})$ is the dc jitter sensitivity, which describes the propagation delay deviation due to the change in dc supply voltage.

The time-domain correspondence of a sinc function is a rectangular pulse [15]. Consequently, the relationship between the time-domain voltage noise and jitter transfer can be expressed as

$$\text{PSIJ\_sensitivity}(t) = \begin{cases} \frac{(T_{p\max\text{DC}} - T_{p\min\text{DC}})}{T_{p0}(\text{VDD}_{\max} - \text{VDD}_{\min})} & 0 \le t \le T_{p0} \\ 0 & \text{others.} \end{cases} \quad (11)$$

The width of PSIJ_sensitivity(t) pulse is the nominal propagation delay T_{p0}. The pulse height is the ratio of dc jitter sensitivity to the nominal propagation delay.

By convoluting the time-domain voltage ripple and the relationship between the time-domain voltage noise and jitter transfer, the CTIE curve can be calculated. The total time-domain jitter can then be extracted from the maximum and minimum values in the CTIE curve. The convolution process is illustrated in Fig. 2(a), using the resistive-voltage-noise-only case as an example. On the basis of the assumption that the decoupling capacitor of each branch is sufficiently large, and only parasitic resistance exists, the time-domain voltage ripple will be a triangular pulse. The rise time of the triangular voltage ripple will be the same as the triangular IC noise current [16]. Suppose that the propagation delay of the aggressor circuit is longer than that of

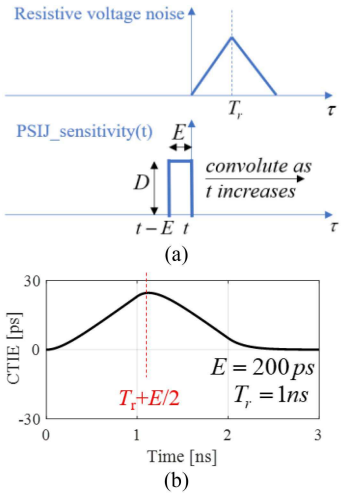

Fig. 2. Illustration of the convolution process. (a) Resistive noise convolution process. (b) Example of a calculated CTIE curve for resistive noise.

the victim circuit. T_r will be larger than the victim buffer propagation delay [18]. For simplicity of illustration, the height of the PSIJ_sensitivity*(t)* is denoted as D and is equal to $(T_{p\max\mathrm{DC}} - T_{p\min\mathrm{DC}})/((\mathrm{VDD}_{\max} - \mathrm{VDD}_{\min})T_{\mathrm{p0}})$, whereas the width is denoted as E and is equal to T_{p0}. For the situation, as shown in Fig. 2(a), the start time of the IC noise current is set to $t = 0$. The minimum CTIE is obtained when $t = 0$, as the overlap area of the voltage ripple and PSIJ_sensitivity*(t)* is zero. The maximum CTIE is obtained when $t = T_r{+}E/2$, as the overlap area of the voltage ripple and PSIJ_sensitivity*(t)* is largest. This finding can be validated from the analytical expression derived in [15]. In addition, from the CTIE curve calculated from the convolution of the triangular voltage ripple and PSIJ_sensitivity*(t)*, as depicted in Fig. 2(b), the CTIE minimum and maximum will occur at $t = 0$ and $t = T_r{+}E/2$, respectively.

In summary, the minimum CTIE can be expressed as

$$\mathrm{CTIE}_{\min} = D\int_{t_1-E}^{t_1} \Delta v dt \tag{12}$$

where t_1 is the time point allowing the integration in time range E to have the minimum value. The minimum value can either be zero or the maximum value with negative sign. In contrast, the maximum CTIE can be expressed as

$$\mathrm{CTIE}_{\max} = D\int_{t_2-E}^{t_2} \Delta v dt \tag{13}$$

where t_2 is the time point allowing the integration in time range E to have the maximum value. The total time-domain jitter can be calculated by using $\mathrm{CTIE}_{\max} - \mathrm{CTIE}_{\min}$.

For a more general case, the integration of the voltage ripple can be derived analytically, as in the following (14) shown at the bottom of the next page:

If the value of t_1 is determined, the minimum CTIE can be calculated by $\mathrm{DS}(t_1) - \mathrm{DS}(t_1 - E)$. If the value of t_2 is determined, the maximum CTIE can be calculated with $\mathrm{DS}(t_2) - \mathrm{DS}(t_2 - E)$. For simplicity, the time points t_1 and t_2 can be located by observing the predicted time-domain voltage ripple shape, as previously illustrated. This process is demonstrated for a more complicated case in Section III.

III. Measurement Validation

The proposed prediction method is validated through experiments. First, the test IC chip, including the aggressor and victim circuit, is designed. Second, on-die PDN characterization is performed to extract the equivalent PDN *R–L--C* parameters. Third, the aggressor switching noise current on the IC power node is characterized. Fourth, the PSIJ sensitivity of the victim driver is measured. Finally, the circuit total PSIJ with the aggressor operation is measured and compared with the predicted jitter calculated from the PSIJ-PDN formulation.

A. Test Vehicle Design

The functional design of the test IC is illustrated in Fig. 3. The aggressor circuit is called the current consuming circuit (CCC) and is composed of several design blocks. The aggressor is designed to generate controllable triangular current pulses on the power net of the victim driver to mimic the real design situation. The noise current is the shoot-through current of the last stage inverter in a CCC section. It is intentionally created by separating the input of the PMOS and NMOS, as illustrated in Fig. 4. The input of the PMOS comes from the inverted NAND calculation, whereas the input for NMOS comes from the inverted NOR calculation. The peak amplitude of the current introduced by the CCC can be controlled by 3-bit control pins A1–A3. The control pins determine how many CCC sections are turned ON. The victim driver is an eight-stage inverter chain. Since the inverter chain type buffers share the same kind of PSIJ sensitivity function, the number of stages will not affect the validation process. The circuit schematic of the victim buffer is depicted in Fig. 5. W and L indicate the width and length of the transistors, respectively. For the inverter chain, the multiplication factor M for each stage is continually increased by the same factor.

The layout of the in-house designed chip is shown in Fig. 6. The layout of the CCC and the victim inverter is labeled in the white rectangle. The on-die decap is achieved with NMOS; the gate terminal is connected to the power, and the source/drain terminals are connected to the ground. The on-die decap is designed to be 200 pF in total. The bonding pads on the periphery of the chip are 80 μm by 80 μm, with a 100 μm pitch. The test IC die is taped out with CMOS 180 nm technology and is wire bonded to a PCB test board. On the test board, the power plane for the aggressor circuit and the victim circuit are separated. The CCC control pins are designed to be controlled with an on-board switch. The decap pins are also designed for the placement of the bulk decoupling capacitors.

B. On-Die PDN Impedance Measurement and Model Extraction

To characterize the PDN impedance looking from the on-die power node, the measurement is performed, as shown in Fig. 7. A 100 μm pitch SG microprobe is located at a pair of power/ground pads for the victim circuit. The microprobe output is connected

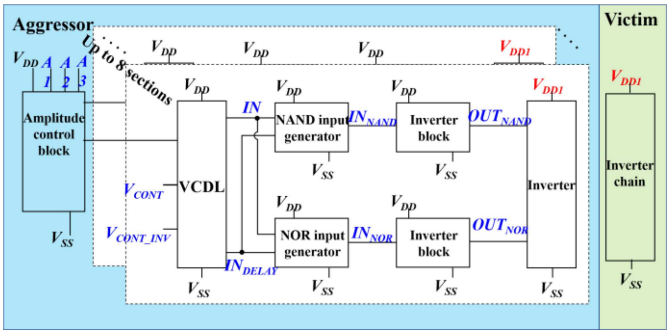

Fig. 3. Functional design of the test IC.

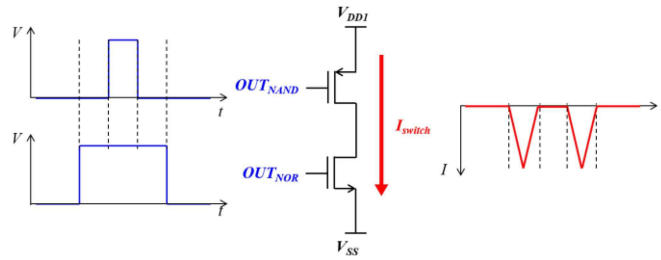

Fig. 4. Generation of a controllable triangular switching current.

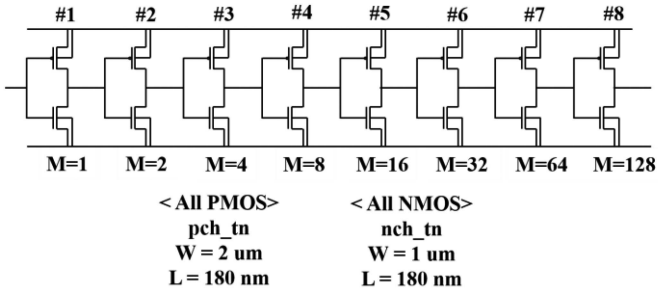

Fig. 5. Design parameters of the victim inverter chain.

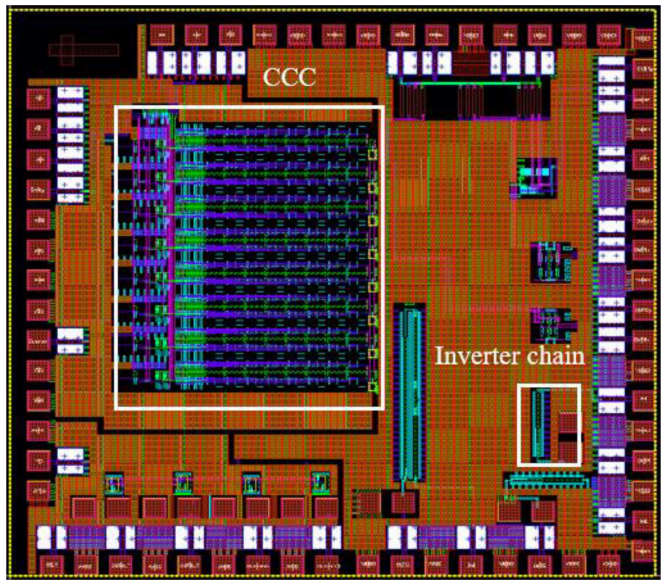

Fig. 6. Layout design of the test IC.

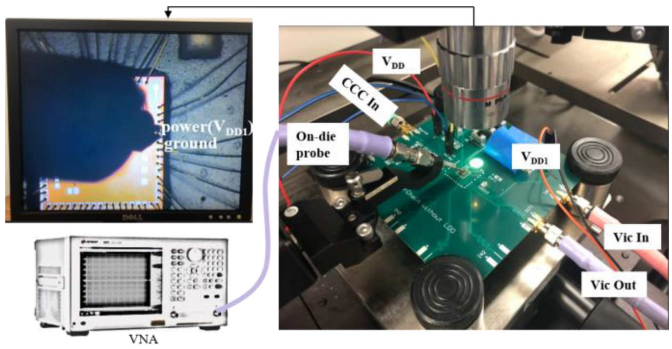

Fig. 7. Setup for impedance measurement using a vector network analyzer.

to a vector network analyzer. The on-die PDN impedance is obtained by transformation of the one-port S parameter to a Z parameter. The nominal power supply voltage is 1.8 V, and the input for the CCC and victim is kept to zero. On the basis of the on-die PDN impedance curve, the corresponding R–L–C parameters can be extracted. The extracted equivalent circuit model and all the values of the circuit elements are shown in Fig. 8. R_{ondie}, L_{ondie}, and C_{ondie} represent the equivalent resistance, inductance, and capacitance for the on-die portion. C_{ondie} is known from chip layout design value. R_1 and L_1 are the parasitic resistance and inductance due to the wire bond and PCB board. C_{plane} is the plane capacitance from the PCB and can be

$$S(t) = \int \Delta v dt = -\frac{I_p}{T_r}\frac{R_{\text{ondie}}L_1'}{(L_{\text{ondie}}+L_1')}\frac{1}{\omega}\begin{pmatrix}\frac{-e^{-\alpha t}(\alpha\sin(\omega t)+\omega\cos(\omega t))+\omega}{\omega^2+\alpha^2}u(t)\\ -2\frac{-e^{-\alpha(t-T_r)}(\alpha\sin(\omega(t-T_r))+\omega\cos(\omega(t-T_r)))+\omega}{\omega^2+\alpha^2}u(t-T_r)\\ +\frac{-e^{-\alpha(t-2T_r)}(\alpha\sin(\omega(t-2T_r))+\omega\cos(\omega(t-2T_r)))+\omega}{\omega^2+\alpha^2}u(t-2T_r)\end{pmatrix}$$

$$-\frac{1}{C_{\text{ondie}}}\frac{I_p}{T_r}\frac{L_1'}{(L_{\text{ondie}}+L_1')}\frac{1}{\omega}$$

$$\begin{pmatrix}\frac{-e^{-\alpha t}\left(\left(\omega^2-\alpha^2\right)\sin(\omega t)-2\alpha\omega\cos(\omega t)+\left(-\omega^3-\omega\alpha^2\right)te^{\alpha t}\right)-2\alpha\omega}{\left(\omega^2+\alpha^2\right)^2}u(t)\\ -2\frac{-e^{-\alpha(t-T_r)}\left(\left(\omega^2-\alpha^2\right)\sin(\omega(t-T_r))-2\alpha\omega\cos(\omega(t-T_r))+\left(-\omega^3-\omega\alpha^2\right)(t-T_r)e^{\alpha(t-T_r)}\right)-2\alpha\omega}{\left(\omega^2+\alpha^2\right)^2}u(t-T_r)\\ +\frac{-e^{-\alpha(t-2T_r)}\left(\left(\omega^2-\alpha^2\right)\sin(\omega(t-2T_r))-2\alpha\omega\cos(\omega(t-2T_r))+\left(-\omega^3-\omega\alpha^2\right)(t-2T_r)e^{\alpha(t-2T_r)}\right)-2\alpha\omega}{\left(\omega^2+\alpha^2\right)^2}u(t-2T_r)\end{pmatrix}. \quad (14)$$

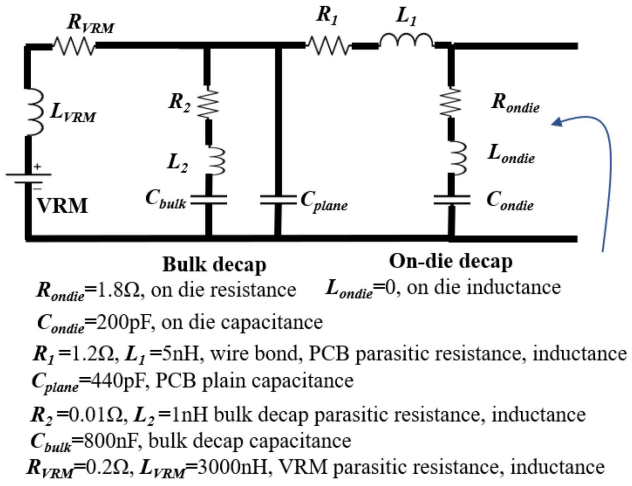

Fig. 8. Extracted equivalent circuit model for PDN.

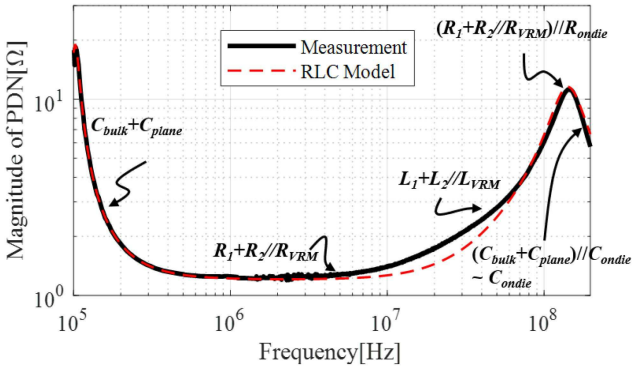

Fig. 9. PDN impedance of the test IC.

calculated based on PCB geometry. $C_{\rm bulk}$ is for the bulk decap. R_2 and L_2 are the ESR and ESL of the bulk decap. The bulk decap is 800 nF. For the dc VRM branch, $R_{\rm VRM}$ and $L_{\rm VRM}$ are the parasitic resistance and inductance. All the parasitic resistances and inductances are extracted by fitting the PDN impedance curve of the equivalent circuit to the measured PDN impedance.

The PDN impedance calculated from the extracted *R–L–C* circuit model is relatively close to the measurements, as depicted in Fig. 9. The PDN impedance is first dominated by the capacitance portion and is mainly from the $C_{\rm bulk}$ and $C_{\rm plane}$. Then, the PDN impedance is dominated by the resistive portion and is from R_1 in series with the equivalent resistance of the bulk decap branch and VRM branch. With the increase in frequency, the PDN impedance increases, and the inductive portion is from L_1 in series with equivalent inductance of the bulk decap branch and VRM branch. The antipeak value is determined by the on-die resistance in parallel with the equivalent resistance for the rest of the branches. Then, the PDN impedance is decreased by the on-die decap. The on-die decap is designed as 200 pF and can be used in the equivalent circuit model to match the measured PDN impedance. It should be noted that even though the measurement validation case has only peaks related to the on-die decap and bulk decap on PCB, it does not limit the application scenario

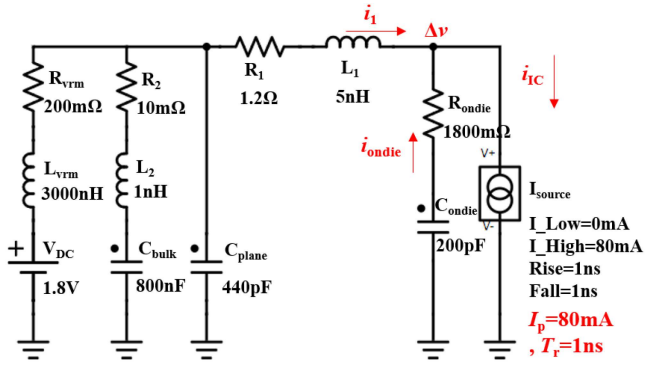

Fig. 10. Circuit simulation setup.

of the proposed method. As long as the PDN impedance peaks caused by different branches are sufficiently separated, which is the common case, this method can be applied.

C. IC Noise Current Characterization

After establishment of the PDN model and extraction of the related *R–L–C* parameters, the next step is obtaining the IC current peak and rise time value. In practice, for the IC designers, the current information should be easy to obtain as the SPICE models are usually available. For system designers, this information is usually provided by the IC vendors. In this work, instead of measuring the on-die IC current directly, the measured on-die power voltage and the extracted PDN model are used, and the rise time and peak value information of the IC switching current are obtained with (9), as the voltage measurement is more convenient and accurate in the present lab environment. This relationship between voltage ripple and the IC current and PDN parameters is validated with a circuit simulation, as shown in Fig. 10. For the extracted PDN circuit model, an ideal triangular current pulse is added. The peak value of the current is set to 80 mA, and the rise time of the current is set to 1 ns.

The comparison of the formulation calculation and the simulation results for the on-die current $i_{\rm ondie}(t)$, $i_1(t)$ current, and the on-die voltage ripple $\Delta v(t)$ are shown in Fig. 11. The formulation can capture most of the waveform characteristics. The ringing portion in all three waveforms is associated with the antipeak in the PDN network, as shown in Fig. 9. The results indicate that $i_1(t)$ and $i_{\rm ondie}(t)$ are comparable. Although the bulk decap is much larger than the on-die decap, the relatively large R_1 and L_1 will impede the current flow to the bulk decap branch. From the on-die voltage ripple $\Delta v(t)$, the time when the first voltage dip occurs is very close to the rise time of the IC current 1 ns. This is, in general, valid if the decap value for each branch is sufficiently large. The voltage ripple caused by the capacitor element can be neglected. For the resistive and inductive elements, when the triangular IC current passing through a resistive element, the shape of the voltage ripple will also be a triangular pulse and the voltage dip time be the rise time of the IC current. When the current is passing through an inductive element, the voltage noise will be constant during the rising or falling edge period of IC current, just with opposite values. The voltage dip time will

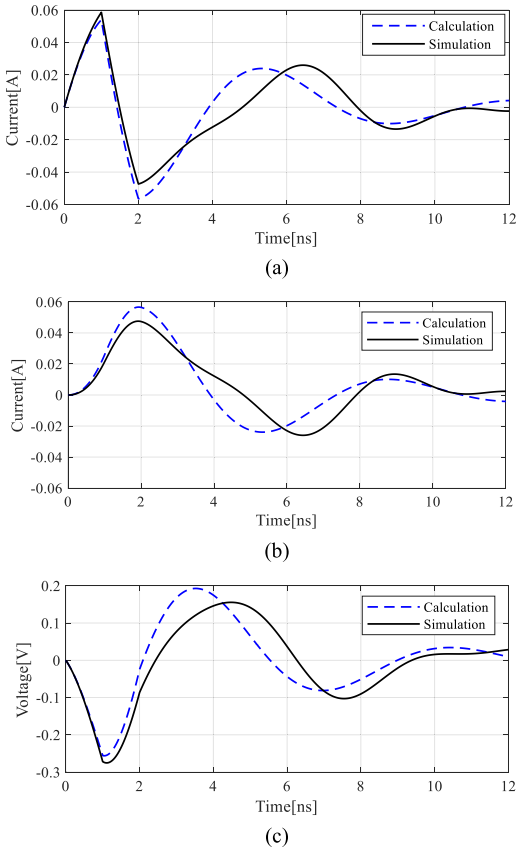

Fig. 11. Comparison of the derived formulation with simulation results. (a) $i_{\text{ondie}}(t)$. (b) $i_1(t)$. (c) $\Delta v(t)$.

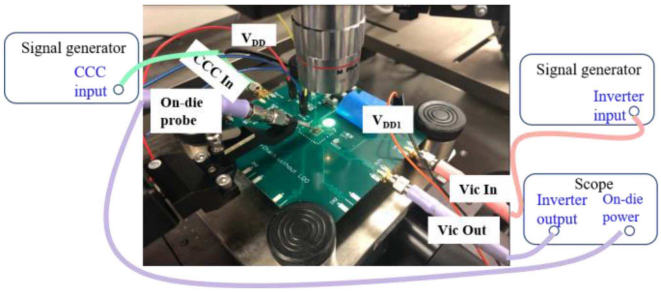

Fig. 12. Voltage ripple and total PSIJ measurement setup.

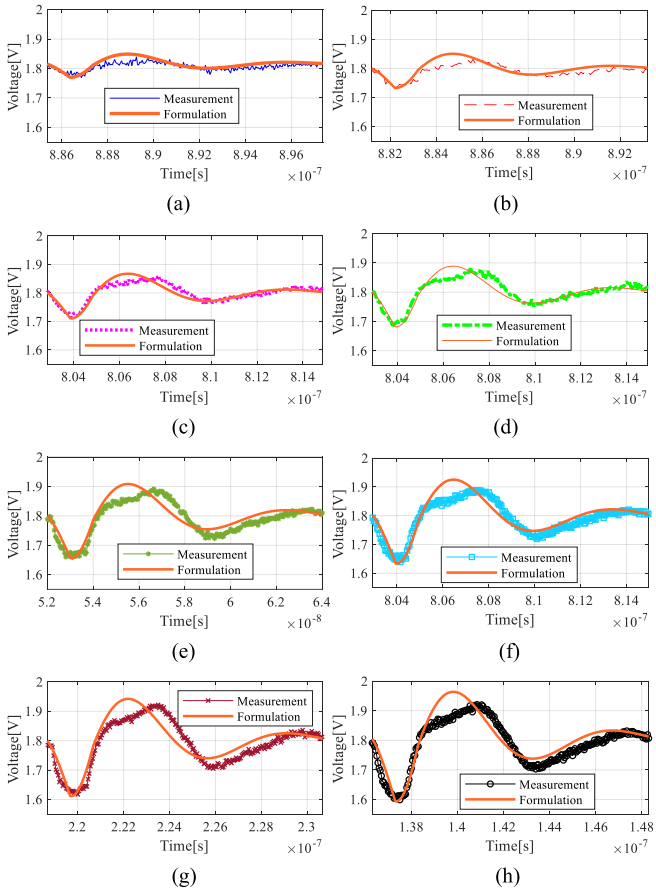

Fig. 13. Comparison of the derived formulation with measurement results for voltage ripple. A1A2A3 = (a) 000, (b) 001, (c) 010, (d) 011, (e) 100, (f) 101, (g) 110, and (h) 111.

also be the rise time of the IC current [15], [16]. In addition, the voltage value at this time point can be used to derive the peak current value with (9).

For the measurement test case, the 3-bit amplitude control of CCC is used, and there will be eight different cases. The measurement setup is shown in Fig. 12. The on-die voltage noise is measured with an oscilloscope with a micro SG probe. Given the low PDN impedance in the frequency range of interest, the 50 Ω probe would introduce little disturbance to the measurement data. The nominal supply voltage for the driver is 1.8 V. The inputs of the inverter chain and the CCC are square waves with frequency value of 19.23 and 5.9 MHz, respectively. For each input period of CCC, there will be two noise voltage pulses generated and the adjacent voltage ripples are separated. The frequency of victim driver and aggressor is set to be nonintegral multiples to avoid all the victim input rising edges seeing the same power supply waveform.

The on-die power voltage noise and the inverter chain output are measured simultaneously. The comparison of the measured maximum voltage ripple and the calculated voltage waveforms for the eight cases are shown in Fig. 13. The maximum voltage ripple is used to account for the maximum time variance of the switching edge. For the start point of each triangular pulse in the real measurement, it corresponds to the time 0 in Fig. 11. As a result, the start point of each $\Delta v(t)$ pulse in the real measurement also corresponds to the time 0 in Fig. 11. The formulation calculated waveforms are plotted in the solid curves. The formulation correlates with the measurement results with reasonably good accuracy. The formulation calculated curve can capture most of the measured waveform characteristics. With increasing control bit sequence value, the voltage ripple value concordantly increases. As described before, from the first dip of the voltage ripple and the time to reach the first voltage dip in the voltage ripple waveform, the IC current rise time and the peak value can be estimated. The extracted rise time and peak current value for each case are summarized in Table I.

TABLE I
EXTRACTED RISE TIME AND PEAK CURRENT

A1A2A3	Rise Time (ns)	Peak current I_p (mA)
000	1	14
001	1	21
010	1	28
011	1	37
100	1	45
101	1	52
110	1	59
111	1	66

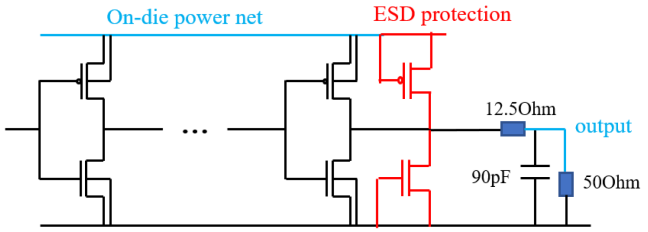

Fig. 14. Simulation setup for inverter chain PSIJ sensitivity analysis.

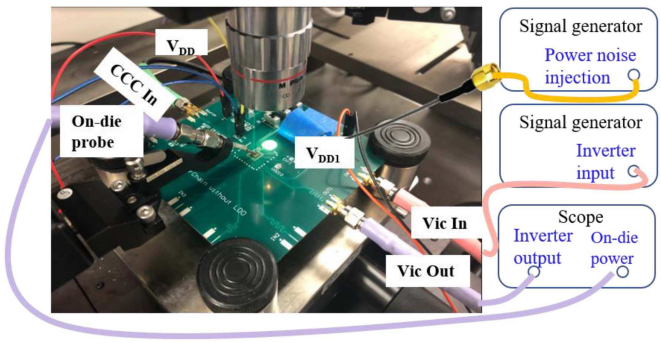

Fig. 15. Equivalent loading extraction measurement setup.

D. Victim Inverter Chain PSIJ Sensitivity Characterization

After the IC current information is obtained, the next step is to derive the victim driver PSIJ sensitivity. The equivalent loading resistance and capacitance of the inverter chain circuit need to be determined. The parasitic loads are originated from the on-die metal line, wire bond, and PCB trace connected to the driver output. With the parasitic loads, the jitter sensitivity of the inverter chain circuit is simulated using HSPICE. The equivalent simulation circuit is plotted in Fig. 14. The sinusoidal noise is added on the on-die power net, and the jitter for each frequency is evaluated at the output.

Ideally, the loading resistance and capacitance can be extracted directly from the impedance curve simulated at the driver output location looking to the loading side. However, in this case, the wire bond geometry information is not available, so the parasitic loads are determined from the comparison of measurement and simulation, as shown below.

The measurement setup for parasitic parameter extraction is shown in Fig. 15. A semirigid cable is soldered onto the

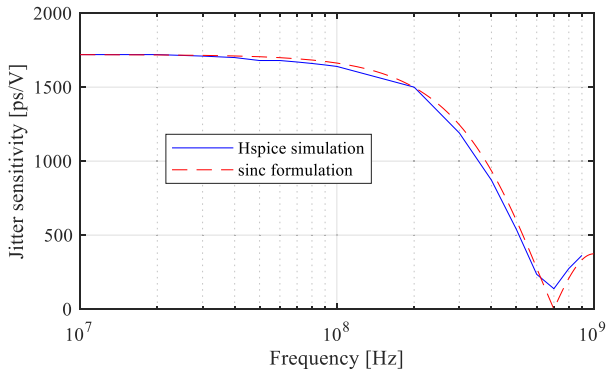

Fig. 16. Comparison of victim circuit jitter sensitivity from simulation and formulation.

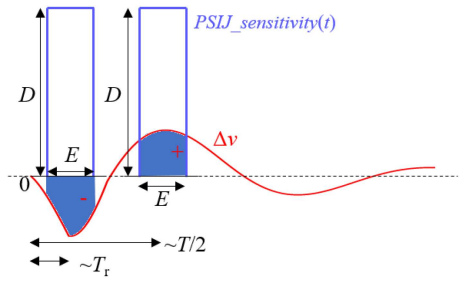

Fig. 17. Convolution process for finding the maximum and minimum CTIE value.

PCB power port for sinusoidal power rail noise injection. The microprobe is applied to measure the injected voltage noise at the on-die power node. All the PCB traces are designed to be 50 Ω and are connected out through SMA connectors. The dc operation voltage for the driver is 1.8 V. The input of the inverter chain is a square wave switching between 0 and 1.8 V. The output waveform of the inverter chain is measured through an SMA cable to an oscilloscope. The on-die power net voltage is measured simultaneously with the oscilloscope. The scope is set to 50 Ω input impedance.

At dc, with 1.8 V power and 50 Ω scope input impedance, the driver output voltage is measured as 1.2 V. On the basis of the circuit simulation, the equivalent loading resistance is determined as 12.5 Ω. In contrast, when a power rail is injected with 18 MHz power noise, the jitter sensitivity is measured as 1720 ps/V. From the circuit simulation, the equivalent loading capacitance is determined to be 90 pF because the simulated jitter sensitivity with this loading is closest to the measured value.

The simulated jitter sensitivity result is close to a sinc function, as shown in Fig. 16 . Since the period of the noise voltage is much larger than the propagation delay of the circuit in low-frequency ranges, the phase of the noise voltage does not change much and is approximately constant during the output transition. As a result, at low frequencies, the jitter behavior is almost the same as a dc offset of the supply voltage [6] and the sensitivity value will be constant at the low-frequency ranges. So, the dc jitter sensitivity can be determined from the simulated sensitivity curve at the low-frequency ranges. From the property of the

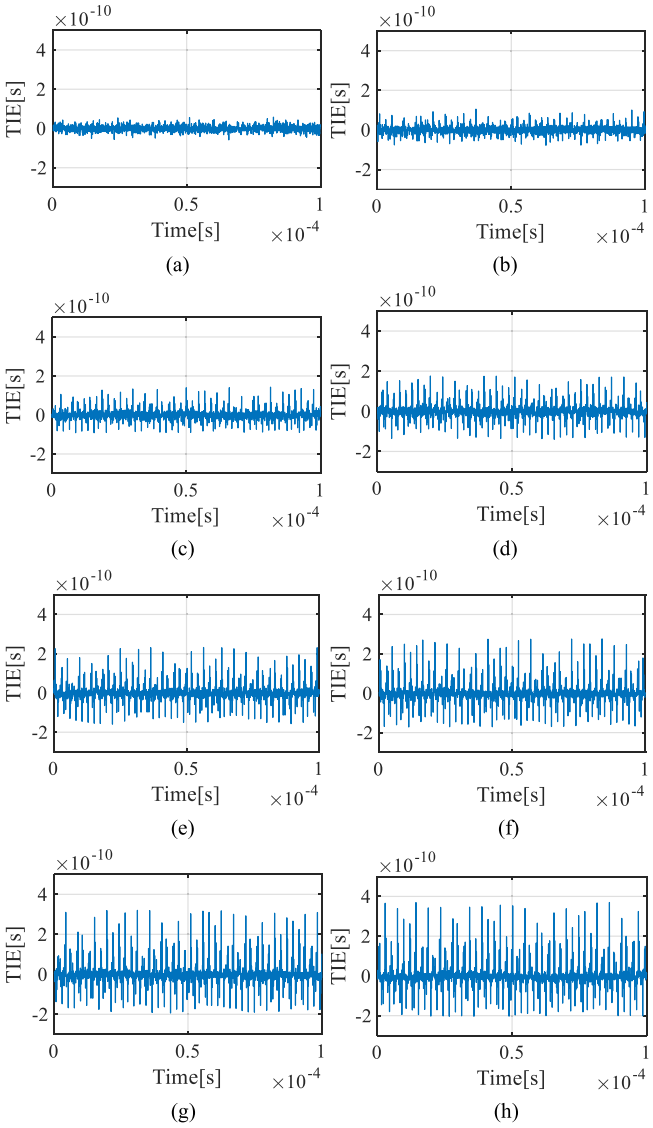

Fig. 18. Measured TIE results. A1A2A3 = (a) 000, (b) 001, (c) 010, (d) 011, (e) 100, (f) 101, (g) 110, and (h) 111.

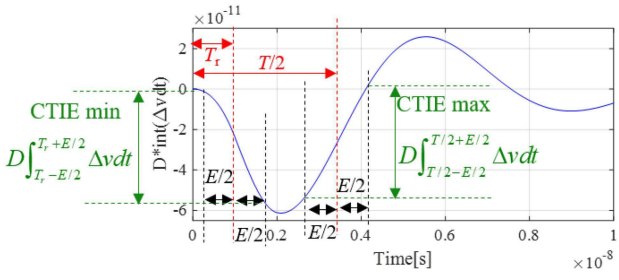

Fig. 19. Calculation results of $D\int \Delta v dt$ for A1A2A3 = 000.

sinc function, the first dip location corresponds to the frequency where $fT_{p0} = 1$. Hence, the propagation delay is the inverse of the frequency where the sinc function shows the first dip. Based on (10) and the simulated sensitivity curve, the dc jitter sensitivity is 1720 ps/V, and the propagation delay is determined to be 1.43 ns.

TABLE II
COMPARISON OF THE MEASURED AND CALCULATED TOTAL JITTER

A1A2A3	Peak-peak value of measured TIE sequence(ps)	Peak-peak value of calculated CTIE sequence (ps)	Error (%)
000	111.5	108.6	2.6
001	170	162.0	4.7
010	227	217.5	3.5
011	300	286.9	4.4
100	380	349.0	8.1
101	435	403.3	7.3
110	505	458.0	9.3
111	570	511.5	10.3

E. Comparison of Calculated Total PSIJ With Measured Values

With the information on PDN *R–L--C*, IC current, and driver PSIJ sensitivity, the total PSIJ when an aggressor circuit is operating can be derived. As previously shown, the CTIE is calculated as the convolution of the on-die voltage ripple and the time-domain PSIJ transfer relationship. The width of this time-domain PSIJ transfer relationship is the propagation delay and is denoted as E. In contrast, the height of the rectangular pulse is the ratio of dc jitter sensitivity to the propagation delay and is denoted as D.

The convolution process for this test case is illustrated in Fig. 17. Because jitter is the difference between the maximum and minimum CTIE value, only the time point when the minimum and maximum occurs must be found. Because D is a constant, this process is equivalent to finding the minimum and maximum values of the voltage ripple integration in the time range of the propagation delay E, as discussed in Section II-B. In this case, the minimum occurs when the integration is performed between $T_r-E/2$ and $T_r+E/2$. Correspondingly, t_1 in (12) is determined as $T_r+E/2$. For the maximum integration value, it can be assumed to occur near $T/2$. In this case, T is the period of the ringing corresponding to the antipeak in the PDN impedance curve. The maximum occurs when the integration is performed between $T/2-E/2$ and $T/2+E/2$. Correspondingly, t_2 in (13) is determined as $T/2+E/2$.

The total PSIJ under CCC operation is characterized by the time interval error (TIE) sequence. TIE is defined as the timing difference between the ideal and actual edges. It is the discrete version of CTIE and can be obtained from measurement. The measured TIE for eight cases is shown in Fig. 18. The TIE sequence is obtained by comparing the edge locations of the measured inverter chain output waveforms with and without the PDN noise. The calculated D multiplied by the voltage ripple integration result for the A1A2A3 = 000 case is shown in Fig. 19. From this curve, the jitter can be determined. The minimum CTIE is the value at time $T_r+E/2$ minus the value at time $T_r-E/2$. The maximum CTIE is the value at time $T/2+E/2$ minus the value at time $T/2-E/2$. Then, the jitter is the difference

between the maximum and minimum CTIE. For the case of 000 amplitude control bits, the measured jitter is 111.5 ps, while the calculated jitter is 108.6 ps.

For the eight current peak cases, the measurement and calculation results are summarized in Table II. Except in the last two cases, the error percentage is within 8.1%. Because the maximum voltage decrease in the last two cases is larger than 0.2 V, it might possibly be too large and could introduce nonlinear effects. The proposed derivation assumes that the PSIJ sensitivity is linear in a small voltage ripple range. Therefore, the relatively large errors for these cases are reasonable.

IV. Conclusion

With the derived analytical formulation, the PDN design parameters are directly correlated with the jitter of a specific circuit, given the triangular noise current information. The proposed PSIJ prediction method, based on the PDN *R–L–C* parameters, is validated through experiments on the designed test vehicle. With the derived PDN–PSIJ correlation, as long as the ratio of the values of adjacent decoupling capacitors is sufficiently large, which can be satisfied in general design, the total jitter of the driver with the current PDN design can be evaluated. Alternatively, the guidelines for PDN design can be developed based on the noise current information and a defined buffer jitter criterion, as establishing the PDN design guidelines is a reverse problem of the jitter analysis caused by PDN noise. In future research, the proposed approach could be further extended to accommodate more complicated PDN noise, such as the overlapped burst impulse patterns and the ac steady-state noise.

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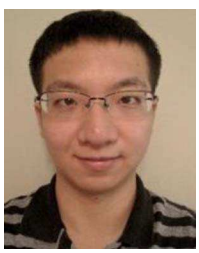

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