

Electronic-photonic quantum systems on-chip

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Abstract: We present progress towards realizing electronic-photonic quantum systems on-chip; particularly, entangled photon-pair sources, placing them in the context of previous work, and outlining our vision for mass-producible quantum networking blocks. © 2022 The Author(s)

The recent, rapid, buildup of nascent but promising quantum computing technologies necessitates a need for realizing a large-scale quantum network to facilitate their cooperative use. With commercial quantum computing already a reality, the quantum processing power of such systems can be scaled in a way similar to the parallelism of interconnected cores or servers in classical data centers and supercomputers. This will, however, require optical quantum networks capable of interconnecting quantum nodes, and transmitting and receiving quantum states without loss of entanglement. These networks may spark revolutionary developments, such as a quantum internet.

Our vision is to develop monolithic electronic-photonic quantum systems on-chip (epQSoCs) to function as quantum state transceivers (QSTs) in a quantum communications network. QSTs will be systems with mixed classical and quantum capabilities, and are ideally implemented in CMOS to allow for cost and complexity scaling. CMOS is not only the technology to have scaled to billions of components on a single chip, but it also allows for fast control of the electrical components in quantum photonic circuits. Furthermore, monolithic integration simplifies packaging of the components, which enables more complex systems, such as a microprocessor with photonic I/O [1].

Thus far, our work has concentrated on building a single-chip photon-pair source using spontaneous four-wave mixing (SFWM) in a silicon ring microresonator. Figure 1 shows an illustration of our epQSoC-QST concept, on which we have made progress in multiple stages. To date, we have demonstrated the first quantum-correlated photon-pair generation device in an unmodified CMOS process; the first single-chip integrated photon-pair source with pump filtering exclusively on-chip; and the first electronic-photonic quantum system-on-chip with feedback-controlled frequency locking, high-extinction pump rejection, and signal/idler demultiplexing. Table 1 places our work within the

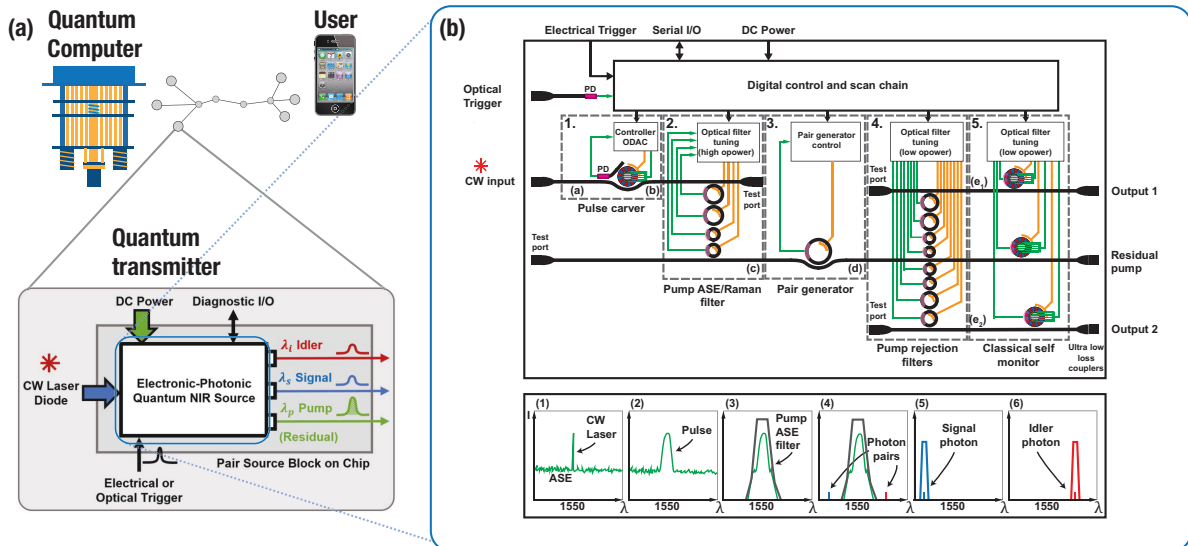


Fig. 1: (a) Illustration of our concept. Each transmitter in a quantum network is a “wall-plug” epQSoC, which takes DC power and a CW laser supply as inputs, and outputs photon pairs. (b) The proposed source comprises: (1) a pulse carver (analog modulator), (2) a bandpass filter to reject the pump laser’s amplified spontaneous emission (ASE), (3) a closed-loop feedback-controlled microring based on SFWM, (4) Vernier high-order microring bandpass filters to reject the pump photons and demultiplex the (5) signal and (6) idler photons. The chip’s optical I/O is achieved with low-loss grating couplers [2].

context of other exciting demonstrations in this field, in which advances are being made at a rapid pace, as the chronology in Fig. 2 illustrates.

Reference (italic = <i>our work</i>)	Filter type	Number of chips	Frequency locking	Detected coincidence rate (cps)	Single chip pump extinction ratio (dB)	Off chip pump extinction ratio (dB)	Losses from pair source to detectors (dB)	CAR
Harris <i>et al.</i> , 2014 [4]	Bragg grating	2	×	0.04	65 / 95–100	0	37	50
Piekarek <i>et al.</i> , 2017 [5]	Cascaded lattice	2	×	1.16	55	0	25	165
Gentry <i>et al.</i> , 2018 [6]	Cascaded microrings	1	×	410	97	0	6	12
Kumar <i>et al.</i> , 2020 [7]	CROW	2	×	138	74	0	26	155
Oser <i>et al.</i> , 2020 [8]	Cascaded Bragg grating	1	×	151	80	22	17	60
Afifi <i>et al.</i> , 2021 [9]	Contra-directional couplers	1	×	0.5	60	40	8	125
Kumar <i>et al.</i> , 2021 [10]	CROW	1	×	1900	>96	>40	16	145
Fargas-Cabanillas <i>et al.</i> , 2021 [11]	Cascaded microrings	1	×	600	>70	0	8	15
Kramnik <i>et al.</i> , 2022 [12]	N/A	1	✓	300	N/A	>100*	10	38
Wang <i>et al.</i> , 2022 [13]	Cascaded microrings	1	✓	50	>80	>0*	7	5

Table 1: Comparison to similar pair sources in the literature, with our work in italics. Highlighted in green are desirable properties for a pair source: single-chip, with frequency locking, and with all pump rejection performed on-chip. Red indicates that these conditions are not met, and orange indicates that the condition is met with caveats. *Note that for [13], only one of the signal or idler channels required off-chip filtering, due to a bug in the design which prevented full signal/idler demultiplexing.

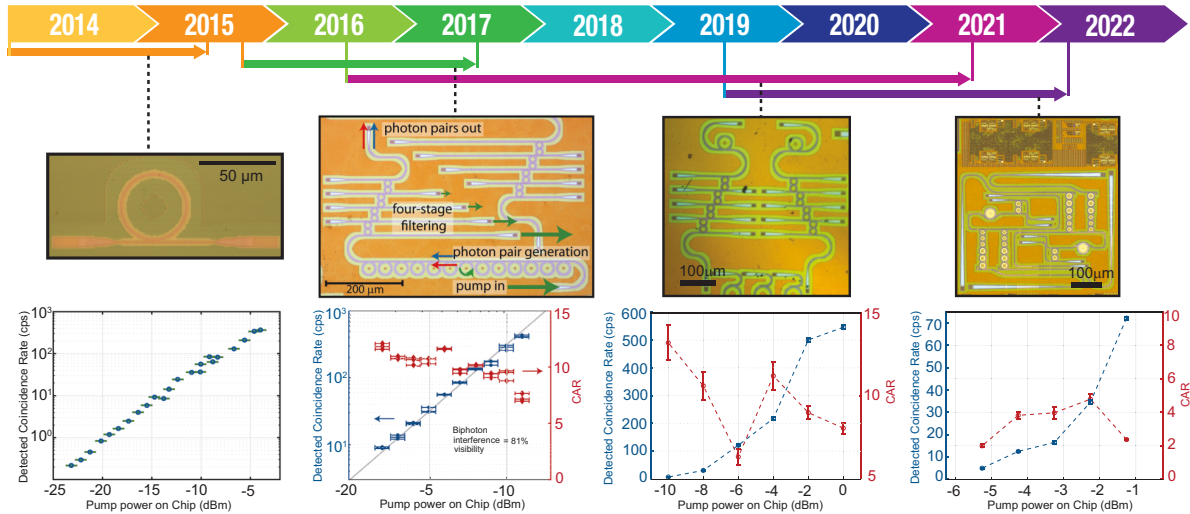


Fig. 2: A chronology of our work on developing a single-chip photon-pair source with electronics and photonics on the same chip, indicating when the chip design was submitted to the foundry, and when the work was published. From left to right, the relevant citations are [3], [6], [11], and [13].

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