Monolithically Integrated High-Order Vernier Filters and Tuning Circuits for Electronic-Photonic Quantum System-on-Chip

J.M. Fargas Cabanillas[1,†], D. Kramnik[2], I. Wang[1], S. Buchbinder[2], A. Ramesh[3], P. Kumar[3], V. Stojanović[2], Anatol Khilo[1,*] and M.A. Popović[1,‡]

[1]*Department of Electrical and Computer Engineering, Photonics Center, Boston University, Boston, MA 02215, USA*
[2]*Department of Electrical Engineering and Computer Science, UC Berkeley, Berkeley, CA 94720, USA*
[3]*Center for Photonic Communication and Computing, Dept. of Electrical and Computer Eng., Northwestern University, Evanston, IL 60208, USA*
[*]*Current affiliation: Ayar Labs Inc., 3351 Olcott Street, Santa Clara, CA 95054, USA*

[†]*jofa@bu.edu,* [‡]*mpopovic@bu.edu*

Abstract: We demonstrate a monolithically integrated 6th-order filter, with heater driver circuits implemented alongside photonics in a zero-change 45 nm CMOS platform, achieving <1 dB drop loss and >80 dB on-chip pump power suppression.

Single photon sources are a key building block for quantum photonics technologies and integrated silicon photonics is a promising platform for realizing them due to its compatibility with scalable, high-fidelity CMOS manufacturing [1,2]. A key challenge in scaling the complexity of on-chip systems based on nonlinear optical photon-pair sources is filtering out the classical pump light in order to make use of the quantum-correlated photons downstream. Much progress has been made in achieving sufficient pump extinction [$\mathcal{O}$(100 dB)] [3, 4] with on-chip filtering. Further improvements in on-chip filtering could enable the addition of single photon detectors on chip for a fully integrated quantum signal processing system. More generally, it could enable small form-factor fiber-attached chips with only single photons exiting into the fiber. Here, we demonstrate 6th-order, tunable, high-extinction Vernier optical band-pass filters, with heater driver circuits implemented alongside photonics in a 45 nm SOI CMOS process. They show more than 80 dB classically measured pump suppression, less than 1 dB insertion loss, and rapid reconfigurability in a highly integrated form factor. The device can be a self-contained "IP block" (component) in electronic-photonic platforms and a building block for what we envision as a new class of electronic-photonic quantum systems on-chip (EPQSoC).

Fig 1(a) shows a 3D layout of our first EPQSoC intended to be a "wall-plug" source of photon pairs. The system includes low-loss grating couplers to couple the pump in and the single photons out of the chip. A second-order tunable

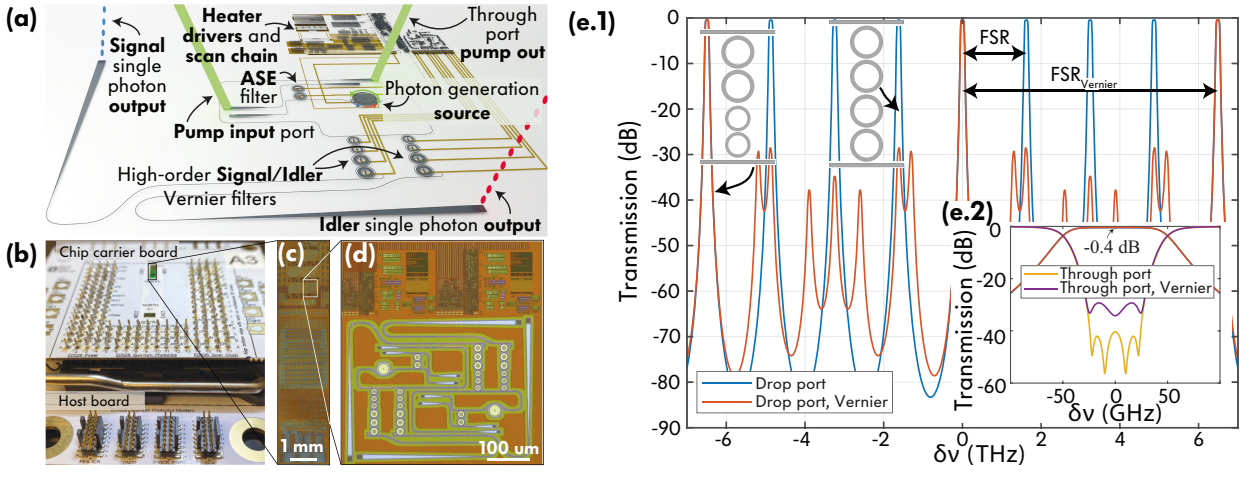

Fig. 1: (a) Electronic-photonic quantum system-on-a-chip (EPQSoC) schematic; (b) flip-chip packaging scheme with chip carrier and host board; (c) top view of SOI CMOS die that is flip-chip attached to PCB with Si substrate removed by XeF_2 etch; (d) optical micrograph of a wall-plug photon-pair source EPQSoC; (e) simulated 4th-order regular and Vernier scheme micro-ring-filter transmissions: (e.1) drop port, (e.2) through port.

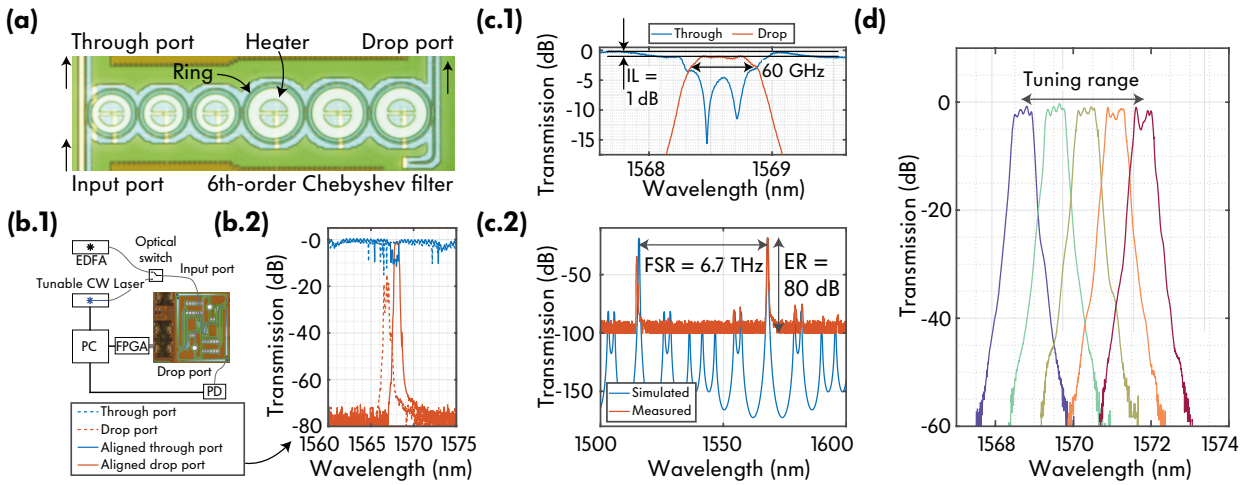

Fig. 2: (a) Sixth-order ring filter optical micrograph; (b.1) filter tuning set up; (b.2) filter transmission before and after alignment; (c.1) aligned-filter zoom-in of passband; (c.2) aligned-filter drop-port simulation compared with the measurement; (d) aligned-filter drop-port transmission sweeping all the tuning range.

filter aligns to the pump laser attenuates the ASE noise. This is followed by a wavelength-tunable photon-pair source which can self-lock to the pump wavelength [5]. Two high-order filters, with one centered at the signal and the other at the idler wavelength, remove almost all the classical pump light and route the pairs of single photons to separate output grating couplers (one each for the signal and idler photons).

Vernier high-order filters use rings of different radii to extend the effective free-spectral range (FSR) well beyond schemes using rings of the same radius [6]. In Fig 1(e) we show by example the difference between a regular and a Vernier scheme 4$^{\text{th}}$-order filter. The two different filter's FSRs are related as $FSR_{\text{Vernier}} = 4 \cdot FSR_0$. The Vernier scheme 4$^{\text{th}}$-order filter is composed of two rings of $FSR = FSR_0$ and two others with $FSR = 0.8 \cdot FSR_0$.

Fig 2(a) shows a micrograph of the characterized 6$^{\text{th}}$-order filter. As in the previous example, the FSR ratio between the big and small rings is 0.8. Each ring has an integrated doped-silicon heater with a DAC driver on the chip. The high-level control of the chip scan chain is done on a PC using Python through an FPGA [Fig 2(b.1)]. A multi-variable non-derivative optimization algorithm (Nelder-Mead method) is used to align the filters. The alignment procedure is performed using a broadband source, to convert a highly nonlinear, not ill-behaved optimization space into one with a well-defined global optimum. Fig 2(b.2) shows the filter response before and after alignment.

The measured drop-filter insertion loss is less than 1 dB as shown in Fig 2(c.1) (0.78 dB in simulation). In Fig 2(c.2) we show the measured drop-port transmission, which is overlapped with the simulated drop-port transmission (offset in wavelength and amplitude to match the measured passband at 1568.7 nm). The filter 3 dB bandwidth is 60 GHz, the effective FSR is 6.7 THz, and the measured pump rejection is at least 80 dB, the measurement being limited by the sensitivity of our optical power sensor. In future studies, we will use single-photon detectors to experimentally verify that the extinction can go down to 160 dB as shown in simulation. Finally, once the filter is aligned, we can tune the passband wavelength by adding a scaled version of the "eigenvector of the system" to the heater-codes vector which accounts for all the thermal cross-talk, giving a total of 4 nm tuning range for the filter, as shown in Fig 2(d).

In separate experiments we have demonstrated integrated feedback control of four-wave mixing via carrier sweep-out in a photon generation source [5], operating in both stimulated and spontaneous regimes and (here) integrated pump filtering, paving the way for a fully-integrated pair generator SoC.

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