A Four-level Active Gate Driver with Continuously Adjustable Intermediate Gate Voltages

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***Abstract*— The *dv*/*dt* and *di*/*dt* during switching transients are increased dramatically due to the very fast switching speed of silicon carbide (SiC) MOSFET, which are the major sources for the electromagnetic interference (EMI) noises. To improve the system's EMI performance, a novel four-level active gate driver (4-L AGD) with independent adjustable turn-on and turn-off gate voltages is proposed. Based on the trajectory modeling of the SiC MOSFET, *dv*/*dt*, *di*/*dt*, switch losses can be optimized by applying different intermediate voltage levels during turn-on and turn-off transients to improve the system EMI performance, suppress voltage and current overshoots and oscillations. Compared with the existing AGD with the fixed intermediate voltage, the proposed AGD's intermediate voltage level can be flexibly and continuously adjusted in a very wide range during both turn-on and turn-off transients. The proposed AGD working principles, trajectory modeling and the optimizations of the intermediate voltages are analyzed. Finally, simulations and experimental validations are carried out on a double pulse test platform with different intermediate voltages. The proposed AGD has the capability to fine tune *dv*/*dt*, *di*/*dt* and suppress overshoots effectively according to the experimental results.**

***Keywords*— Active gate driver(AGD), trajectory modeling of silicon carbide (SiC) MOSFET, trajectory optimization algorithm, electromagnetic interference (EMI), switch losses.**

I. INTRODUCTION

Silicon carbide (SiC) metal–oxide–semiconductor field-effect transistor (MOSFET) is widely used in power converters nowadays because of its higher operating frequency, higher power density, lower switching and conduction losses when compared with its silicon counterpart [1]. However, excessive drain-source voltage slew rate *dv*/*dt* during the fast switching and reverse recovery of the body diode might cause false switching, self-turn-on effect and introduce common mode noise into the circuit [2, 3]. Higher drain to source current slew rate *di*/*dt* will lead to high voltage surge on the drain-source voltage V_{DS} that may exceed its rated breakdown voltage and cause current overshoot and oscillations due to inevitable parasitic elements in the circuit and power devices, causing permanent damage to the MOSFET [4]. All the elaborate details about the causes and negative impacts of typical switching oscillations are analyzed in [5]. Controlling *dv*/*dt*, *di*/*dt* to suppress electromagnetic interference (EMI) noises has been an intractable problem for SiC MOSFET applications for decades. To increase the operation reliability and efficiency of SiC-based converters, the analytical modeling of the switch transients should be well investigated and advanced techniques are expected to overcome the switching oscillations.

Different technologies are adopted in existing literatures to suppress the switching oscillations. These are mainly caused by *dv*/*dt*, *di*/*dt*, parasitic inductance and capacitance in the circuit. Optimizing the package of the power devices and printed circuit board (PCB) layout to reduce the parasitic parameters is an obvious direction to solve these issues, but the latest packaging technologies are expensive and the stray inductance is hard to be reduced due to the complex structure of the PCB [6]-[9]. Using an additional RC snubber is another common method to mitigate these effects [10, 11]. The RC snubber network can suppress the switching stress and damp the ringing to mitigate the oscillations and overshoots. However, adding a passive RC snubber will decrease the overall efficiency of the converter.

Currently, more attention is attracted by the development of active gate driver (AGD) method due to its flexibility and practicability [12]-[19]. The most widely used approach is the variable external gate resistance method [12, 13]. By adjusting gate resistance in different switching stages, the switching speed can be tuned. Nevertheless, the adjustable steps are limited. The variable gate voltage method is popular because an adjustable voltage regulator is always easier to be implemented. In [14], only fixed intermediate voltage level (0 V) is provided for the turn off transient. In [15, 16], the switching slew rate can be optimized by an S-shape or series voltage-changing slew rate control profile. However, the circuitry is complex or expensive. In [17]-[19], there is a four-level slew rate control profile, but either the position or

value of the intermediate voltage is limited. In [18], although the intermediate voltage levels can be adjusted, a discrete adjustment step exists and the turn-on and turn-off intermediate voltage levels are interrelated. Thus, the optimizations for both turn-on and turn-off processes cannot be achieved. In addition, less literatures talk about how to select the intermediate voltage.

In this paper a four-level active gate driver (4-L AGD) with independent turn-on and turn-off voltage levels is proposed to improve the system performance. Working principles and circuit implementations are demonstrated in section II. The modeling of the switching transients during turn-on and turn-off is analyzed in section III. In addition, a model-based trajectory optimization algorithm is developed to decide the selection of intermediate voltages for turn-on and turn-off process. Finally, the simulation validation and experimental verification of the model is presented in section IV and V.

II. Circuit Design and Working Principles of The Proposed Four-Level Active Gate Driver

For traditional gate driver circuit design, the trajectory modeling for dv/dt and di/dt during turn-on and turn-off transient can be express from [19]:

$$\begin{cases} \dfrac{di_{ds}}{dt} = \dfrac{V_{GG} - V_{th} - i_{ds}/g_m}{C_{iss} \cdot R_g / g_m + L_s} \\ \dfrac{dv_{ds}}{dt} = -\dfrac{V_{GG} - v_{mil}}{C_{gd} \cdot R_g} \end{cases} \quad (1)$$

$$\begin{cases} \dfrac{di_{ds}}{dt} = g_m \cdot \dfrac{V_{th} + i_{ds}/g_m - V_{GG}}{C_{iss} \cdot R_g \Big/ g_m + L_s} \\ \dfrac{dv_{ds}}{dt} = \dfrac{V_{GG} - v_{mil}}{C_{gd} \cdot R_g} \end{cases} \quad (2)$$

where V_{GG} is gate to source voltage, V_{th}, g_m is the threshold voltage and transconductance of the device, respectively. R_g is the gate driver resistor. C_{gs}, C_{gd} and C_{ds} are the junction capacitances. $C_{iss} = (C_{gs} + C_{gd})$ is the input capacitance of the device. $v_{mil} = V_{th} + i_{ds}/g_m$ is the Miller plateau voltage. From the equations, the dv/dt and di/dt can be adjust by varying gate to source voltage V_{GG} and external resistance R_g. In this paper, the main principle of the proposed AGD is to apply different gate to source voltage V_{GG} during the current and voltage changing duration to control the slew rate, thus suppressing the overshoots, oscillations and switch losses.

Fig.1 shows the general structure of the proposed AGD. The AGD circuitry consists of three parts: a local controller, intermediate voltage generator: two buck converters and voltage selectors S_1, S_2, S_3. The independent adjustable turn-on and turn-off intermediate voltage v_{gON2} and v_{gOFF2} are

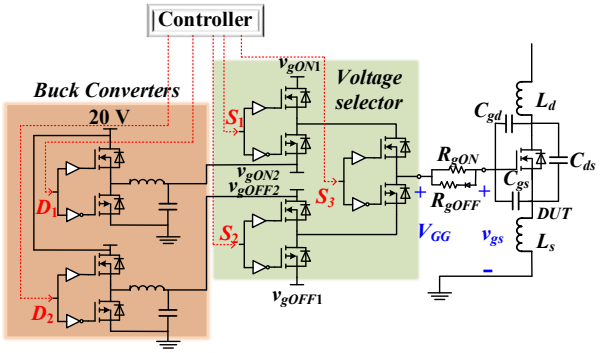

Fig. 1. Schematic of the proposed 4-L AGD

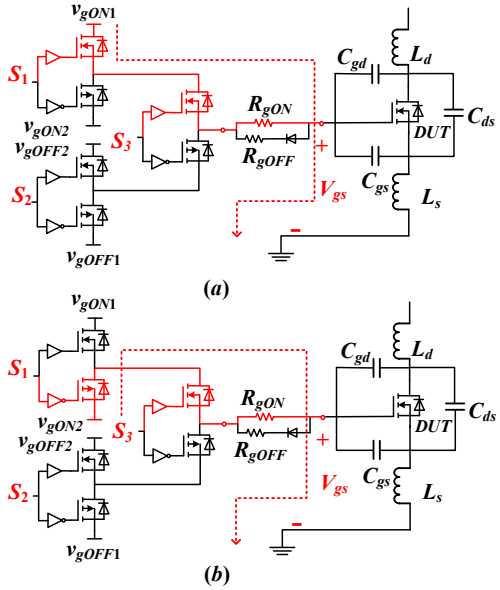

Fig. 2. Operation modes of the AGD at turn-on: (a) v_{gON1} 20 V generating circuit; (b) intermediate v_{gON2} generating circuit.

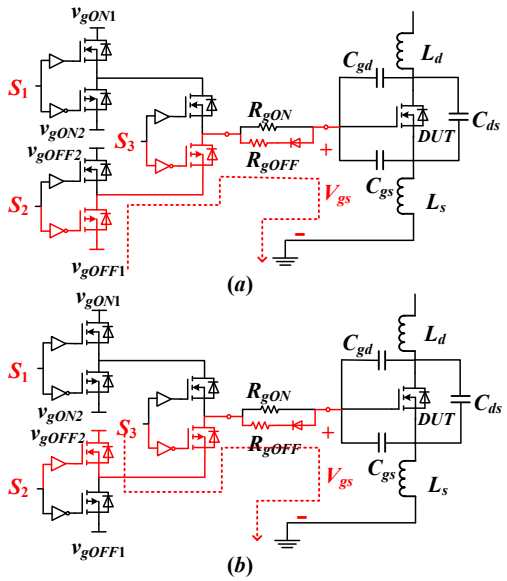

Fig. 3. Operation modes of the AGD at turn-off: (a) v_{gOFF1} -5V generating circuit; (b) intermediate v_{gOFF2} generating circuit.

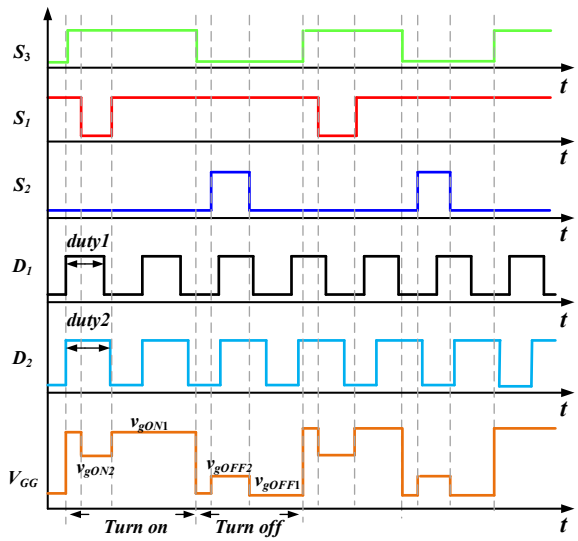

Fig. 4. Control waveforms

regulated by two independent duty ratios D_1 and D_2 of the buck converters. The power supply of the buck converters is 20 V, so the output voltage range of the buck converter is 0 V to 20 V, theoretically. The frequency of the buck converters should be high enough to reduce size and response fast. The local controller will generate the pulse width modulation (PWM) signals for buck converters and voltage selectors. It also controls the duration of each substage, i.e., the applied period of the intermediate voltage v_{gON2} for turn-on process and v_{gOFF2} for turn-off process. For the model of SiC MOSFET, C_{gs}, C_{gd} and C_{ds} are the junction capacitances. L_d and L_s are the equivalent parasitic inductances on the drain and source side, respectively. R_{gON} and R_{gOFF} are the turn-on, turn-off gate driver resistance. V_{GG} is the output voltage of the voltage selector S_3 and v_{gs} is the voltage across the gate and source terminals of the device.

From the SiC MOSFET data sheet, the traditional turn-on and turn-off gate voltages are applied as v_{gON1} 20 V and v_{gOFF1} -5 V, respectively. To optimize the slew rate of i_{ds} and v_{ds}, the intermediate voltages v_{gON2} and v_{gOFF2} are applied. Therefore, four gate driver voltage levels are generated by the proposed AGD.

The operation modes of the proposed 4-L AGD are shown in Fig.2 and Fig.3. For turn-on transient, there are two operation modes to generate the turn-on voltage 20 V and v_{gON2}. When S_3 is pulled up, S_1 is pulled up first to apply the traditional turn-on voltage 20 V, then S_1 will be pulled down during the current rising and voltage falling period to apply intermediate voltage v_{gON2}. When the turn-on process is finished, S_1 changes to high level and 20 V is applied again to guarantee the device under test (DUT) turning on completely. Similarly, for turn-off transient, when S_3 is pulled down, S_2 is pulled down first thus the -5 V will be applied. During the current falling substage, S_2 is pulled up to apply the intermediate voltage v_{gOFF2}. When the turn-off process

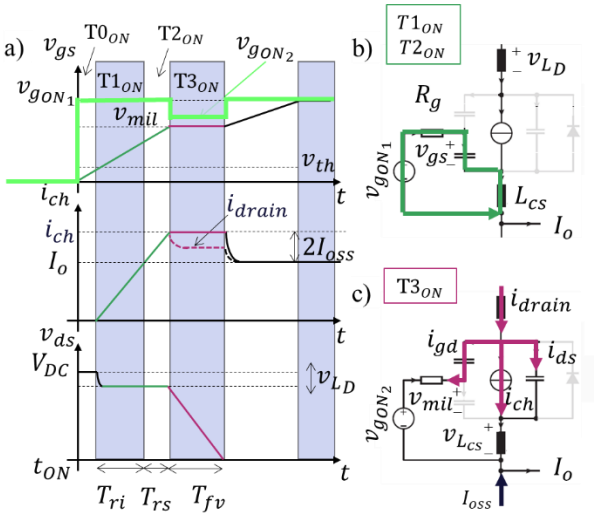

Fig. 5. SiC MOSFET switching turn-on transient: a) waveforms; b) equivalent circuit during T_{1ON} and T_{2ON}; c) equivalent circuit during T_{3ON}.

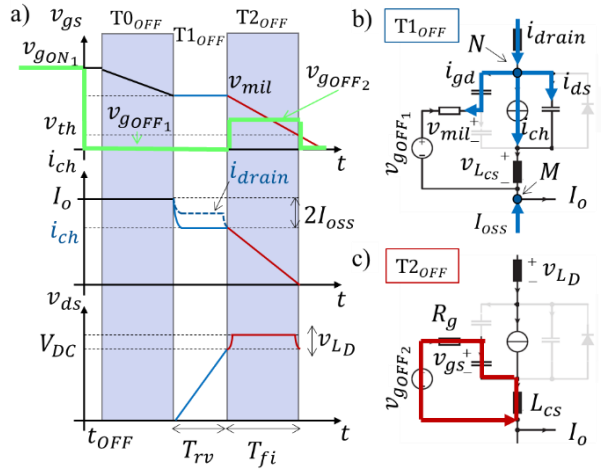

Fig. 6. SiC MOSFET switching turn-off transient: a) waveforms; b) equivalent circuit during T_{1FF}; c) equivalent circuit during T_{2OFF}.

ends, S_2 changes to low level and -5 V is applied to guarantee the device is turning off completely. The control waveforms of S_1, S_2, S_3, D_1, D_2 and V_{GG} are illustrated in Fig.4.

III. Modeling and Optimization

Fig.5 and Fig.6 show the characteristic waveforms and equivalent circuit of turn-on and turn-off transient of the SiC MOSFET. The turn-on process mainly includes turn-on delay ($T0_{ON}$), current rising ($T1_{ON}$), reverse recovery of diode ($T2_{ON}$), voltage falling ($T3_{ON}$). The turn-off process mainly includes turn-off delay ($T0_{OFF}$), voltage rising ($T1_{OFF}$), current falling ($T2_{OFF}$). As the equivalent circuits shown, the MOSFET channel is modeled as a controlled current source i_{ch}, which can be expressed as [20]:

$$i_{ch} = g_m\left(i_{ch}\right)\left(v_{gs} - V_{th}\right) \tag{3}$$

where g_m is the transconductance through the MOSFET channel i_{ch}, which is:

$$g_m\left(i_{ch}\right)=\sqrt[x]{\frac{k_1 i_{ch}^{\ x}}{i_{ch}-k_2}} \tag{4}$$

the constants x, k_1 and k_2 can be extracted from the corresponding datasheet by a curve fit of gate-source voltage v_{gs} with drain-source current i_{ds}. I_o is the output current.

For turn-on transient: during interval $T0_{ON}$, the turn-on gate voltage v_{gON1} = 20 V is applied and the turn on process is initiated. The gate to source capacitance C_{gs} is charged while the Miller capacitance C_{gd} is discharged, which leads to gate voltage v_{gs} rising to the threshold voltage V_{th}. During interval $T1_{ON}$, the drain to source current rises to the load current I_0 as soon as v_{gs} reaches V_{th}. At the same time intermediate voltage v_{gON2} is applied. The current rising time t_{ri} is calculated by [21]

$$t_{ri}=-\ln\left(1-\frac{I_0}{g_m\left(V_{GG}-V_{th}\right)}\right)\left(C_{gs}R_{on}+L_s g_m\right) \tag{5}$$

The current slope of i_{ds}, energy losses during this interval can be calculated as follows:

$$di_{ds}/dt=\frac{i_{ch}+2I_{oss}}{t_{ri}} \tag{6}$$

$$Esw_{ri}=\frac{1}{2}V_{DS}I_0 t_{ri} \tag{7}$$

During interval $T2_{ON}$ and $T3_{ON}$, the current is increased by $2|I_{oss}|$ because of the reverse recovery effect of the body diode. Details about the diode reverse recovery model can be found in [22]. The falling time, slew rate of drain-source voltage, and energy losses are approximately:

$$t_{fv}=-\frac{Q_{oss}}{I_{oss}} \tag{8}$$

$$\frac{dv_{ds}}{dt}=-\frac{V_{DS}}{t_{fv}} \tag{9}$$

$$Esw_{fv}=\frac{1}{2}V_{DS}\left(I_0-2I_{oss}\right)t_{fv} \tag{10}$$

Summarizing, the loss energy in the turn on process is:

$$Esw_{ON}=\frac{1}{2}V_{DS}I_0 t_{ri}+\frac{1}{2}V_{DS}\left(I_0-2I_{oss}\right)t_{fv} \tag{11}$$

For turn-off transient: during interval $T0_{OFF}$, v_{gOFF1} = -5 V is applied, then the input capacitance C_{iss} is discharged and v_{gs} decays to the minimum value called the first Miller plateau. During interval $T1_{OFF}$, drain-source voltage is rising to DC link value V_{DS}, the output capacitance C_{oss} of the device is charged. Simultaneously, i_{ch} is reduced by two times the current required I_{oss} to charge C_{oss}, where C_{oss}= C_{gd} + C_{ds}, I_{oss}=i_{ds}+i_{gd}. Then the voltage rising time can be defined by the time required to charge C_{oss}.

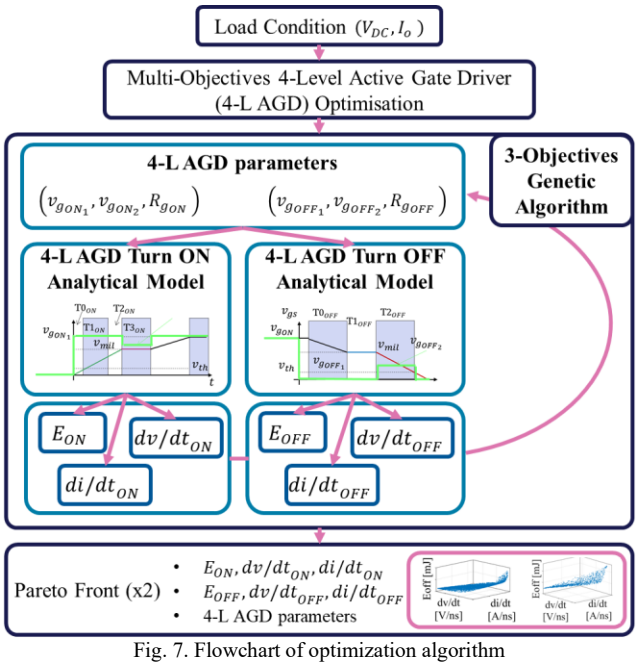

Fig. 7. Flowchart of optimization algorithm

$$t_{rv}=\frac{Q_{oss}}{I_{oss}} \tag{12}$$

where Q_{oss} is the voltage-dependent charge stored in C_{oss} at voltage V_{DS}. The slew rate of v_{ds} and energy loss during this interval are:

$$\frac{dv_{ds}}{dt}=-\frac{V_{DS}}{t_{rv}} \tag{13}$$

$$Esw_{rv}=\frac{1}{2}V_{DS}\left(I_0-2I_{oss}\right)t_{rv} \tag{14}$$

During interval $T2_{OFF}$, the remaining current i_{ch} is decreasing, which is proportional to the gate-source voltage. Thus, the time required for current falling to zero can be expressed [21]:

$$t_{fi}=-\ln\left(\frac{V_{th}+V_{GG}}{V_{Miller}+V_{GG}}\right)\left(C_{gs}R_{off}+L_s g_m\right) \tag{15}$$

The fast-decreasing current will also cause a voltage drop across the parasitic inductance L_d in the power loop, which leads to an increase in the v_{ds} by:

$$V_{Ld}=L_d\left(I_0-2I_{oss}\right)/t_{fi} \tag{16}$$

The slew rate of i_{ds} and energy loss are given as follows:

$$di_{ds}/dt=\frac{i_{ch}}{t_{fi}} \tag{17}$$

$$Esw_{fi}=\frac{1}{2}\left(V_{DS}+V_{Ld}\right)\left(I_0-2I_{oss}\right)t_{fi} \tag{18}$$

Summing up the loss during the interval $T1_{OFF}$ and $T2_{OFF}$, the total energy loss during turn-off is:

$$Esw_{OFF} = \frac{1}{2} V_{DS} (I_0 - 2I_{oss}) t_{rv} + \frac{1}{2} (V_{DS} + V_{Ld}) (I_0 - 2I_{oss}) t_{fi} \tag{19}$$

The analytical switching model described in this section is implemented in MATLAB environment using two functions, one for turn-on event and one for turn-off event.

According to the trajectory modeling, using intermediate voltage can reduce the slew rate and related EMI noise, but it also causes higher energy losses. Thus, an optimization algorithm based on a multi-objective stochastic population-based optimization algorithm (NSGA-II embedded in MATLAB environment) is developed to decide the optimized intermediate voltage levels by considering the tradeoff of the energy losses against the EMI noise. The flowchart for the optimization function is shown in Fig.7. In this case, it is considered that, at circuit design stage, all the gate driver parameters can be varied, including maximum and minimum voltage levels, V_{gON1} and V_{gOFF1}, and the gate resistors, R_{gON} and R_{gOFF}. While during converter normal operation, just the intermediate voltage levels, V_{gON2} and V_{gOFF2}, can be changed online. To sum up, the design algorithm consists of six input parameters, three for each switching transition.

Thanks to the proposed 4-L AGD topology, the intermediate voltage levels for turn-on (v_{gON2}) and turn-off (v_{gOFF2}) are independent. Thus resulting in the possibility of optimizing independently the two switching trajectories. Each optimization loop utilizes the analytical switching models, for turn-on and turn-off, to carry out a performance evaluation and identify the optimal combination of 4-L AGD parameters to minimize three objectives for both switching transitions: energy losses, *dv*/*dt*, and *di*/*dt*. Once the performance indexes are calculated, the algorithm solves the following multi-objectives minimization problems:

$$\min\left(E_{ON}, \frac{di}{dt}_{ON}, \frac{dv}{dt}_{ON} \right) \tag{20}$$

$$\min\left(E_{OFF}, \frac{di}{dt}_{OFF}, \frac{dv}{dt}_{OFF} \right) \tag{21}$$

Having the following boundary conditions:

$$\begin{cases} v_{gON_2} < v_{gON_1} < v_{gMax} \\ v_{mil} < v_{gON2} < v_{gON_1} \\ R_{gON} > 0 \end{cases} \tag{22}$$

$$\begin{cases} v_{g\,\min} < v_{gOFF_1} < v_{gOFF_2} \\ v_{gOFF_1} < v_{gOFF_2} < v_{mil} \\ R_{gOFF} > 0 \end{cases} \tag{23}$$

where v_{gMax} and v_{gmin} are respectively the maximum and minimum gate voltage level admissible for the device, while

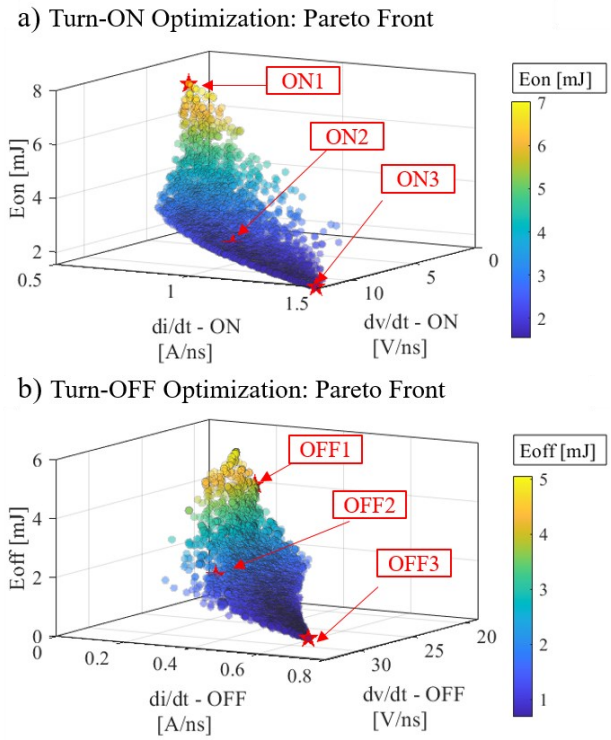

Fig. 8. 4L-AGD optimization results using C2M0025120D at 800V and 40A. Optimal pareto front solutions for: a) turn-ON case, b) turn-OFF case.

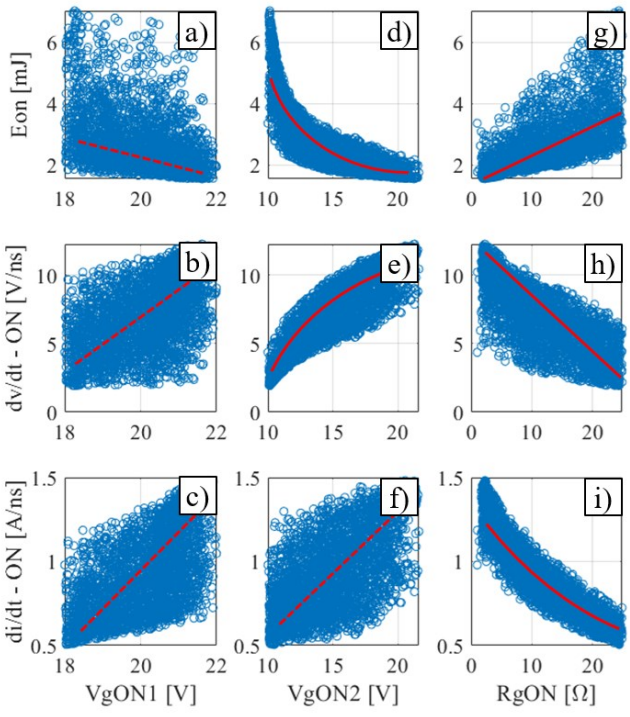

Fig. 9. Turn-On gate driver parameters (V_{gON1}, V_{gON2}, R_{gON}) variations along the Pareto-front and their effect on the three objectives (E_{on}, *dv*/*dt*, *di*/*dt*).

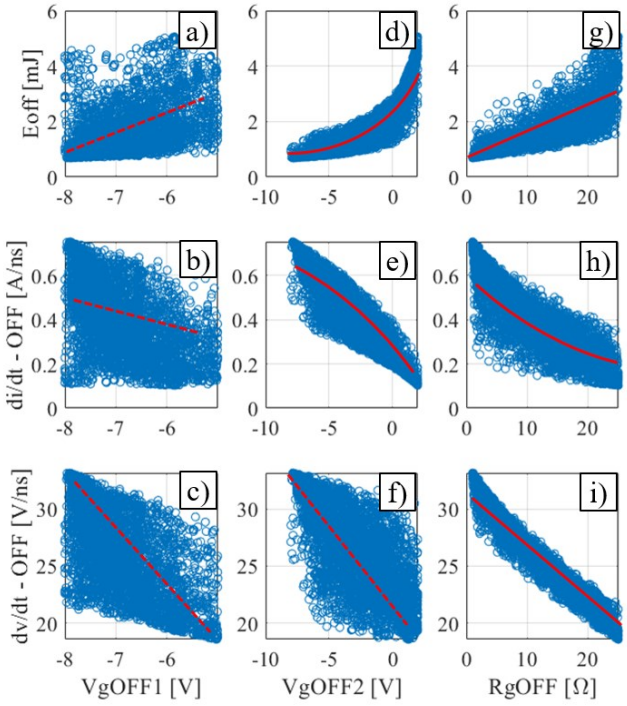

Fig. 10. Turn-Off gate driver parameters (V_{gOFF1}, V_{gOFF2}, R_{gOFF}) variations along the Pareto-front and their effect on the three objectives (E_{off}, dv/dt, di/dt).

v_{mil} is the Miller plateau voltage corresponding to that particular switching event.

IV. Optimisation Results

Although the proposed optimization strategy along with the developed analytical model are general and can be used to optimize the 4L-AGD on a broad range of operative points, in this work this algorithm is applied to a simple case study example: a single point of load scenario, corresponding to a half-bridge devices configuration, with a DC bus voltage of 800V and a load current of 40 A.

The devices selected are Wolfspeed 1200V-63A (C2M0025120D) SiC MOSFETs. Stray capacitances and transconductance curves and other parameters necessary as input for the analytical switching model are imported from the datasheet [23].

Fig. 8 shows the solutions evaluated during the two independent optimizations for turn-on and turn-off transients, each dot marker corresponds to a different combination of the three gate driver parameters. The optimal solutions are shown in the three-dimensional space: energy losses - dv/dt - di/dt. In this case the Pareto-front consists of a surface and all the elements that belong to it can be considered optimal solutions. As expected, faster switching transitions, corresponding to higher dv/dt and di/dt, result in lower losses. This confirms a clear competitive behavior of the three

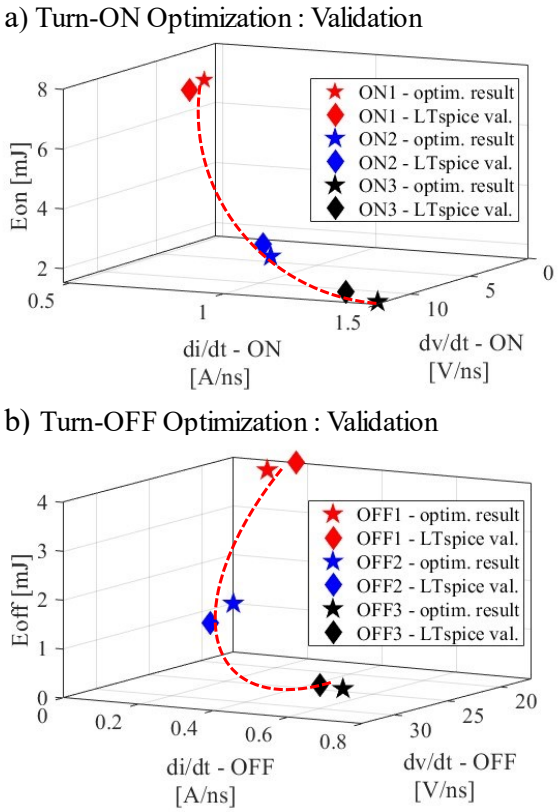

Fig. 11. Validation results, comparison between analytically predicted values and LTspice simulation results

performance indicators, justifying the multi-objectives optimization approach.

To have a better understanding of how the algorithm achieved these results, it is worth to analyze the variation of the gate driver parameters along the Pareto front.

Fig. 9 summarizes the effect of the three turn-on gate driver design parameters (v_{gON1}, v_{gON2}, R_{gON}) on the three objectives (E_{ON}, dv/dt_{ON}, di/dt_{ON}). The effect of the first and higher voltage level, v_{gON1}, can be seen in the first column of the figure matrix (Fig. 9. a-c). Even though the trends can be highlighted (dashed red line), higher v_{gON1} result in higher dv/dt and di/dt and lower losses, and there is a broad data dispersion, meaning that this parameter does not have a dominant effect on the performance indexes. On the other hand, the second and third column of Fig. 9 show the significant impact respectively of the intermediate voltage level (v_{gON2}) and gate resistor (R_{gON}). The most significant trends are highlighted with a continuous red line. In this case, turn-on AGD optimization, the most interesting result is observed in Fig.9.d and Fig.9.e: between 10V and 15V, increasing the intermediate voltage level contributes to strongly reduce the energy losses and increase the dv/dt, after 15V the positive effect on the energy losses is gradually

decreased, thus limiting the benefits of introducing an intermediate voltage level.

Similar to Fig. 9, Fig 10 summarizes the effect of the three turn-off gate driver design parameters (v_{gOFF1}, v_{gOFF2}, R_{gOFF}) on the three objectives (E_{OFF}, dv/dt $_{OFF}$, di/dt $_{OFF}$). Fig. 10. a-c shows the effect of the first and lower voltage level, v_{gOFF1}, on the three objectives. Also in this case the first voltage level, does not have a dominant effect on any of the performance indexes. Full red line are used in the second and third column of the figure matrix to highlight the dominant trend caused by variation of intermediate voltage level (v_{gOFF2}) and gate resistor (R_{gOFF}). It is worth noting that, thanks to Fig.10.d, it is possible to conclude that to have a significant benefit in terms of losses reduction the intermediate voltage level needs to be selected higher than -2V.

In this section, to validate the analytical switching model and the optimization algorithm, a subset of optimal solution is selected from the Pareto front and further analyzed with using LTspice circuit simulator. The simulation is set up to using the same condition described for the optimization example: half-bridge configuration, with a DC bus voltage of 800V and a load current of 40 A. The model used for the SiC MOSFETs is the one available on the manufacturer website for the device C2M0025120D. As shown in Fig.8, to perform this validation in a broader range of input parameters, three different solutions have been selected from each Pareto-front: ON1, ON2, ON3, OFF1, OFF2, OFF3. Fig.11 shows the comparison between the optimization results, predicted using the analytical model, and the same solutions re-evaluated using LTspice simulations. The average error is below 20% for all the analyzed combinations. While this error is not negligible and further work are necessary to improve the analytical model accuracy, it is important to note that the overall Pareto-front trend is respected, both for turn-on and turn-off, which implies that the optimality of the obtained solutions is guaranteed.

V. Experimental Results

A double pulse test was carried out to validate the proposed AGD circuit design. The half-bridges in the AGD design are all implemented with the ultrafast driver IC IXD609. In the double pulse test bench, the power device under test and the upper freewheeling device both are 1.2kV/63A SiC MOSFET (C2M0025120D) from CREE.

To verify the performance of the proposed AGD, the experiment was carried out at 400V/40A with different turn-on and turn-off intermediate voltages. The turn-on process with four different intermediate voltage V_{gON2} and traditional 20 V is shown in Fig.12. The dv_{ds}/dt, di_{ds}/dt and peak voltage V_{os} all decreased when V_{gON2} decreased from 20 V to 8 V. The turn-off process with four different intermediate voltage v_{gOFF2} and traditional -5 V is shown in Fig.13. The dv_{ds}/dt,

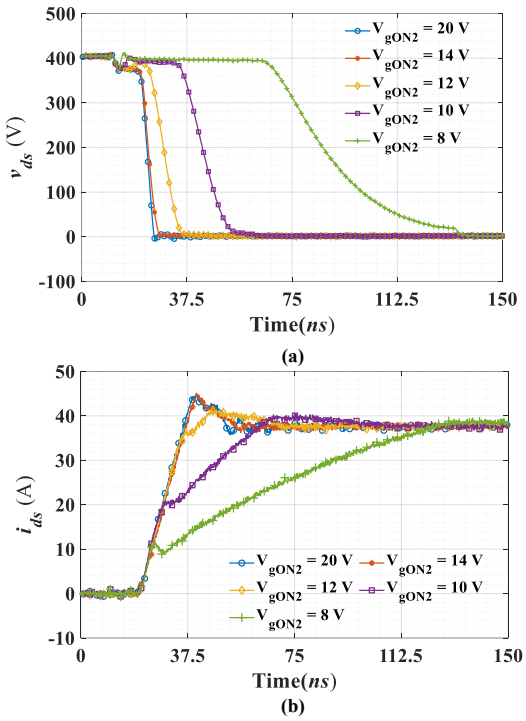

Fig.12. Turn-on switching waveforms with different V_{gON2}: (a) drain to source voltage; (b) drain to source current.

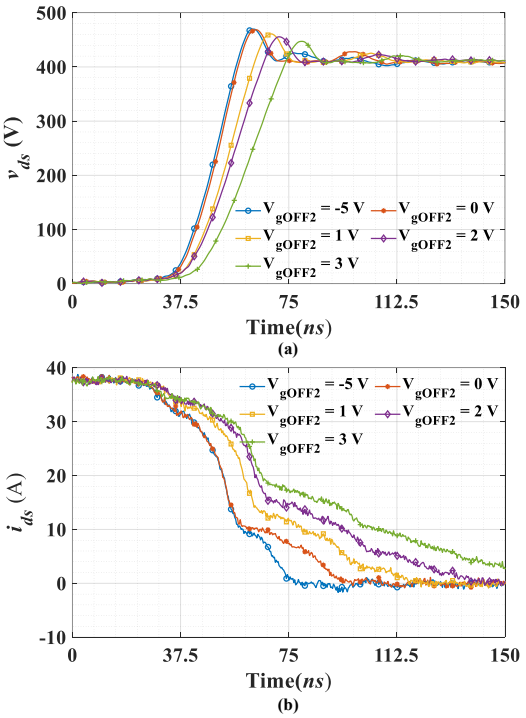

Fig. 13. Turn-off switching waveforms with different V_{gOFF2}: (a) drain to source voltage; (b) drain to source current.

di_{ds}/dt both decreased when v_{gOFF2} increased from -5 V to 3 V. All the results are summarized in Table 1.

Table 1: Experiment results summary

Turn-on switching				Turn-off switching			
v_{gON2} (v)	dv/dt (v/ns)	di/dt (A/ns)	E_{ON} (uJ)	v_{gOFF2} (v)	dv/dt (v/ns)	di/dt (A/ns)	E_{OFF} (uJ)
20	14.9	0.999	801.7	-5	20.52	2.15	69.7
14	13.2	0.991	827	0	20.19	2.01	68.3
12	7.27	0.881	1274	1	18.63	1.65	60.2
10	4.75	0.259	2172	2	16.84	0.5	55.2
8	1.63	0.122	5039	3	14.74	0.3	47.1

VI. CONCLUSIONS

This paper presented a novel four-level active gate driver design. Trajectory models for SiC MOSFET during turn-on and turn-off processes and optimization algorithm by considering the device switching loss, dv/dt, and di/dt were developed to generate the optimal intermediate turn-on and turn-off voltages. The switching slew rate can be optimized by applying the appropriate intermediate voltage during turn-on and turn-off transient at the same time. The suppression impact of dv/dt, di/dt, and energy loss was validated under 800V/40A with different intermediate voltage levels in simulation. Circuit designs were verified under 400V/40A. Compared with the existing AGD methods, the proposed solution can provide independent intermediate voltages for both turn-on and turn-off process with numerous adjustment steps to fine control switch slew rate dv/dt, di/dt and switch losses. High-voltage experimental validation for optimization will be carried on in future work.

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