An All Silicon Carbide 3kV/540V Series-Resonant Converter for Electric Aircraft Systems

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***Abstract*—In this work, an all silicon carbide (SiC) series-resonant converter (SRC) design is proposed and demonstrate to achieve a single stage dc-to-dc conversion from 3kV to 540V (±270V) for future electric aircraft applications. The proposed SRC consists of a neutral-point-clamped (NPC) converter using 3.3kV SiC MOSFETs on the primary side, a H-bridge converter using 900V SiC MOSFET on the secondary side and a high frequency (HF) transformer. The detailed design methods for the SRC power stage and the HF transformer are presented. Especially, a tradeoff between the complexity for the cooling system and the need for high power density and voltage insulation is addressed in the transformer design, leading to a novel multi-layer winding structure design to enhance the insulation capability and also the mechanical robustness. The proposed bobbin design is realized using additive manufacturing. The detailed analysis and modeling of the parasitic capacitance between sections introduced by fringe electrical field is presented. To validate the effectiveness of the proposed SRC design, a 25kW converter prototype using 3.3kV SiC discrete devices has been developed with a peak efficiency of 99.08% achieved in experimental studies.**

***Index Terms*—SiC MOSFETs, high frequency transformer, series-resonant converter, parasitic capacitance.**

I. INTRODUCTION

THANKS to the advances in the silicon carbide (SiC) technology, SiC devices can withstand higher voltage and operate at higher switching frequency, which can enable a high efficiency single stage conversion from the medium voltage (MV) dc to several-hundred-volt low voltage dc. Many applications, e.g., the data center power supplies and auxiliary power supplies for railway systems and/or electric aircraft, tend to adopt this technology due to the lower complexity, higher efficiency and power density [1].

At present, the more-electric aircraft (MEA) and all-electric aircraft (AEA) [2]-[4] are becoming more and more popular due to high power efficient and environment friendly passenger flight. The low-voltage ac distribution is widely used in today's commercial airlines. The maximum onboard electric power generation capacity in operating commercial airliners is approximately 1 MW on the Boeing 787, which uses ±270V dc, 115~235V ac to supply the ancillary electrical power systems. Recently, Airbus launched a hybrid-electric demonstrator, E-Fan X [5], which features the use of 2 MW electric motors and 3 kV dc electrical distribution. The use of MV dc distribution on an aircraft system can significantly achieve a higher efficiency of the electric power distribution and lightweight due to lower ohmic losses and reduced weight of conducting cables and connectors.

In this paper, the design and demonstration of an isolated single stage 3 kV to 540 V dc/dc converter are presented. This concept can bridge the future 3 kV dc distribution system and the state-of-the-art (SOA) electrical equipment using ±270 V dc. For isolated DC-DC converters, both dual-active bridge (DAB) and series-resonant converters (SRC) are widely used [6]-[8]. Compared with the DAB, the SRC features low turn-off losses, simple operation, and zero-voltage switching (ZVS) for all devices. Therefore, high efficiency of the SRC can still be achieved at a high operating frequency which is the key to reduce the volume of magnetic components. To achieve both high efficiency and high switching frequency, 3.3 kV SiC MOSFETs are used to design an SRC operated at the resonant frequency. To accommodate the 3 kV dc voltage, a neutral-point-clamped (NPC) half-bridge converter [4] is used on the primary side and the dead times of switching devices are carefully designed to achieve ZVS for all MOSFETs.

The high operating frequency and the high terminal voltage pose several challenges for the design of high frequency (HF) MV transformer [24]. Especially the use of thicker insulation layers and the needs to achieve high power density make the thermal management difficult for the transformer. In addition, the partial discharge could a potential issue for the transformer designed to operate in the thin air of 20,000-25,000 ft. Therefore, 3D-printed multi-layer bobbins, which designed to ensure sufficient insulation for the transformer are presented in detail in this paper. Meanwhile, the parasitic capacitance of the transformer brings several problems for the SRC. For example, high winding capacitance gives rise to a high charging current at the input of the transformer and therefore increases the additional losses and peak voltage stress across secondary switching devices [9]. The fringe electrical field, which is usually ignored in previous parasitic capacitance modeling [10]-[13], can introduce additional parasitic capacitance [14]-[17]. In this paper, the parasitic capacitance introduced by fringe electrical field between sections is analyzed using the

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static and dynamical capacitance model and the finite element method (FEM).

This paper is organized as follows: topology and operation principles of the proposed SRC are introduced in section II. The transformer design and parasitic capacitance analysis are introduced in section III, followed by the prototype implementation and experimental studies presented in section IV.

II. MV Serious-Resonant Converter Design

A. MV Converter Design

For isolated DC-DC converters, both dual-active bridge (DAB) and SRC are widely used [18]. A SRC topology is selected for its high efficiency, high power density and the possibility of ZVS for all switching devices. Compared to the DAB converter, SRC features much lower turn-off loss, such that high efficiency can be maintained at high switching frequency, which is the key to reduce the volume of magnetics. The circuit diagram of the proposed SRC is shown in Fig. 1. Since the dc link voltage is 3 kV on the primary side, an NPC half-bridge using 3.3 kV 80 mΩ discrete SiC MOSFETs in TO-247 package is selected. Compared with the 6.5 kV SiC MOSFETs, the 3.3 kV SiC MOSFETs have advantages in costs, packaging availability and technical maturity. Due to the use of half bridge on the primary side, the MV terminal voltage for the transformer is ±1500V. The resonant tank consists of the leakage inductor L_r, the resonant capacitor C_r and the magnetizing inductor L_m. On the secondary side, since the output nominal voltage is 540 V, custom 900V SiC modules with forced air cooling are used. A full-bridge building block is designed for the secondary converter.

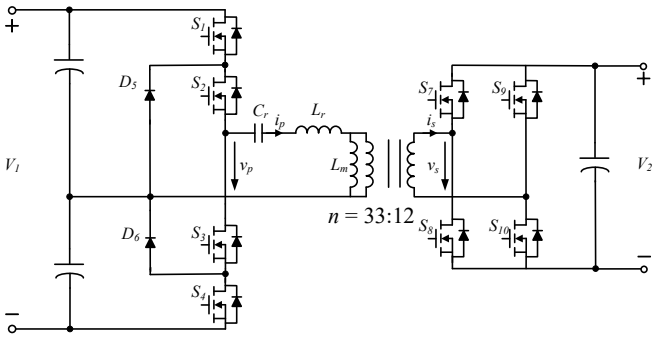


Fig. 1. Circuit diagram of the proposed SRC.

For the SRC, some parameters (e.g. magnetizing inductance, switching frequency and turns ratio) are required to be carefully designed. These detailed parameters are summarized in Table I. The frequency of the SRC depends on the targeted efficiency of the converter and the available losses of switching devices and the transformer. Considering the switching loss characteristics and the transformer's targeted efficiency of 99.5%, the operating frequency of 48 kHz was selected.

TABLE I
KEY PARAMETERS OF THE PROPOSED SRC

Parameter	Specification
Nominal power	25 kW
Operating frequency	48 kHz
Input voltage	3 kV
Output voltage	540 V
Resonant capacitance	184.5 nF
Leakage inductance	59.6 μH
Magnetizing inductance	3.10 mH
Transformer turns ratio	33:12

B. Operating Principles of the SRC

Due to the high switching frequency, the SiC MOSFETs should operate under ZVS conditions to ensure high efficiency. Fig. 2 shows the waveforms of the converter when it operates at the resonant frequency. The converter has six operating modes in a period with details described as follows.

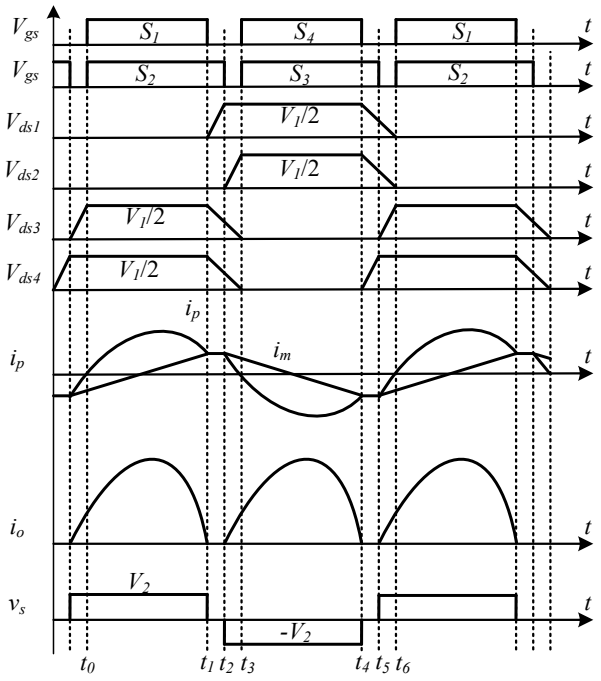


Fig. 2. Theoretical operation waveforms of the proposed SRC.

Mode 1 (t_0 to t_1): This mode starts when the resonant inductor current i_p becomes positive. S_1 and S_2 are both turned on at t_0 and i_p flows through S_1 and S_2 during this mode. S_7 and S_{10} are turned on the secondary side. The L_m is linearly charged with output voltage and the output current i_o is proportional to the difference between i_p and magnetizing current i_m.

Mode 2 (t_1 to t_2): At time instant t_2, i_p and i_m are equal. Meanwhile, i_o decreases to zero and S_7 and S_{10} are turned off. In this mode, the output is disconnected from the transformer, thus L_m becomes a free inductor, which is in series with L_r resonating with C_r. S_1 is turned off, while S_2 is still ON. The drain-to-source voltages of S_3 and S_4 start to decrease and the

drain-to-source voltages of S_1 starts to increase. The primary resonant current i_p freewheels through D_5 and S_1.

Mode 3 (t_2 to t_3): S_2 is turned off at t_3 and i_p flows through the body diodes of S_3 and S_4, which leads to ZVS for S_3 and S_4. In this operating mode, i_p starts to drop. S_8 and S_9 are turned on and i_o begins to rise.

The operation modes 4-6 are similar to mode 1-3 and are not discussed in details here. The analysis shows that ZVS conditions can be achieved for S_1 ~ S_4 and ZCS can be achieved for S_7 ~ S_{10}. In addition, the voltage of the primary MOSFETs are the half of the input dc link voltage V_1.

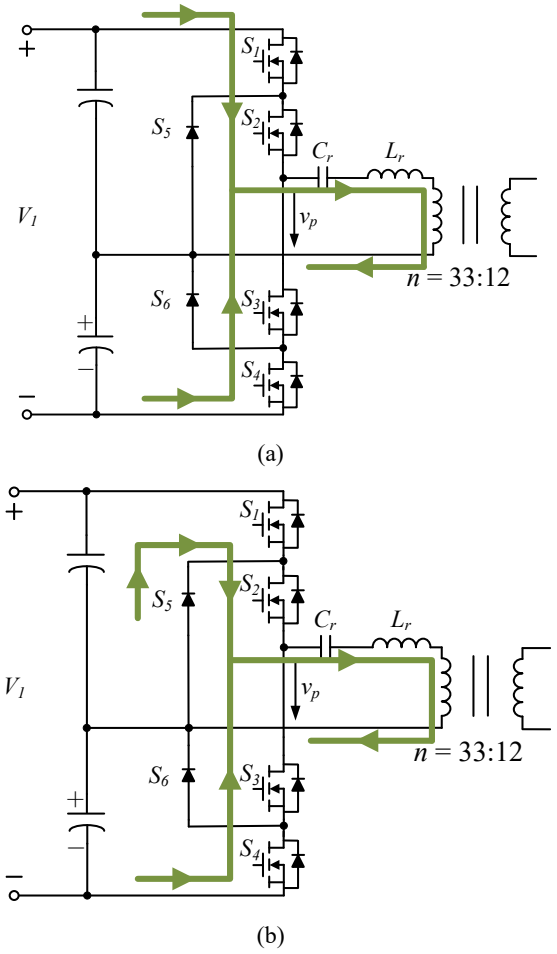


Fig. 3. ZVS operation of the proposed SRC. (a) dead time t_{d3} (t_1~t_2). (b) dead time t_{d2} (t_2~t_3).

C. ZVS Analysis

For the SRC, the dead time is critical to ensure the ZVS condition. Three dead times of the SRC based on the NPC topology are defined as

$$t_{d1} = t_3 - t_1 = t_6 - t_4 \quad (1)$$

$$t_{d2} = t_3 - t_2 = t_6 - t_5 \quad (2)$$

$$t_{d3} = t_2 - t_1 = t_5 - t_4 \quad (3)$$

where t_{d1} is the dead time of S_1 and S_4 and t_{d2} is the dead time of S_2 and S_3. As shown in Fig. 3(a), the output capacitor C_{oss} of S_1 is charged and the C_{oss} of S_3 and S_4 are discharged during the dead time of t_{d3} (t_1~t_2). When the C_{oss} of S_1 is fully charged, S_2 will be turned off and the C_{oss} of S_2 will be charged during the dead time of t_{d2} (t_2~t_3) in Fig. 3(b). At the same time, the C_{oss} of S_3 and S_4 are still discharged and the voltage of S_3 and S_4 will drop from $V_1/4$ to 0. Since the magnetizing inductance L_m is large, the magnetizing current I_m can be constant during the dead time. Therefore, the dead times t_{d1}, t_{d2} and t_{d3} should meet the following Equations to achieve the ZVS condition:

$$I_m t_{d1} \geq 4C_{oss}\frac{V_1}{2} \quad (4)$$

$$I_m t_{d2} \geq C_{oss}\frac{V_1}{2} + 2C_{oss}\left(\frac{V_1}{2} - \frac{V_1}{4}\right) \quad (5)$$

$$I_m t_{d3} \geq C_{oss}\frac{V_1}{2} + 2C_{oss}\frac{V_1}{4} \quad (6)$$

The maximum magnetizing current I_m can be expressed as

$$I_m = \frac{V_1}{8 f_s L_m} \quad (7)$$

where V_{in} is the input voltage and f_s is the resonant frequency. Substituting (7) into (4), (5) and (6), the condition for ZVS can be modified as

$$t_{d1} \geq 16C_{oss} f_s L_m \quad (8)$$

$$t_{d2} \geq 8C_{oss} f_s L_m \quad (9)$$

$$t_{d3} \geq 8C_{oss} f_s L_m \quad (10)$$

III. HF MV Transformer Design

HF MV transformer is one of the critical components in the SRC which provides the galvanic isolation between the primary side and the secondary side. Though numerous designs of HF MV transformers can be found in the existing literature [19]-[21], it is still challenging to design HF MV transformers, especially for high power applications. The insulation layer of the MV transformer is relatively thick to meet the insulation requirement. Meanwhile, the surface area of the transformer is much smaller due to high power density of HF transformer, which poses significant challenges to the thermal management. In other words, high efficiency and high-performance insulation design is critical to the HF MV transformer.

Although higher operating frequency (50-100 kHz) may increase the power density, it could result in much higher core and winding losses. In this work, considering the requirements of high power density, the resonant frequency of the SRC is selected at 48 kHz. In this case, nanocrystalline core is selected due to its low core loss and high operation flux density. The C cores are used in this transformer. Compared with E cores, the use of C cores can lead to a larger exposed area of the windings for the forced convective cooling and an easier construction [8]. The parameters of the transformer are listed in Table II. With the optimized turns ratio, litz wire and winding structure, the total loss of the core and windings are 117.5 W, which leads to a peak efficiency of 99.5%.

Due to the electric potential difference between primary side and secondary side, proper electric insulation material should be placed between these two sets of windings for isolation purpose. The Kapton film has a high insulation performance. However, it is difficult to remove the air from multiple tape layers, thus the partial

discharge is inevitable. Using the Nomex insulation paper can mitigate this issue. However, wrapping the core or windings with thick insulation paper is not easy. In the proposed design, as shown in Fig.4, a multi-layer 3D-printed bobbin is used to enhance the insulation capability and also the mechanical robustness. The solid fulfill of the 3D-printed bobbin also reduces the risk of partial discharge. To achieve better cooling for the windings and the core, the bobbin structure is optimized to allow enhanced airflow.

TABLE II
KEY PARAMETERS OF THE HF TRANSFORMER

Parameter	Specification
Nominal power	25 kW
Operating frequency	48 kHz
Terminal voltages	±1.5 kV/ ±540 V
Turns-ratio	33:12
Primary winding	0.1mm (AWG38) × 900
Secondary winding	0.1mm (AWG38) × 3600
Winding type	Shell-type
Core type	F3CC0125 nanocrystalline
Volume	1.32 L
Efficiency	99.5%

A. Transformer Bobbin Design

Since the terminal voltage across the primary winding is ±1500 V, the insulation between the adjacent layers of the primary winding is required. Meanwhile, the primary and secondary windings need to be isolated due to the large voltage difference between these two sets of windings. Therefore, the thickness of each layer of the bobbin using polyamide (Nylon 12) should meet the insulation requirement. In Fig. 4(a), the multi-layer bobbin consists of bobbin S, P1, P2, P3 and the cover. The bobbin P1, P2 and P3 are for the 3-layer primary winding and the bobbin S is for the secondary winding. As shown in Fig. 4, each layer of the primary and secondary windings is wound on individual 3D-printed bobbins and assembled concentrically. The secondary winding is arranged between the primary winding and the magnetic core. The thickness of bobbin S, P2 and P3 is 1 mm. And the thickness of bobbin P1 and cover is 2 mm. The 6 mm thick barrier are placed in the middle of the surface of bobbin P1, P2 and P3 to separate two sections of the primary winding.

To enhance the cooling performance for the windings and core of the transformer, the geometry structure of the bobbin S is optimized and presented in Fig. 4(b). The secondary winding has a larger loss due to the high current. On the side walls of bobbin S, notches are placed on each side of wall. Meanwhile, the height of the wall is 1 mm larger than the diameter of the litz wire of secondary winding. Therefore, there are a certain clearance between the secondary winding and the bobbin P1, which provides a channel for air to flow through. Similarly, spacers are placed on the inner surface of the bobbin S to separate the core and the bobbin. It allows the air to flow through it and cool down the portion of the magnetic core covered by the bobbin.

The transformer prototype is shown in Fig. 4 (f). It can be seen that the spacer and notch of the bobbin S creates several channels for the forced air cooling. The cover is assembled as the outermost layer of the bobbin, which packaged the windings and provide sufficient insulation between the outer layer of primary winding and the core. The dimensions of the transformer are 125 mm × 120 mm × 88 mm and the volume of the transformer is 1.32 L.

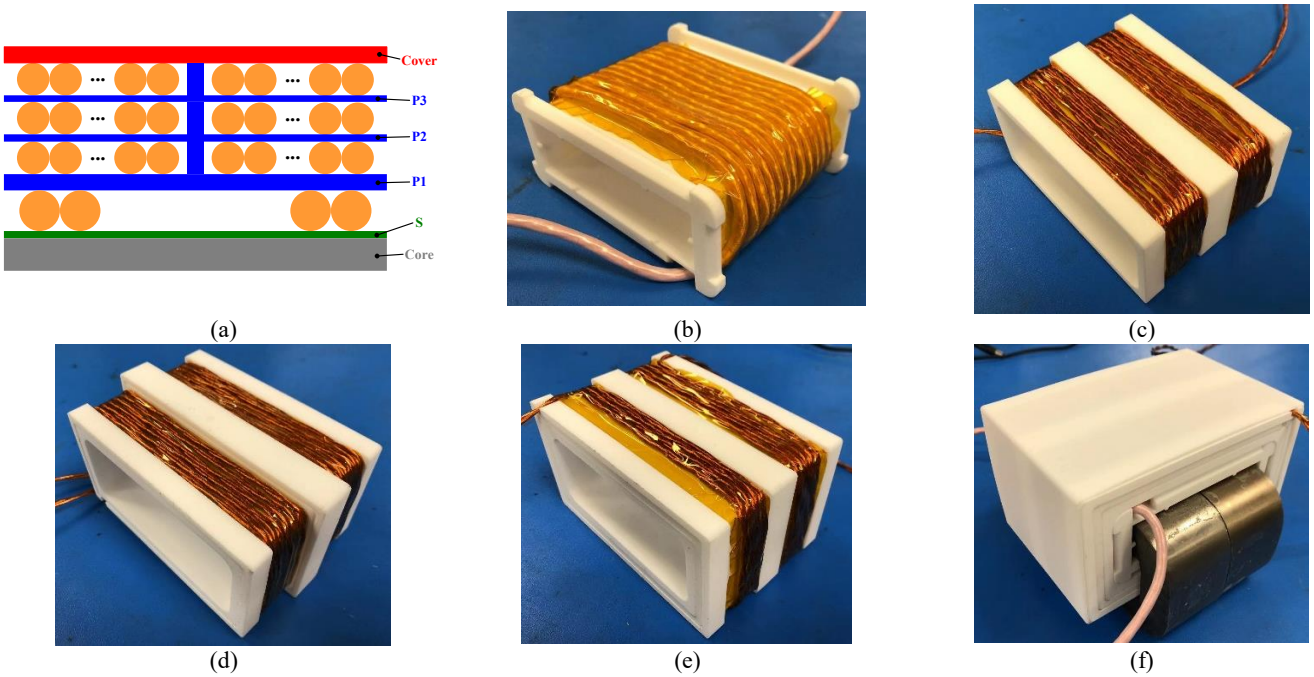


Fig. 4. (a) An illustration of the architecture of the proposed transformer. (b) Secondary winding on bobbin S. (c) First layer of primary winding on bobbin P1. (d) The second layer of primary winding on bobbin P2. (e) The third layer of primary winding on bobbin P3. (f) The prototype of the MV transformer.

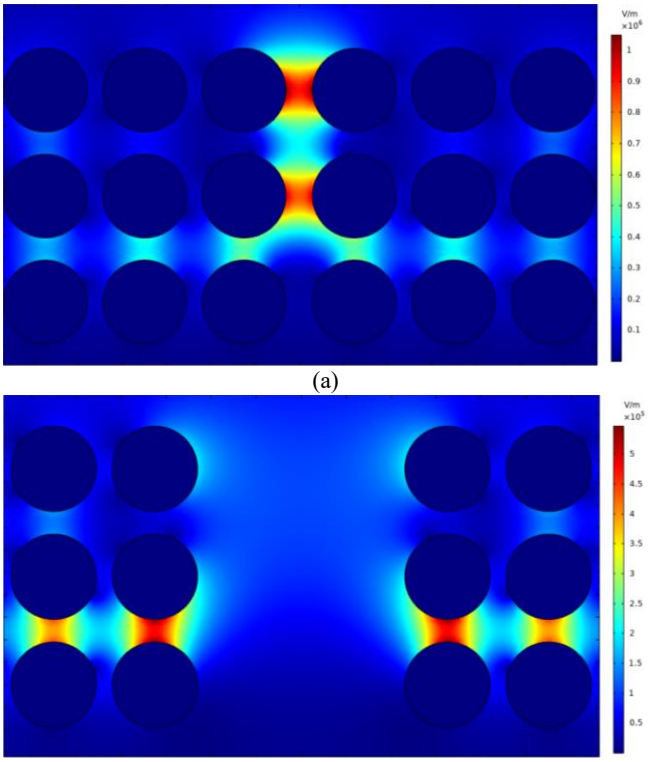


Fig. 5. The FEA simulation of the fringe electric field between two sections vs. bobbin wall thickness l_b between two sections. (a) l_b = 1 mm. (b) l_b = 6 mm.

B. Parasitic Capacitance

High parasitic capacitance of the MV transformer have severe detrimental effect on the voltage regulation and CM noise of the SRC [22]. To achieve high conversion efficiency, the parasitic capacitance needs to be minimized. For the MV transformer, the layer-to-layer capacitance using parallel-plate model can be expressed as

$$C_{LL} = \varepsilon_0 \varepsilon_w \frac{2\pi h_w \left(l_{LM} / (2\pi) \right)}{d_{LL}} \tag{11}$$

where h_W is the height of the winding, l_{LM} is the mean length per turn of the winding, ε_0 is the permittivity of vacuum, ε_w is the permittivity of the wire insulation, and d_{LL} is the effective distance between layers of the winding. And the equivalent capacitance C_W for the complete winding can be calculated by the stored electric field energy in each layer [12]

$$C_W = \frac{4(n-1)}{3n^2} C_{LL} \tag{12}$$

where n is the number of layers. For multi-section windings, the sections are connected in series and the total capacitance C_{MSW} can be presented as

$$C_{MSW} = \frac{1}{N_S} \frac{4(n-1)}{3n^2} C_{LL} \tag{13}$$

where N_S is the number of sections. However, parasitic capacitance between sections caused by fringe electrical field are not negligible [17]. As shown in Fig. 5, the finite element analysis (FEA) simulation results are presented to show the fringe electric field between two sections. In the simulation, the input voltage of the winding is 1500 V with all the turns equally share the voltage. It can be seen that the electrical field strength between two sections can be much larger than that between layers due to a relatively high voltage potential difference.

In Fig. 6(a), the electrical field lines between two sections of the FEA are shown. The electrical field lines flows from one wire to the adjacent wire of the other section. Therefore, the section-to-section capacitance can be obtained by the turn-to-turn capacitance of each layer. The turn-to-turn capacitance with the bobbin is shown in Fig. 6(b). l_b is the thickness of bobbin between sections. r_c and r_t are the radii of the conductor and the wire with coating. θ is the deflection angle.

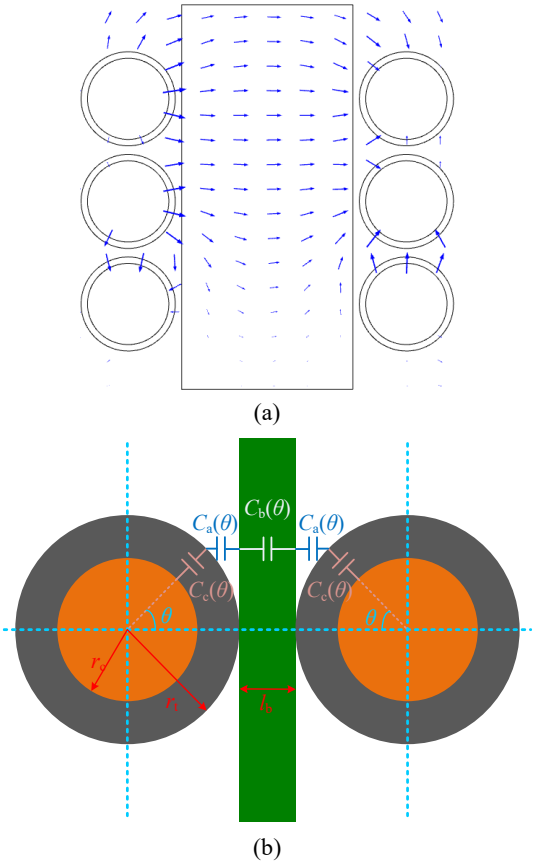


Fig. 6. (a) The electric field line distribution between sections. (b) The static capacitor model of turn-to-turn capacitance.

It can be seen that the turn-to-turn capacitance $C_{tt}(\theta)$ consists of the insulating coating capacitance $C_c(\theta)$, the air capacitance $C_a(\theta)$ and the bobbin capacitance $C_b(\theta)$. These capacitances can be presented as

$$dC_c(\theta) = \frac{\varepsilon_0 \varepsilon_c l_t}{\ln \frac{r_t}{r_c}} d\theta \tag{14}$$

$$dC_a(\theta) = \frac{\varepsilon_0 r_t l_t}{2r_t (1-\cos\theta)} d\theta \tag{15}$$

$$dC_b(\theta) = \frac{\varepsilon_0 \varepsilon_b r_t l_t}{l_b} d\theta \tag{16}$$

where ε_b and ε_c are the permittivity of bobbin and insulating

coating, l_t is the length of turn. The permittivity of each material is shown in Table III. Therefore, the total turn-to-turn capacitance C_{tt} can be calculated by

$$dC_{tt}(\theta)=\frac{1}{2\dfrac{1}{dC_a(\theta)}+\dfrac{1}{dC_b(\theta)}+2\dfrac{1}{dC_c(\theta)}} \tag{17}$$

$$C_{tt}=\int_{-\frac{\pi}{2}}^{\frac{\pi}{2}} dC_{tt}(\theta) \tag{18}$$

The total equivalent capacitance C_{WE} of the winding can be obtained using the stored electrical field energy.

$$\frac{1}{2}C_{WE}U_t^2=\frac{1}{2}C_{MSW}U_t^2+\sum_{i=1}^{n}\frac{1}{2}C_{tt,i}\Delta V_i^2 \tag{19}$$

$$C_{WE}=C_{MSW}+\sum_{i=1}^{n}\frac{\Delta V_i^2}{U_t^2}C_{tt,i} \tag{20}$$

where U_t is the terminal voltage of the winding, n is number of layers, ΔV_i is the voltage potential difference between sections of the layer i and $C_{tt,i}$ is the turn-to-turn capacitance between sections of the layer i.

The second term in (20) represents the equivalent capacitance between sections. It shows that the bobbin wall thickness l_b and the voltage potential difference ΔV_i are the two factors that can reduce the section-to-section capacitance. In Fig. 5, the electrical field strength is dramatically decreased when l_b increases from 1 mm to 6 mm, which causes the decrease of the static capacitance C_{tt} and further decreases the section-to-section capacitance. However, the bobbin wall thickness l_b needs to be carefully designed. There is a tradeoff between the bobbin wall thickness and utilization of window. A low utilization of window will result in a relatively high winding loss or core loss.

TABLE III
RELATIVE PERMITTIVITY OF THE MATERIAL

Parameter	Symbol	Value
The permittivity of the bobbin	ε_b	3.6
The permittivity of the coating	ε_c	3.0

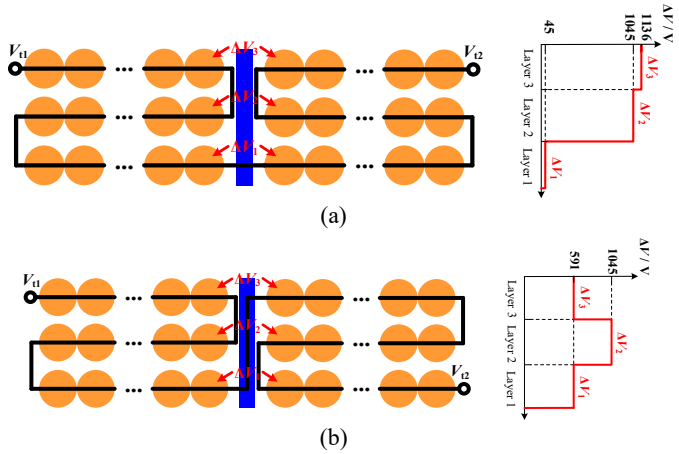


Fig. 7. Winding arrangement and related voltage difference of each layer. (a) The mirror winding arrangement. (b) The parallel winding arrangement.

A proper winding arrangement can also reduce the parasitic capacitance. The mirror and parallel winding arrangement are shown in Fig. 7. Since the electrical field energy associates with the sum of ΔV_i^2, the mirror winding arrangement will store larger electrical field energy than the parallel arrangement. According to the second term in (20), the equivalent capacitance between sections of the parallel winding arrangement can be 25% smaller than that of the mirror winding arrangement in this design.

C. Design Guidelines

Compared with the conventional transformer [12], [23] in Fig. 8, the proposed transformer can achieve lower voltage stress between layers and lower parasitic capacitance. According to (13), the winding parasitic capacitance of the conventional transformer can be N_s times as large as that of the proposed transformer. A large parasitic capacitance of the transformer will give rise to a high charging current at the transformer input, resulting in lower efficiency and increased peak voltage stress across secondary rectifying devices [22]. Since the proposed transformer has two sections, the peak voltage potential difference of the proposed transformer is half of that of the conventional transformer. The lower voltage stress between layers of the proposed transformer decreases the insulation requirements between layers.

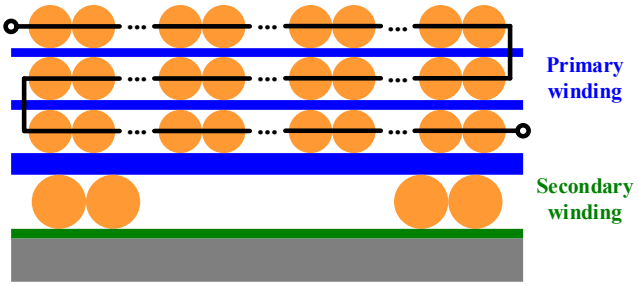


Fig. 8. The structure of the conventional transformer

Additionally, the insulation paper and Kapton tape are widely used insulation materials in the conventional transformers. However, the insulation paper with enough thickness will take significant efforts to wrap the winding. Multiple Kapton tape layers are commonly used to achieve the insulation requirements. The air bubble between tape layers are hard to be eliminated and therefore cause the partial discharge problems. For the proposed multi-layer bobbin, it is easy to wind the wires on the bobbin with good alignment. Since the 3D-printed bobbin is solid, the air in the insulation material is totally eliminated, which mitigates the risk of partial discharge.

To achieve these advantages, the design guidelines for the multi-layer bobbin based transformer are as follows:

1) The thickness of each layer of the bobbin should meet the insulation requirement.
2) To enhance the cooling performance for the windings and core, notches and spacers are designed to provide a channel for air to flow through and cool down the transformer.
3) To decrease the parasitic capacitance of the transformer,

the thickness of the bobbin wall between sections should be carefully designed and the parallel winding structure is preferred.

IV. Converter Prototyping and Experimental Studies

Fig. 9 shows the prototype of the proposed SRC converter for the experimental study. Four films capacitors on the MV side are utilized to hold the 3 kV DC link voltage. The primary converter includes four discrete 3.3kV SiC MOSFETs and two diodes. Two dual-chancel gate drivers are place on top of the main power board to drive the SiC MOSFETs. On the low voltage side, i.e., the secondary side, the H-bridge converter [23] consists of two 900V half bridge SiC modules, a laminated busbar and dc link capacitors. A 0-4 kV programable power supply is connected to the MV side of the converter. The overall test setup is shown in Fig. 10. The hi-pot test has been conducted on the transformer to verify the insulation design. It shows that the insulation of the transformer can withstand a test voltage of 5 kV for an hour. The leakage current is less than 5 μA.

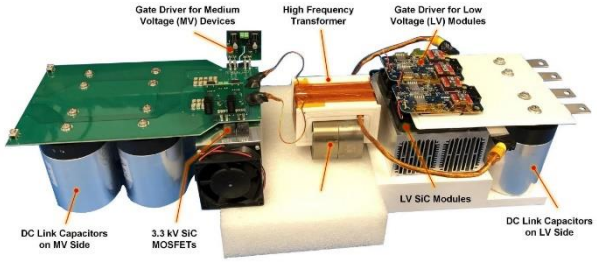


Fig. 9. Prototype of the proposed SRC.

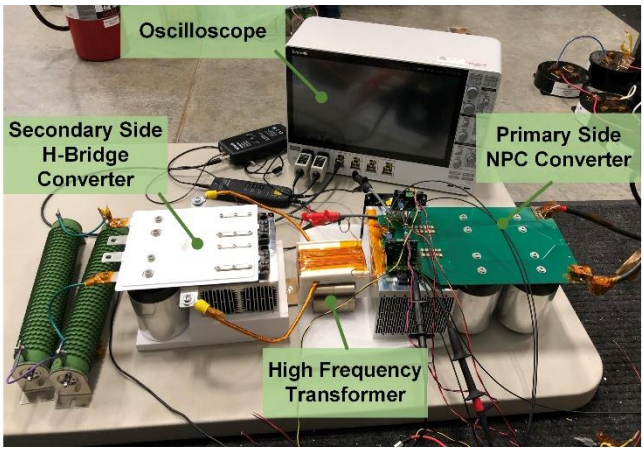
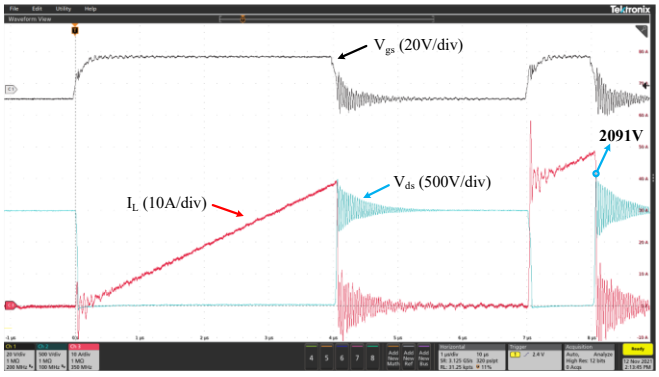


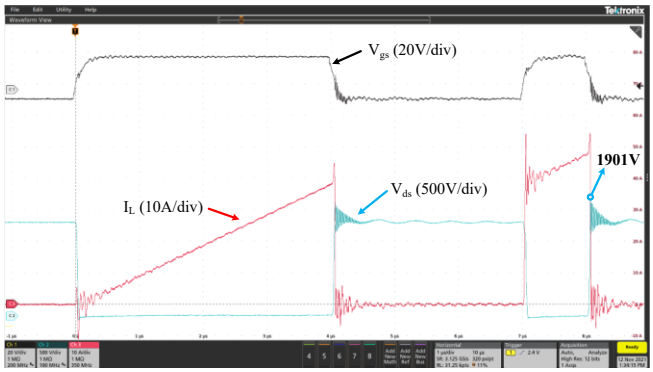
Fig. 10. The experimental test setup.

A. Device Testing Results

The double pulse test (DPT) has been performed to validate the functionality of the gate driver circuit and the main power board design. The results of the DPT using the 3.3 kV SiC MOSFETs are shown in Fig. 11. The DC bus voltage is 1500V, which is the same as the normal operating voltage in the SRC, and the peak inductor current I_L is around 50 A. In Fig. 11(a), it can be observed that the measured maximum drain to source voltage is 2091 V. This relatively high voltage overshoot mainly caused by the due stray inductance of the TO-247 package. The decoupling capacitor can decrease the overshoot voltage and the DPT results with the decoupling capacitance of 0.25 µF are shown in Fig. 11(b). Obviously, the overshoot voltage decreases from 2091 V to 1901 V. However, a low frequency oscillation is introduced on V_{ds} due to the energy conversion between decoupling capacitors and stray inductance in the commutation loop.



(a)



(b)

Fig. 11. The DPT results (a) without and (b) with the decoupling capacitors.

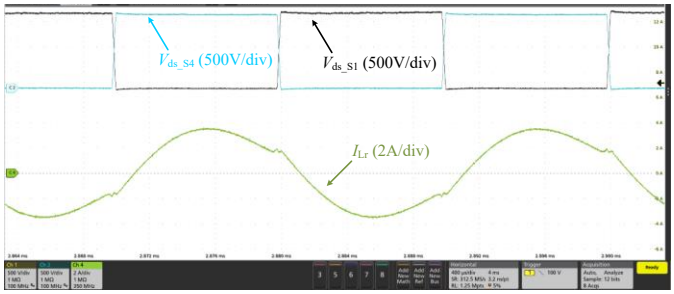


Fig. 12. Measured waveforms of primary side devices voltages and resonant current.

B. Converter Operating Waveforms

To verify the performance of the proposed SRC, such as the ZVS conditions, the voltage waveform of the primary side switching devices and the primary side resonant current waveform are measured. In this test, the converter is operated at the resonant frequency f_0 = 48 kHz with a duty cycle of 0.5. The dead time t_{d3} is set to 800 ns to make sure ZVS can be achieved for the primary side devices. The DC bus voltage of 3 kV is applied. The primary side converter is controlled by the

TABLE IV
CALCULATED LOSSES OF THE CONVERTER AT FULL LOAD

MV converter loss	LV converter loss	Transformer		Capacitor Loss	Total Efficiency
		Winding loss	Core loss		
60.25 W	33.24 W	67.31 W	50.19 W	1.51 W	99.15 %

dSPACE MicroLabBox. A Tektronix oscilloscope with two 6 kV differential voltage probes and a Rogowski coil are used for the measurement. The measured voltage waveforms of the 3.3 kV discrete MOSFETs S1 and S4 and the waveform of the primary side resonant current are shown in Fig. 12. It can be seen that ZVS can be achieved on the primary side MOSFETs. The waveforms are smooth to validate the proper design of the converter. The results illustrate that the resonant frequency is equal to the switching frequency, which means that soft-switching is achieved over the entire load range.

C. Thermal Test and Efficiency Measurement

In the HF transformer design, the cooling of the multi-layer winding is a challenge. Therefore, the short circuit test was performed to measure the winding temperature rise at rated conditions. In this test, the secondary side wind of the HF transformer is shorted and the primary RMS current is equal to current in the full-load condition. Therefore, only the winding losses reach to their maximum value in this operation mode. The system is continuously operated for over an hour until it reaches the thermal equilibrium. The thermal image at the steady state is presented in Fig. 13. It can be seen that the temperature of the winding is much higher than that of the core during the test. The hot-spot on the winding of the HF transformer is 75.4 ℃.

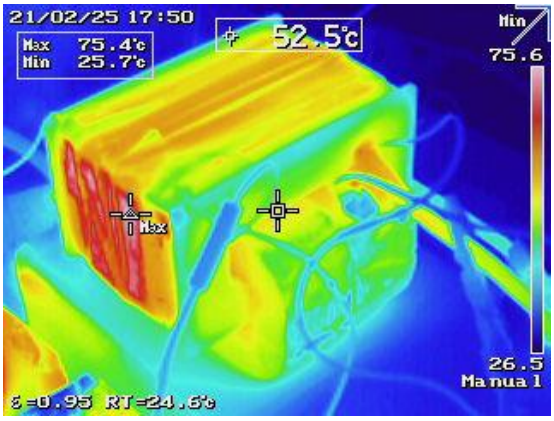


Fig. 13. Thermal image of the HF transformer in the short circuit test.

In addition, the efficiencies of the SRC converter with different loads are measured and the efficiency curve is shown in Fig. 14. It can be observed is that the system efficiency can go beyond 99.0% in the medium to heavy load range, e.g., 50% ~ 100%, with a peak efficiency of 99.08%. In Table IV, the calculated losses of the converter at full load are listed. Due to a relative high MV side on-state resistance of 80 mΩ, the MV converter loss is higher than the LV converter loss. The calculated efficiency at full load is 99.15%, which match very well with the measured efficiency.

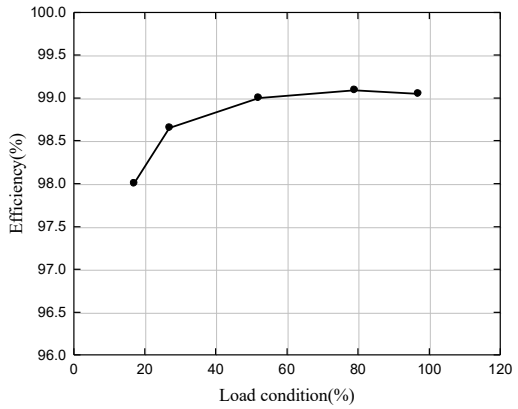


Fig. 14. Measured efficiencies of the SRC prototype.

D. Parasitic Capacitance

According to (20) and the geometry of the transformer, the parasitic capacitances can be calculated. In Table V, the calculated and measured parasitic capacitances are listed. The parasitic capacitances are measured by Bode 100 to verify the calculation of the parasitic capacitance. The core is floating in the measurement. The calculated and measured impedance are shown in Fig. 15. The errors of calculations using the proposed method are 5.4 %.

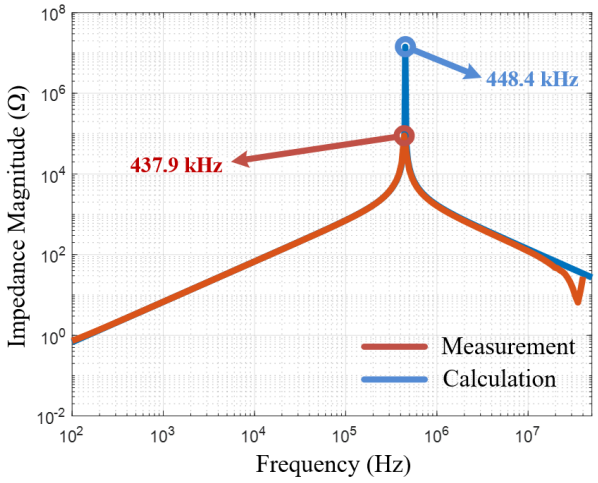


Fig. 15. The calculated and measured impedance.

TABLE V
PARASITIC CAPACITANCE OF THE HF TRANSFORMER

Winding capacitance	Section-to-section capacitance	Layer to core capacitance	Total calculated capacitance	Measured capacitance
36.11 pF	3.23 pF	0.38 pF	39.72 pF	41.99 pF

V. Conclusion

In this work, a 25 kW, 48 kHz all SiC SRC design is presented to achieve a single stage dc to dc conversion from 3kV to 540V (±270V) for future electric aircraft applications. The design of the converter power stage and HF MV transformer were presented. The dead time of the NPC topology is analyzed to achieve ZVS conditions. The 3-D printed multi-layer bobbins are designed to enhance the insulation capability and also the mechanical robustness, which mitigates the risk of partial discharge. The modeling and analysis of the parasitic capacitance of the windings are presented for a more accurate model. The parasitic capacitance between sections introduced by fringe electrical field have been identified. The 25 kW prototype of the proposed SRC is built, and the experimental waveforms show that the SRC can achieve ZVS for all switches. The experimental results also proved that the SRC can achieve an overall efficiency around 99% and verified the proposed model for parasitic capacitance.

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