Design and Demonstration of a Medium-Voltage Silicon Carbide ANPC Power Stage

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***Abstract*—In this paper, the design of a high-power medium-voltage (MV) active-neutral-point-clamped (ANPC) converter using the 1.7kV silicon carbide (SiC) MOSFET modules is presented. How to achieve a low stray inductance design while meeting voltage insulation requirements are the challenges addressed in this work through the use of a three-dimensional (3D) busbar design approach. In addition, various resonant frequency measurement methods are investigated, leading to an accurate current commutation loop inductance extraction from the voltage ringing of the device. Experimental studies are performed using two ANPC power stages in a pump-back configuration to verify the performance of the proposed design.**

Keywords—ANPC Converter, Busbar, SiC MOSFET, Stray inductance

I. INTRODUCTION

Compared to the conventional two-level (2-L) converters, the three-level (3-L) active-neutral-point-clamped (ANPC) converters are widely used in high-power medium voltage (MV) applications, due to their distinctive merits, such as lower blocking voltage required for the devices, higher power quality, and evenly loss distribution among switches [1]-[3]. Recently, thanks to the advancement of the silicon carbide (SiC) technology, the SiC MOSFETs, which have faster switching speed and lower switching loss compared to their silicon counterparts, are available for the MV applications. To develop a SiC based high power ANPC converter, instead of using the printed circuit board based bussing, copper busbars are commonly used to carry high current while keeping an acceptable temperature rise.

The fast switching transient of the SiC MOSFETs can lead to a high voltage overshoot across the switches, due to the large stray inductance in the current commutation loop (CCL) of the 3-L converter. To address this issue, the CCL stray inductance should be minimized for a 3-L converter, which is much difficult to accomplish compared to the 2-L inverter. For low voltage ANPC, e.g., when DC bus voltage is less than 1 kV, the CCL stray inductance in a high power 3-L converter can be lower than 20nH [3]. However, when DC bus voltage goes beyond 1.5kV, the CCL stray inductance can be much larger, e.g., around 115nH for the large commutation loop [4]-[10]. As a result, the low stray inductance busbar design while meeting voltage insulation requirements is still desired for the SiC based MV ANPC converter. In this work, the design of a 150kVA single phase ANPC converter power stage is presented, which has a low-inductance bussing structure and can withstand up to 2.6kV on the DC link. Detailed design considerations for the converter are discussed.

To validate the design of the converter, the inductance extraction of the CCLs is normally made for either 3-L DC-AC inverters [3]-[12] or other converter topologies [13]-[17]. The CCL inductance is usually calculated according to the frequency of the voltage oscillation across the device during its switching transient. However, accuracy of the oscillation frequency measurement has rarely been discussed, which however determines the accuracy of the stray inductance measurement. In this work, an accurate voltage oscillation frequency measurement is proposed for stray inductance extraction. The measurement method is validated through the comparison between the experimentally calculated inductances versus the results extracted from the simulation. In the end, additional testing results are presented to demonstrate the effectiveness of the proposed design.

II. ANPC CONVERTER DESIGN

The design of a single phase ANPC converter power stage is studied in this work, as shown in Fig. 1(a), consisting of six switching positions. The operating principle of the topology and the two CCLs has been well explained in [3] and [11], which are not repeated here. As shown in Fig. 1(a), the small loop of the CCLs is represented by the dashed blue line, while the large loop is labeled with the dashed brown line.

A. Component Selection and Overall Layout

The form factor and foot print of the components are critical for the converter design, since it determines the busbar complexity and the converter power density. In the proposed ANPC converter design, to be able to support 2.6kV DC-link voltage, the voltage blocking ability of each device should be larger than 1.3kV. As a result, the 1.7 kV SiC MOSFET modules HT-3234 [19] from CREE Wolfspeed are used in this work, which is in half bridge configuration (HB), as shown in Fig. 2. Four film capacitors with each rated at 1500V and 195uF were used to form the capacitor bank on the DC-link. The selection of capacitors is essential for the CCL stray inductance, converter power density and etc.

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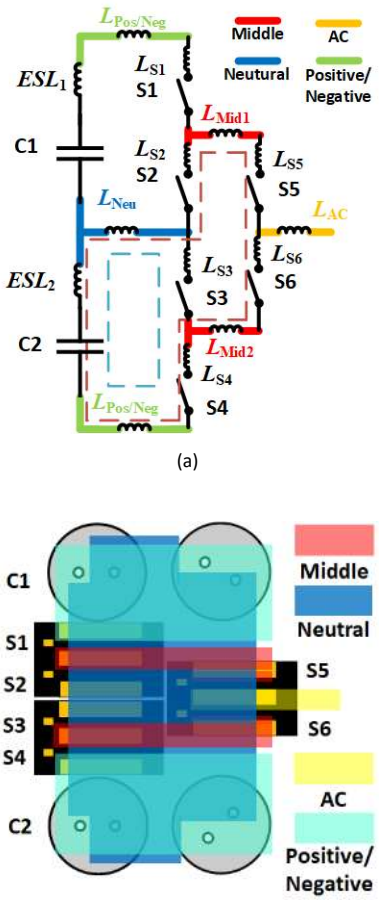

Fig. 1. A single phase ANPC converter (a) the schematic highlighted with CCLs and parasitic inductances; (b) the diagram of the busbar architecture with power modules and capacitors.

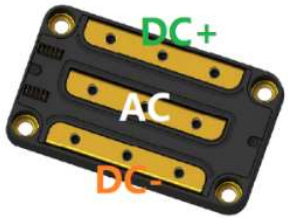

Fig. 2. The package of the HT-3234 power module

The overall diagram of the proposed ANPC power stage, including the modules, busbars, and capacitors, is shown in Fig. 1(b), where the metal planes with different voltage levels in the bussing structure are color coded, corresponding to the electrical connections shown in Fig. 1 (a).

B. Insulation Implementation

To meet the voltage insulation requirements, the thickness of the polyethylene terephthalate (PET) film between the two stacked layers of busbar is 0.5 mm, while 0.25 mm thick PET films are applied to the exterior surface of the busbar. With 60 kV/mm dielectric strength, the 0.25 mm and 0.5 mm thick PET films are capable to withstand 15 kV and 30 kV voltages, fulfilling the insulation requirement of the design. As shown in Fig. 3(a), spacers are used in this work to provide low inductance contact between the busbars, the capacitors, and

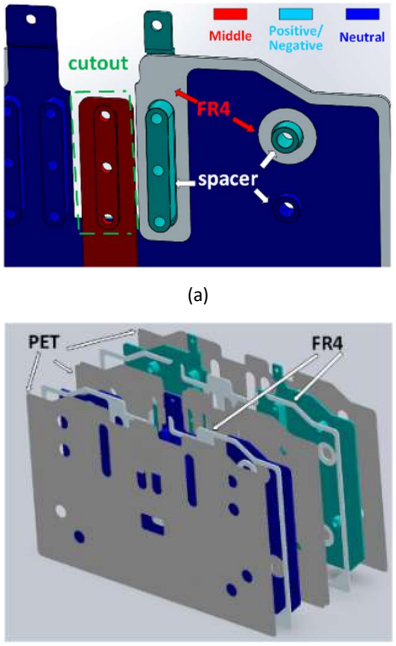

Fig. 3. The insulation considerations (a) between metal plates and spacers and (b) between metal plates and for the edges of the busbar

the modules. For the distances between the spacers, both creepage distance and clearance distance should be satisfied. According to [20], for pollution degree 2, material group III condition, a minimum 13 mm should be maintained between the terminals with 1.3 kV, and 26 mm should be kept for 2.6 kV. For the insulation between metal plates and the spacers, cutouts are needed on the metal plates, as shown in Fig. 3(a). These cutouts, however, influence the current distribution and lead to higher stray inductance. On the edges of the busbars, FR4 is also applied for sealing. The overall insulation implementation is illustrated in Fig. 3(b).

C. Stray Inductance Reduction

A conventional busbar design is shown in Fig. 4 (a), where all the planes are laminated into a single bussing structure. In this design, S5 and S6 are in one HB module, whose DC+ and DC− terminals are connected to the AC terminals of the other two modules, the diagram of which is shown in Fig. 1(b). Since the AC terminal of the HT-3234 module is located between DC+ and DC−, the overlap area between the Positive/Negative and Neutral planes will be reduced if it is necessary to bolt the Middle plane down to the module from the top. This can significantly increase the stray inductance due to the large cutout given by the insulation requirement. The busbar stray inductance on the small loop is 13.1 nH at 10 MHz in this design, based on the simulation results in Q3D.

To reduce the stray inductance, a 3D bussing architecture [9], [17] is utilized in this ANPC design. As shown in Fig. 4(b), there are two separated bussing structures. The busbar on top is formed by the Neutral plane and the Positive/Negative planes, which are laminated into one structure. The spacers are used to lift it up, such that the other busbar at the bottom, composed by the Middle planes and the AC plane, can be bolted down to the modules. In this way, the Middle plane is connected to the module without affecting the lamination areas between the Neutral and Positive/Negative planes. As a

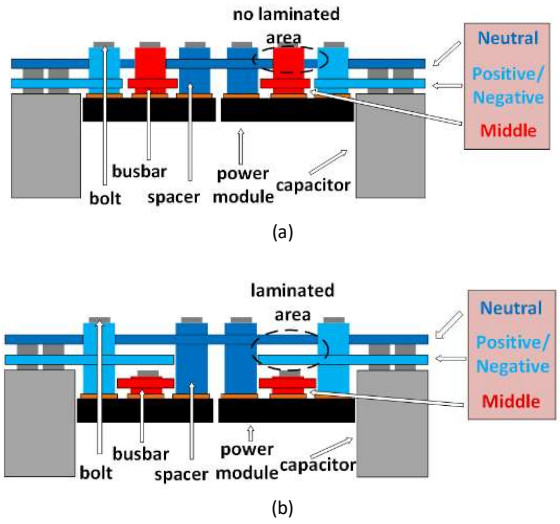

Fig. 4. The cross-sectional views of (a) the conventional design and (b) the proposed design.

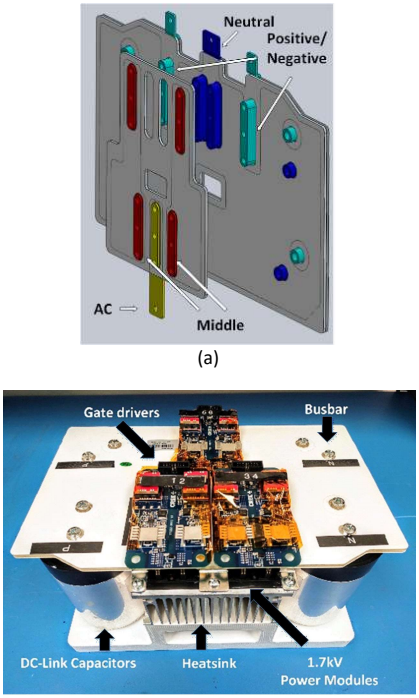

Fig. 5. The proposed ANPC converter design (a) the exploit view of the 3D busbar model; (b) the picture for the power stage.

result, the 3D busbar design can effectively reduce the stray inductance. The stray inductance on the small loop of the proposed design is 7.3 nH at 10 MHz, according to simulation, which shows over 40% reduction compared to the conventional design. The 3D model of the proposed busbars and the power stage of the ANPC converter are shown in Fig. 5(a) and (b).

III. Simulation and Experimental Studies

A. CCL Inductance Analysis

The stray inductances of the busbar are extracted using Q3D based on the model of the fabricated busbars. The inductance of the busbars on the small loop is 9 nH, while the one on the large loop is 27 nH. The measured ESL of each capacitor, using impedance analyzer E4990A, is 17.32 nH. The measured inductance of the power module from the terminal DC+ to terminal DC- is 6.98 nH and inductance from AC to DC− is 7.49 nH. As a result, the total inductances on the small and large loops are calculated as 24.64 nH and 57.62 nH.

B. Experimental Studies

The stray inductance of the CCLs can be extracted based on the waveform of the devices during their switching transient [13]:

$$L_s = \frac{1}{4\pi^2 C_{oss} f_r^2} \tag{1}$$

where L_s is the stray inductance of the CCLs, f_r is the frequency of the voltage ringing, and C_{oss} is the output capacitance of the turn off device on the CCLs.

Usually, the f_r is estimated based on the period of the first cycle of the voltage ringing [3], [17], which however can lead to underestimated f_r and thus resulting in higher calculated stray inductances. For instance, using the method presented in [3] and [17], the calculated inductances from experiments in are 20.0% and 10.9% larger than the simulated results. In contrast, the switching frequency f_r, extracted by applying fast Fourie transform (FFT) over several fundamental cycles of the voltage ringing can lead to more accurate stray inductance calculation. In [12], the calculated inductances from the experiment, based on the f_r derived from multiple waves, are only 2.8% and 7.3% smaller than the simulation values.

Therefore, the ring frequency f_r is extracted based on the FFT of multiple waves to calculate the stray inductance in this work. Fig. 6(a) shows the equivalent circuit of the double pulse test (DPT) for the small loop, where S4 is switching. The corresponding voltage waveform of S4 is shown in Fig. 6(b), where the C2 voltage is 1000V and inductor load current is 400A. Using FFT, the frequency of the drain to source voltage of S4 is 25.71 MHz. With the output capacitance of the device being 1.67 nF at 1000 V, the total inductance in the small loop is 25.71 nH. Similarly, Fig. 6(c) shows the equivalent circuit of the DPT for the large loop, where S6 is switching. The corresponding DPT waveform of S6 at 1kV 400A condition is shown in Fig. 6(d). The calculated frequency of the drain to source voltage of S6 is 16.67 MHz. Thus, the total inductance in the large loop is 54.58 nH. The CCL inductances calculated from DPT are very close to the simulation results. In comparison, the switching frequencies extracted from the first wave of the oscillations in two DPTs are 18.49 MHz and 12.87 MHz, which results in much larger stray inductances, 44.37 nH and 91.57 nH. The results from the simulations and the experiments are listed in Table I.

TABLE I Comparison of Stray Inductance Obtained from Simulation and Experimental Waveforms

CCL	Calculated Stray Inductance		
	Q3D Simulation	***FFT over 8+ fundamental cycles***	***Calculated based on 1st fundamental cycle***
small loop	24.64 nH	25.71 nH	44.37 nH
large loop	57.62 nH	54.58 nH	91.57 nH

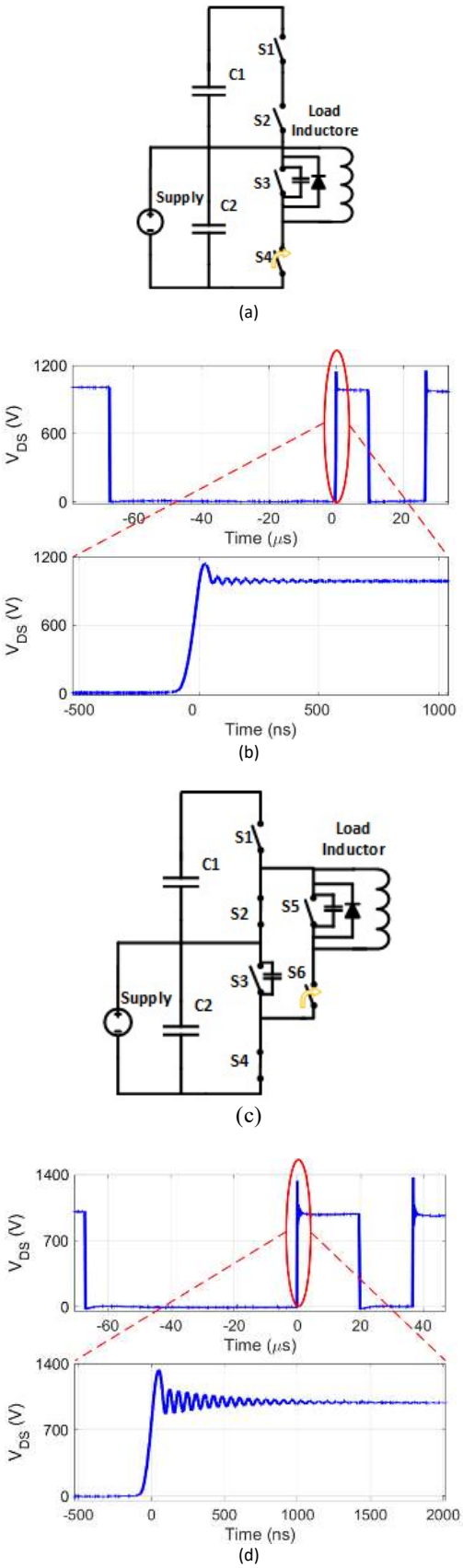

Fig. 6. The devices on the proposed converter under DPT (a) the test circuit of S4; (b) the turn off waveform of S4; (c) the test circuit of S6; (d) the turn off waveform of S6.

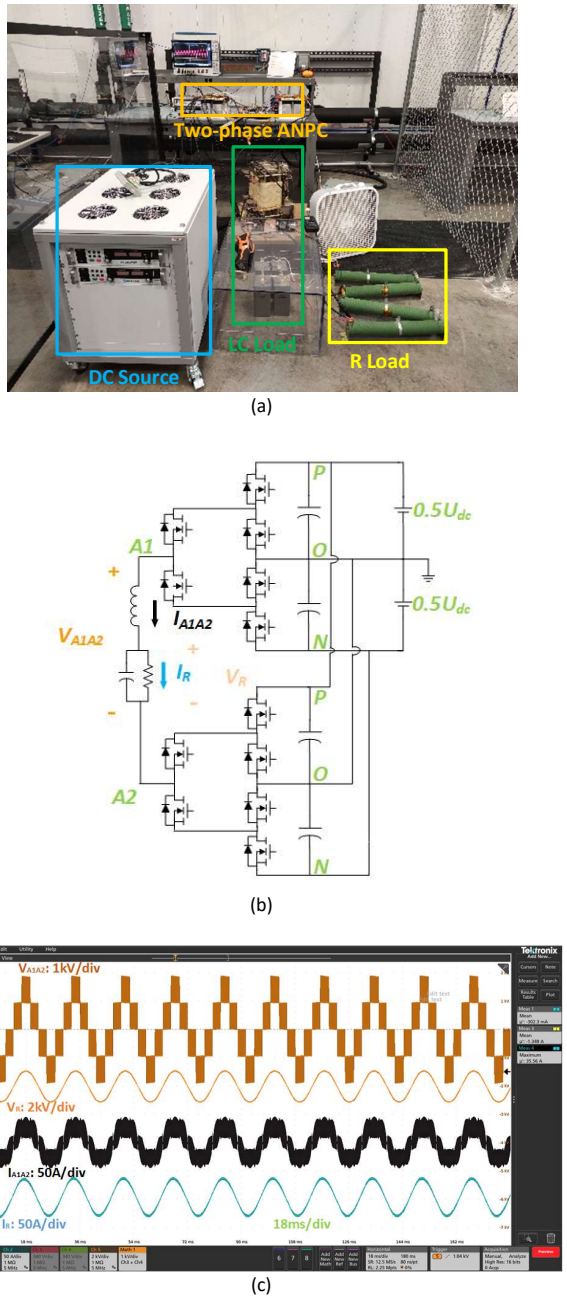

Fig. 7. Experimental study of the ANPC power stage (a) the test setup of the pump-back test using two ANPC power stage; (b) the diagram of the pump-back test; (c) the experimental waveforms of the pump-back test.

Experimental studies using two ANPC power stages are also performed to validate the effectiveness of the design under continuous operation. As shown in Fig. 7(a) and (b), the pump-back test using two ANPC power stages to drive the RLC load is performed. A typical result with 1900V DC bus and 0.6 modulation index is shown in Fig. 6(c). The switching frequency of the devices is 20 kHz, and the line frequency is 60 Hz.

IV. CONCLUSION

The design of 150 kVA MV ANPC converter is presented. The DC link capacitor and power switch are selected specifically to realize the compact struct with high DC bus voltage in this design. The insulation is implemented

considering the different requirements for spacers and metal plates. The stray inductances of the busbars are reduced by applying a 3-D bussing architecture. In this way, the design for a low loop inductance MV 3-L converter can be achieved, with 25.71 nH and 54.58 nH for stray inductances on small loop and large loop. One method for the accurate inductance extraction is proposed. The inductance calculated based on the proposed method is in good alignment with the simulation results. The continuous test validates the performance of the designed ANPC power stage.

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