Fiber-Array-to-Chip Interconnections With Sub-Micron Placement Accuracy via Self-Aligning Chiplets

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Abstract—A self-aligning silicon chiplet approach is used on a silicon-on-insulator (SOI) substrate with ridge waveguides and grating couplers to enable interconnection with arrays of fibers. The approach is enabled by silicon micromachining and 3D printing, achieving highly scalable surface coupling of optical fibers to the gratings at repeatable sub-micron placement accuracies. The coupling efficiency relative to that of active fiber alignment at 1550 nm is 79%. Insertion points for 160 fibers across four chiplets are demonstrated. The design, fabrication and assembly processes together provide a potential technology for fiber-to-chip interconnects.

Index Terms—Optical interconnections, optical fiber coupling, passive alignment, chiplets array.

I. Introduction

THE increasing demand for higher bandwidth has driven the large-scale employment of optical interconnects in modern data centers and in high-performance computers [1]. These optical interconnects are currently penetrating down from mid-board level to the chip level in the vicinity of processing units, meeting the requirements of low-loss signal transmission with lower latency and higher bandwidth, while providing compatibility with on-chip optical networks [2].

In general, fibers may be coupled to chips by surface coupling, edge coupling, or free-form optics [3], [4], [5], [6]. The state of the art of these coupling approaches is summarized in Table I. Edge coupling typically relies on inverse tapers for mode conversion, offering relative low coupling loss with a wide spectral bandwidth; however, the tapers are limited to the edges of chip and occupy a relatively large area and are further hindered by stringent requirements on alignment, as well as facet and fiber polishing. The free-form micro-optics can achieve low-loss coupling with broad bandwidth, but the fabrication is costly and difficult to scale-up. In contrast, surface coupling methods can access the entire wafer area and have ease of scaling to higher densities [6]. However, to accomplish high coupling efficiency, it is still necessary to achieve sub-micron-level placement accuracy.

TABLE I
COMPARISON OF MAJOR FIBER-TO-CHIP COUPLING METHODS

Coupling Approach	Coupling Loss (dB)	3-dB Bandwidth (nm)	Alignment Tolerance for 1-dB Penalty (μm)	Reference
Free-form Optics	0.5	>300	2.2	Yu, 2021 [3]
Edge Coupler	1.81	120	<1	He, 2021 [4]
Surface Coupler (Apodized)	2.5	75	7.5	Zhang, 2020 [5]
Surface Coupler (Dual-band)	5.2	56	N.A.	Gonzalez-Andrade, 2020 [6]

In the present work, to solve the alignment problem associated with surface coupling, a Fiber-Interconnect Silicon Chiplets Technology (FISCT), together with the Positive Self-Aligned Structures (PSAS) is used [7], [8]. With an aim toward fiber interconnections across an entire chip, the alignment design and fabrication processes demonstrated here potentially enable scaling to > 100 fibers on a set of 2 × 2 chiplets.

II. Device Structure

As shown in Fig. 1, the FISCT is mounted on an SOI photonic integrated circuit (PIC) where fan-out grating couplers connected to ridge waveguides couple signals from single-mode SMF-28 fibers. The precise placement of an optical fiber relative to a grating coupler is enabled by three mechanical interfaces: 1) the PSAS spherical domes of thermally reflowed photoresist on the PICs that match with the inverse-pyramid pits etched on the bottom of the carrier die [7], 2) the through-holes in the carrier die that accept the 3D-printed ferrules, and 3) the cylindrical holes in the printed ferrule that accommodate the optical fibers. The first interface can correct initial misalignment up to 10 μm [7], while the other two interfaces anchor the placement in sub-micron level.

In this design approach, the number of ferrules can be scaled up to accommodate larger numbers of optical interconnects on

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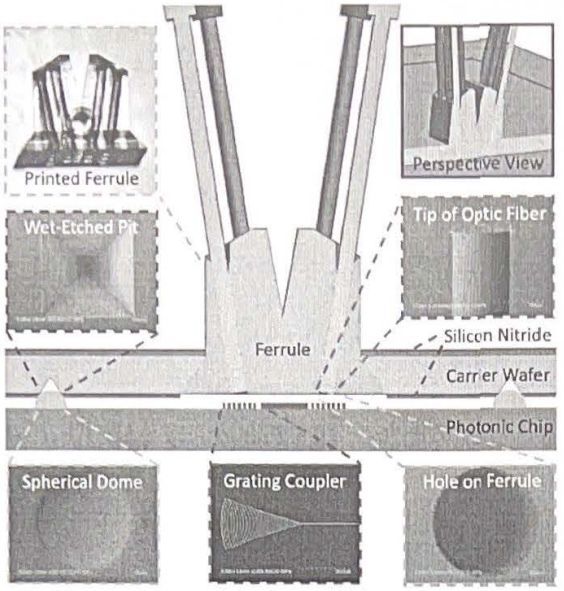

Fig. 1. Cross-sectional view of the FISCT and PSAS structures with microscopic images of the individual components.

a single die. In the present work, to increase the density of interconnects further, five pairs of fiber holes are arranged in a close-packed manner in each ferrule. Accordingly, five pairs of grating couplers are placed in an array on the photonic chip.

III. Fabrication and Assembly

The FISCT is fabricated based on the methods previously developed in [8]. The device layer of grating couplers and ridge waveguides is patterned on 220 nm-thick Si of SOI by electron-beam lithography (EBL) using negative-resist hydrogen silsequioxane and a writing resolution of about 10 nm.

The carrier die is first coated with a 200 nm-thick silicon nitride layer as an etch stop. Then, mask-less photolithography at a resolution of 0.5 μm is used to define 1) the through-holes for ferrule and 2) the alignment pits for the re-flowed domes. The nitride layer is opened by an RIE step, followed by a wet-etch in KOH bath at 90 ° C to form the geometry of the through-holes and the alignment pits.

The ferrule is fabricated by 3D-printing using two-photon lithography. A printing resolution of 200 nm is enabled by the Nanoscribe™ instrument with the IP-S photoresist. The printing is performed on Indium Tin Oxide (ITO) coated glass, followed by development in SU-8 solution for 30 minutes.

To investigate how the coupling efficiency is affected by offset and misalignment, vernier marks are included on the top surface of the photonic chip and on the bottom surface of the carrier. Vernier marks with resolutions of 2 μm, 1 μm, and 0.5 μm are placed on all four edges. The markers on the carrier die are patterned on the nitride layer by positive EBL with poly-methylmethacrylate (PMMA) before the patterning of the openings for wet-etching. The pattern is shallow-etched into the nitride layer which has a remaining thickness of about 120 nm as a protective layer for marker areas from wet-etching. The vernier marks on the device layer, however, are fabricated on the silicon layer along with the fabrication of grating couplers in the same EBL step.

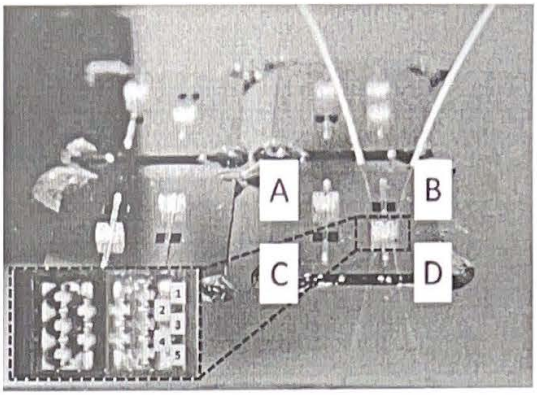

Fig. 2. Assembled 2 x 2 array of chiplets for testing the fiber-array-to-chip optical interconnection. Within each chiplet, four pit locations are available (labeled with letters), each providing 10 fiber-insertion points. Inset: top-view of a single ferrule with numbers indicating the locations of the 5 pairs of fiber-insertion-holes.

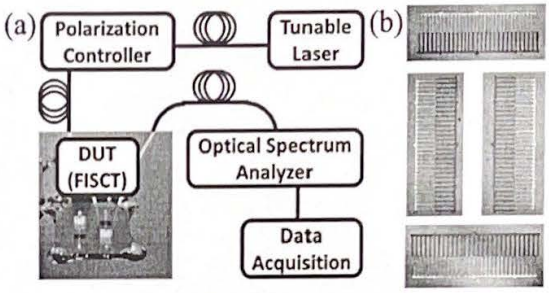

Fig. 3. a) Schematic of the configuration for optical loss measurement (DUT can be FISCT or PIC alone for active benchmark). b) Typical infrared microscopic images of alignment markers placed on four edges of assembled dice, showing sub-micron level placement accuracy.

The domes for alignment are fabricated by reflowing thick AZ40 photoresist. This photoresist is patterned at a resolution of 0.5 μm and reflowed on a hot plate at 120 °C for 60 seconds. With all of the components fabricated as shown in Fig. 1, the FISCT is assembled after dicing of the carrier wafer into small dice by a diamond cutter. The FISCT assemblies achieved with 2 x 2 dice are shown in Fig. 2, where the carrier dice are secured on the PIC by epoxy.

IV. Testing and Results

The optical test configuration is shown in the block diagram of Fig. 3(a). The laser provides a 2.5 dBm output at a wavelength of 1550 nm. The polarization controller is used to maintain TE polarization (parallel to photonic chip surface) at the end of optical fiber on top of device layer. The optical signal intensity data is collected by optical spectrum analyzer connected to a desktop computer.

Before the optical loss of the assembled FISCT is measured, a benchmark test is performed device-by-device with the same

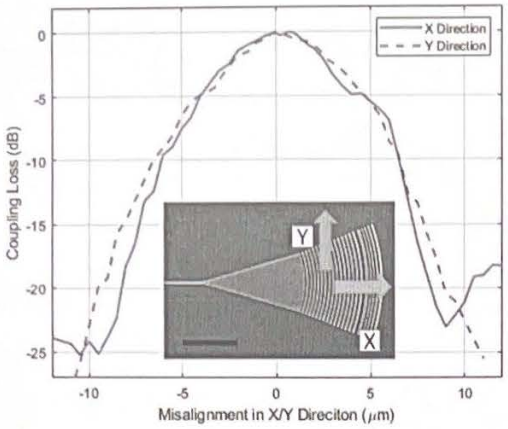

Fig. 4. Benchmark measurement of coupling loss as a function of fiber-to-grating coupler alignment. Inset: direction of optical fiber misalignment relative to grating coupler.

TABLE II

DIE-LEVEL MISALIGNMENT VALUES AS MEASURED BY THE VERNIER MARKERS ON THE ASSEMBLED FOUR DICE

Die Location	Misalignment of Die Placement in Microns			
	Top Edge	Left Edge	Bottom Edge	Right Edge
Top-left	+1	<+1	+1	<+1
Top-right	+0.5	0	0	<|-1|
Bottom-left	0	-1	0	<|-1|
Bottom-right	+0.5	0	+0.5	<+0.5

overall measurement configuration, but now with an active alignment stage with 3-axis positioning accurate to 0.25 μm. As a benchmark, the output signal intensity of the grating coupler devices was first characterized with intentional offsets in all X, Y, and Z axis from the optimum location where the grating coupler lies in the X-Y plane, and the ridge waveguides are parallel to the X direction.

Typical benchmark results are plotted in Fig. 4, where 3 dB loss (50%) of signal intensity corresponds to about $\pm$ 2.5 μm of misalignment in either the X- or Y-directions, while an offset of $\pm$ 7 μm in either the X- or Y- directions results in a 10 dB loss (10%) relative to that of the optimum location. These are comparable to state-of-the-art loss values as discussed earlier. The performance from device to device is consistent for the grating couplers fabricated in the same batch. The system error of the benchmark measurement is approximately $\pm$ 0.1 dB.

For the actual assembled FISCT structure, offset values of every grating coupler were determined based on its known coordinates and from the readings of vernier marks with an infrared microscope. As shown in Table II, the die-to-die alignment on the four edges of every one of the 2 $\times$ 2 carrier dice on the PIC are all controlled to within $\pm$1 micron, demonstrating the successful design, fabrication, and assembly of the FISCT. Besides, the placement accuracy can be further improved in the fabrication process.

Because of the precise alignment of the carrier die to the PIC and the accurate 3D printing, the alignment of the fibers to the grating couplers are controlled at the sub-micron level. This is supported by optical testing with the assembled FISCT, which achieved a low coupling loss of −0.1 dB (79%), relative to that of the optimal result from the active alignment benchmark.

TABLE III

COUPLING EFFICIENCY OF THE FISCT WITH VARIOUS MISALIGNMENTS

Location	Measured Misalignment (μm)		Induced Offset (μm)		Net Misalignment (μm)		Coupling Loss (dB)
	X_M	Y_M	X_I	Y_I	X_N	Y_N	S
D2	-0.5	-1	+1	+1	+0.5	0	-0.10
A3	+0.5	0	0	0	+0.5	0	-0.44
B2	+0.5	-1	0	+2	+0.5	+1	-0.52
D3	-0.5	-1	0	0	-0.5	-1	-0.57

Because the coupling efficiency is greatly affected by alignment accuracy at the sub-micron level, we investigated this relationship further by manually introducing intentional offsets into the positions of the device patterns relative to the optical fiber, and then determining the correlation between the coupling loss and the misalignment value. The results are shown in Table III. These data are labeled with letters indicating the ferrule locations and numbers indicating the locations of fiber-insertion holes within the ferrule (as shown in Fig. 2). With the misalignment value increasing from half a micron to nearly 1 micron, the optical loss, S, increases gradually from −0.1 dB to −0.5 dB. This trend is consistent with the data recorded in the active alignment benchmark.

V. CONCLUSION

In summary, this work has proposed and demonstrated a highly scalable self-alignment structure for efficient surface coupling of fibers to a PIC. This enables the interconnection of arrays of optical fibers across multiple chiplets with more than 100 fiber-insertion points. Due to well-controlled fabrication procedures, this technology achieves optical coupling efficiencies comparable to those of active alignment, thus making it a potential solution for reliable and flexible fiber-array-to-chip interconnects.

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