Breakthrough Short Circuit Robustness Demonstrated in Vertical GaN Fin JFET

R. Zhang, *Student Member, IEEE*, J. Liu, *Student Member, IEEE*, Q. Li, *Member, IEEE*, S. Pidaparthi, A. Edwards, C. Drowley, *Senior Member, IEEE*, and Y. Zhang, *Member, IEEE*

***Abstract*- Insufficient short-circuit (SC) robustness of currently commercial GaN power devices, i.e., the high electron mobility transistors (HEMTs), is a key roadblock for their applications in automotive powertrains. At a 400 V bus voltage (V_{BUS}), the SC withstanding time (t_{SC}) of commercial GaN HEMTs is typically below 1 µs, far below the usual system requirement (>10 µs). This work presents breakthrough short-circuit capability in a vertical GaN fin-channel junction-gate field-effect transistor (Fin-JFET). The Fin-JFET is normally-off with a 0.7 mΩ·cm² specific on-resistance and 800 V avalanche breakdown voltage (BV_{AVA}) at the room temperature. The gate driver in the short-circuit test was designed to be identical to that in device switching applications. The t_{SC} of GaN Fin-JFETs was measured to be 30.5 µs at a V_{BUS} of 400 V, 17.0 µs at 600 V, and 11.6 µs at 800 V, all among the longest reported for 600-700 V normally-off transistors. In addition, GaN Fin-JFETs failed open in these tests and retained BV_{AVA} after failure, which is highly desirable for system applications. In the repetitive 10 µs, 400 V short-circuit tests, GaN Fin-JFETs showed no degradation after 30,000 cycles. Furthermore, to the best of our knowledge, this is the first report of a power transistor with good short-circuit ruggedness at a bus voltage close to its BV_{AVA}. The underlying mechanism is the unique avalanche-through-fin in the Fin-JFET, which is validated by mixed-mode TCAD simulations and unclamped inductive switching tests. These results reveal the inherent ruggedness of GaN Fin-JFETs in the concurrent presence of short-circuit and overvoltage in power electronics systems.[1]**

***Key words* – GaN, FinFET, JFET, short circuit, robustness**

I. Introduction

Short-circuit robustness is a key application requirement for power devices, particularly in automotive powertrains, motor drives, electric grids, and circuit breakers. In these systems, when short-circuit events occur, power devices must withstand an abnormally high current before protection circuits intervene, which typically takes at least ~10 µs [1], [2]. According to the U. S. Department of Energy 2025 Vehicle Drive Roadmap [3], even with ultrafast protection circuits added to gate drivers (which may increase system cost and complexity), the short-circuit withstanding time (t_{SC}) of power devices is required to exceed 2 µs. For power transistors, the hard-switching (or type I) short-circuit condition is usually employed to evaluate the device robustness, where the device is required to withstand an abnormally high current while sustaining the bus voltage (V_{BUS}) in power converters [1].

GaN power devices have been commercialized up to the 650-V class based on the lateral high-electron-mobility transistor (HEMT) structure. GaN HEMTs have been found to possess a limited capability to withstand short circuit. The reported t_{SC} of all types of commercial 600/650-V GaN HEMTs is below 1 µs at the 400 V V_{BUS} in electric vehicle (EV) powertrain inverters [2], [4]. This weak ruggedness has become a roadblock for the penetration of current GaN devices into the EV powertrain market, and more fundamentally, it raises the concern if GaN devices with different designs are generically susceptible to short circuit events in power converters.

Extensive efforts are being made to improve the short-circuit robustness of GaN power devices, and almost all these efforts still build on the HEMT device architecture. Recently, Transphorm [5] and Samsung [6] reported a t_{SC} of 3 µs and 10 µs, respectively, in their R&D GaN HEMTs. However, their ruggedness in repetitive short-circuit events was not reported. Meanwhile, t_{SC} has been found to seriously deteriorate under repetitive stresses for some GaN HEMTs [7].

This work reports breakthrough short-circuit robustness demonstrated in a distinct GaN transistor, the vertical GaN fin-channel junction-gate field-effect transistor (Fin-JFET). This device leverages the benefits of sub-micrometer fin channels, e.g., high channel density, superior gate control, and normally-off operation [8], and those of p-n junctions, e.g., avalanche capability [9] and high-temperature operation [10]. Particularly, the fin channel in GaN can exploit the depletion effect of the sidewall gate stack while maintaining good transport properties [8], [11], thus making it easier to realize the normally-off JFETs as compared to the SiC counterpart [10].

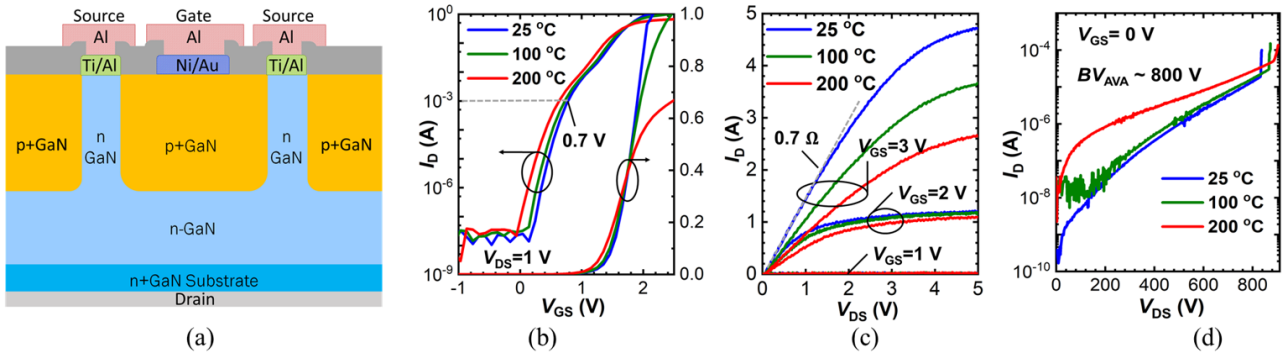
In this work, we present the following major results of the short-circuit capability of GaN Fin-JFETs: (a) a record t_{SC} of 30.5 µs at V_{BUS} = 400 V, (b) a failure-to-open signature where the device maintains the avalanche breakdown voltage (BV_{AVA}) after failure, (c) no degradation after 30,000 cycles of repetitive 10 µs short-circuit stresses at 400 V, and (d) a unique short-circuit capability at the device BV_{AVA} with t_{SC} > 10 µs.

II. Device Characterization and Test Set-ups

Fig. 1(a) shows a schematic of the vertical GaN Fin-JFET fabricated on 100-mm GaN substrates. The device is a NexGen design manufactured in its New York fabrication facility. The devices under test (DUT) in this study are 650-V class GaN Fin-

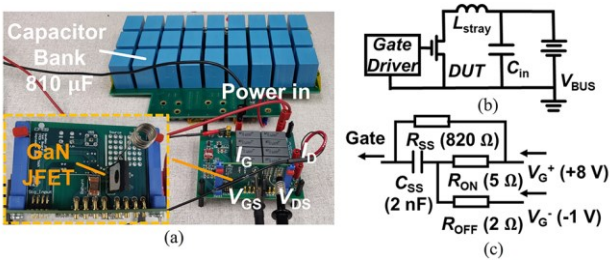
R. Zhang, J. Liu, J. Liu, and Y. Zhang are with the Center for Power Electronics Systems (CPES), Virginia Polytechnic Institute and State University, Blacksburg, VA 24060 USA (email: yhzhang@vt.edu).

S. Pidaparthi, A. Edwards, and C. Drowley are with the NexGen Power Systems Inc, Santa Clara, CA 95051 USA (e-mail: cliff@nexgenpowersystems.com).



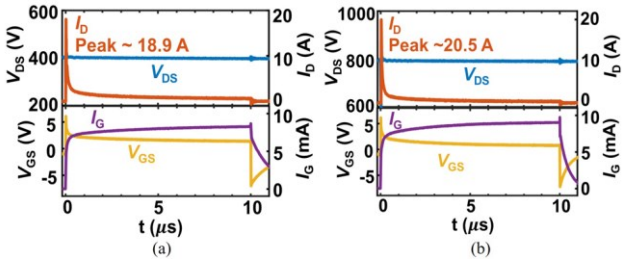
(a) (b) (c) (d)

Fig. 1. (a) Cross-section schematic of the vertical GaN Fin-JFET (not to scale) tested in this work. (b) Transfer and (c) output characteristics of the DUT at 25, 100 and 200 °C. R_{ON} is 0.7 Ω in the linear region at V_{GS}=3 V, 25 °C. (d) Off-state I_D-V_{DS} characteristics at 25, 100 and 200 °C, all measured at V_{GS} = 0 V. The avalanche breakdown voltage is ~800 V at 25 °C.



(a) (b) (c)

Fig. 2. (a) Photo of the test setup. (b) Short circuit test circuit diagram (L_{stray} ~ 48 nH). (c) Circuit diagram of the *RC* gate-drive network.



(a) (b)

Fig. 3. Typical 10 µs short-circuit test waveforms of GaN Fin-JFETs at a V_{BUS} of (a) 400 V and (b) 800 V. DUTs survived both tests and showed no degradation after each test. The peak I_D is around 20 A in the SC tests.

JFETs; the structure is similar to the 1.2-kV Fin-JFET described in [9], [10], except for a thinner, more-highly-doped drift region. The JFET has an array of 1 µm high n-GaN fin channels in a p^+-GaN gate-all-around structure. Total active device area is 0.1 mm^2. The DUTs are assembled in TO-247 packages.

Fig. 1(b) and (c) show the DUT's transfer and output characteristics, respectively, measured at temperatures of 25 °C, 100 °C and 200 °C. A threshold voltage (V_{th}) of 0.7 V was extracted at a drain current (I_D) of 1 mA. At a gate-to-source voltage (V_{GS}) of 3 V, the on-resistance is 0.7 Ω (a specific R_{ON} of 0.7 mΩ·cm^2) at 25 °C, and it increases to 1 Ω at 125 °C and 1.3 Ω at 200 °C. At a V_{GS} of 3 V and a drain-to-source voltage (V_{DS}) of 5 V, the saturation current ($I_{D,SAT}$) is 4.7 A at 25 °C and reduces quickly at higher temperatures (e.g., 2.6 A at 200 °C). This $I_{D,SAT}$ reduction is favorable for realizing high short-circuit robustness. Fig. 1(d) shows the DUT's off-state I-V curves at temperatures from 25 °C to 200 °C, revealing a non-destructive BV_{AVA} of ~800 V with a positive temperature coefficient.

To best mimic the type I short-circuit in EV powertrains, our test setup (Fig. 2(a)) has several design features: (a) a V_{BUS} of 400-V or higher, stabilized by a 810 µF capacitor bank; (b) a high slew rate (*di/dt*) enabled by the low stray inductance of the circuit board (Fig. 2(b)), which mimics the shoot through in power systems; (c) an *RC*-interface gate driving circuit (Fig. 2(c)), which is identical to that used for the DUT's switching operations [9]. This driver is similar to that used for GaN gate injection transistor [12], and it allows the device to operate in the current driven mode. In the gate driver, *C*ss provides a large capacitive gate current (I_G) for fast switching, and a large R_{SS} is used to suppress static I_G and reduce driver loss. The DUT's V_{GS} and V_{DS} were measured by two high-bandwidth passive probes (1 GHz and 500 MHz). I_D was measured by a 30 A current probe (TCP0030A) or a 600 A Rogowski coil (CWTUM/3/B). I_G was calculated from the measured voltage across R_{SS}.

III. Single and Repetitive Short-Circuit Tests

Single-event and repetitive short-circuit tests of GaN Fin-JFETs were performed at the V_{BUS} increased from 400 V up to the DUT's BV_{AVA} (800 V). At least three DUTs were tested for each condition, and good consistency was observed in all tests. All DUTs survived the 10 µs tests at different V_{BUS} with no degradations. Fig. 3 shows the 10 µs test waveforms at V_{BUS} of 400 V and 800 V. A fast turn-on was enabled by the driving circuit (I_D rises to ~20 A in ~20 ns), followed by a large I_D reduction (>10X) due to elevated junction temperatures (T_j), accompanied by an I_G increase and V_{GS} decrease. This $I_{D,SAT}$ reduction with T_j is more pronounced than that in GaN HEMTs, which is the key enablers of the superior short-circuit capability of Fin-JFETs. This strong $I_{D,SAT}$ reduction can be attributed to:
(a) the negative temperature coefficient of bulk GaN mobility;
(b) high T_j facilitating the hole injection in the gate-to-source (G-S) p-n junction, resulting in an increase in I_G and the voltage across R_{SS}, thus reducing the device V_{GS};
(c) the reduction in the knee voltage (V_{knee}), which can be modeled by [13].

$$V_{knee} \approx \frac{qN_{Fin}W_{Fin}^2}{8\varepsilon} + V_{GS} - \frac{kT_j}{q}\ln\left(\frac{N_{Fin}N_A}{n_i^2}\right) \quad (1)$$

where N_{Fin} and W_{Fin} are the doping concentration and width of the fin channel, N_A is the ionized acceptor concentration in p-GaN, and n_i is the intrinsic carrier concentration. At high T_j, V_{knee} decreases due to the reduced V_{GS} and increased N_A [as the

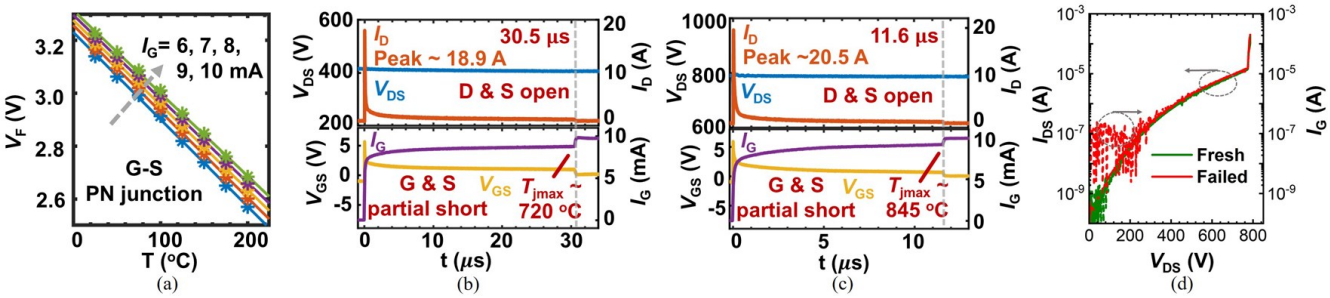


Fig. 4. (a) Forward voltage versus temperature of the gate-source p-n junction at I_G = 6 ~ 10 mA measured at 25 to 200 °C. A linear fit is shown for each I_G. (b) The DUT's short-circuit failure waveforms measured at the V_{BUS} of (b) 400 V and (c) 800 V; the t_{SC} and estimated max T_j are also marked. (d) Off-state I-V characteristics of the fresh and failed DUTs. The I_D-V_{DS} and BV_{AVA} in the blocking state remain the same, and I_G at low V_{DS} is higher in the failed DUT.

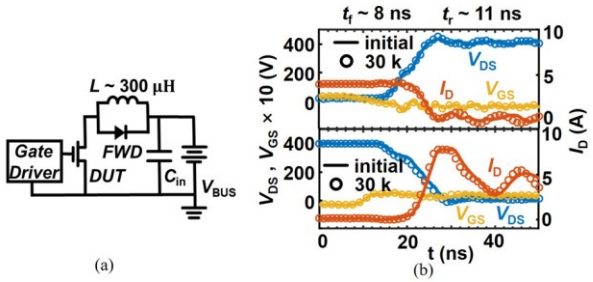


Fig. 5. (a) DPT test setup. (b) Turn-off and turn-on switching waveforms in the 400 V / 4 A DPT for the DUT before and after 30,000 cycles of 400 V, 10 µs short circuit stress, revealing no degradations in the DUT.

acceptor (magnesium) energy is relatively deep in GaN]. The decreased V_{knee} leads to an early saturation and a lower $I_{D,SAT}$.

The forward voltage (V_F) of the G-S p-n junction, i.e., V_{GS} at a specific I_G, shows a good linear relation with T_j in the GaN Fin-JFET. This linear relationship was modeled in [14] for the GaN p-n junction, and the V_F was used as an electrical measure for T_j [15]. Fig. 4(a) shows linear fittings for V_F versus T_j at various I_G from 6 mA to 10 mA, allowing construction of a lookup table for T_j estimation based on any set of (I_G, V_{GS}). This lookup table was used to estimate T_j in the short-circuit process using the (I_G, V_{GS}) extracted from the waveform.

DUTs were tested to failure at different V_{BUS}, and a t_{SC} of 30.5 µs was measured at 400 V (Fig. 4(b)), 17.0 µs at 600 V and 11.6 µs at 800 V (i.e., the BV_{AVA} at 25 °C) (Fig. 4(c)). The estimated T_j at failure is 740~845 °C, suggesting the good crystal quality of GaN. Upon failure, V_{DS} showed no change; I_D and V_{GS} dropped to zero; and I_G increased. These behaviors imply a drain-to-source (D-S) open and G-S partial shorting. This signature was confirmed by static characterizations of the failed DUT (Fig. 4(d)), in which BV_{AVA} was retained. This failure-to-open signature is highly desirable in system applications, as the failed device still blocks voltage, retaining system functionality in the case of parallel devices or multi-chip modules [16].

Repetitive short-circuit tests were performed with 10 µs t_{SC}, 400 V V_{BUS}, and a 3 s pulse period for DUT cooling. The short-circuit energy in each cycle is ~7.5 mJ, yielding a power dissipation of 2.5 mW. No T_j build-up was observed using thermal camera imaging. Double pulse tests (DPT) were performed before and after 30,000 short-circuit cycles (25 hours). Fig. 5(a) shows the DPT test circuit based on the same board as the short-circuit test, which uses the same gate driver and adds a 300 µH inductor and a freewheeling diode (IDH02G120C5). As shown in Fig. 5(b), the DUT's 400 V/4 A switching waveforms exhibited no change after the repetitive short-circuit stresses. No shifts of major device parameters (e.g., BV_{AVA}, V_{TH}) were observed in static characterizations as well.

IV. Short-Circuit Near Avalanche Breakdown

The short-circuit capability at a bus voltage close to BV_{AVA} has not been reported previously. To understand this unique feature of GaN Fin-JFETs, we performed physics-based, electrothermal, mixed-mode TCAD simulations in Silvaco. The device avalanche models are similar to those described in [9], [17], the electrothermal models are based on [18], and impact ionization coefficients are extracted from [19]. The key material

TABLE I. KEY MODELS IN THE ELECTRO-THERMAL SIMULATION

Parameter	Simulation Model
GaN electron mobility ($cm^2 \cdot V^{-1} \cdot s^{-1}$)	Drift layer: $800\times(T_L/300)^{-1.25}$ Substrate: $100\times(T_L/300)^{-1.25}$
GaN k_T ($W \cdot cm^{-1} \cdot K^{-1}$)	$2\times(T_L/300)^{-1.3}$
Thermal resistance ($W \cdot cm^{-2} \cdot K^{-1}$)	Top surface: 2 Bottom surface: 0.1
Impact ionization coefficients (cm^{-1})	Electron: $4.48\times10^8\times\exp(-3.39\times10^7/E)$ Hole: $7.13\times10^8\times\exp(-1.46\times10^7/E)$

T_L: lattice temperature (in Kelvin); E: electric field.

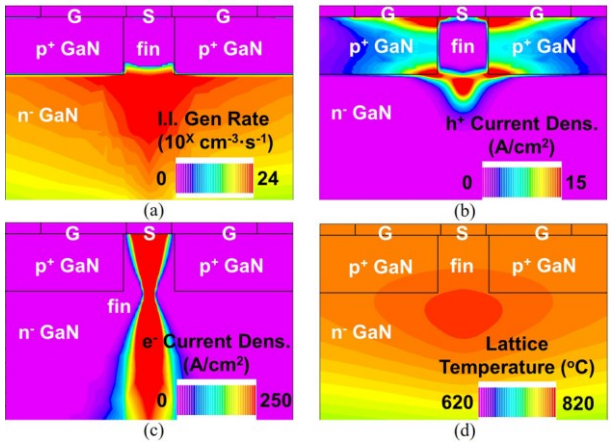


Fig. 6. Simulated contours of (a) the impact ionization generation rate, (b) hole current density, (c) electron current density, and (d) lattice temperature at the t = 11 µs transient in the 800 V short circuit condition.

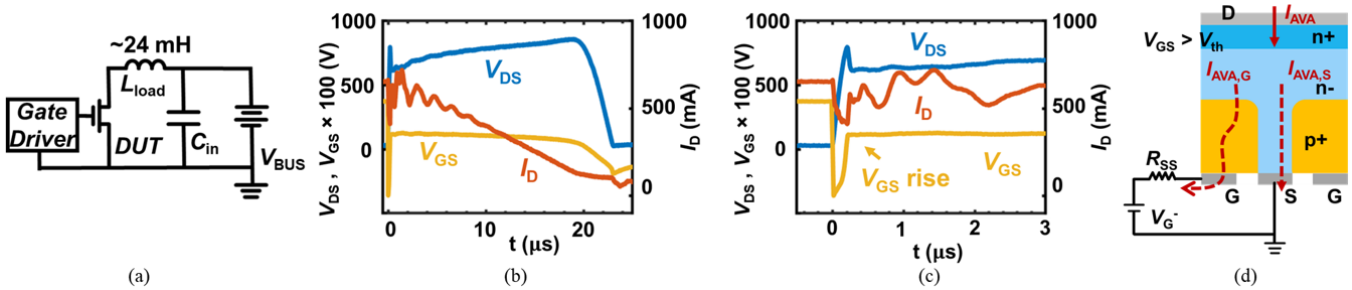


Fig. 7. (a) Circuit diagram of the UIS test. (b) Tested UIS waveform of the GaN Fin-JFET, avalanche energy is ~ 5 mJ. (c) Zoom-in waveform in the first 3 µs. V_{GS} first drops to V_G-, then rises to V_{th}, turning on the fin channel. (d) Illustration of the avalanche-through-fin process in the UIS test with the *RC* gate driver.

models are detailed in Table I. The circuit in the simulation is the same as the short-circuit experiment. The simulation was able to replicate the measured experimental waveforms.

In the simulated short-circuit transient at 800 V (t = 11 µs), the impact ionization (I. I.) generation rate was found to peak at the foot of the fin channel (Fig. 6(a)). The holes generated in the I. I. are removed via the p-GaN gate (Fig. 6(b)), and these holes also facilitate electrons to be pumped from the source to recombine with them (Fig. 6(c)). This produces an "avalanche-through-fin" phenomenon that could accommodate a large I_D flowing through the fin channel into the drift region. As shown in Fig. 6(d), the simulated peak T_j is located at the foot of the fin with a magnitude similar to our prior estimations using (I_G, V_{GS}), suggesting that the DUT fails due to the G-S junction degradation under high electrothermal stress in the concurrent presence of avalanche and short-circuit.

The simulation results can also help understand the quick drop of $I_{D,SAT}$ in GaN Fin-JFETs under the short-circuit stress. At high V_{BUS}, the depletion region expansion results in the narrowing of the current path. The location of peak T_j coincided with that of the narrowest current path, leading to a fast decrease in the carrier mobility. As a result, $I_{D,SAT}$ and the resulted thermal stress on GaN Fin-JFETs were suppressed, leading to a long t_{SC}.

To further validate the "avalanche-through-fin" process, we performed the unclamped inductive switching (UIS) tests using the same *RC* gate driver (Fig. 7(a)). The UIS test is widely used for evaluating device avalanche capability [9], [17], [20], [21]. Compared to the short-circuit test at a fixed bus voltage, the UIS test enables the device to maintain avalanching at its BV_{AVA}, which may increase with the elevated T_j.

As shown in Fig. 7(b), the DUT shows avalanche waveforms in the UIS test. V_{DS} clamps at BV_{AVA}, which increases due to T_j climbing, and I_D reduces to zero. As shown in Fig. 7(c), during the first 0.2 µs after the DUT turns OFF, V_{GS} first drops to negative values and then rises to the device V_{th}, turning on the fin channel. The corresponding physical process is illustrated in Fig. 7 (d). When avalanche begins, the avalanche current (I_{AVA}) first goes through the gate and R_{SS} (820 Ω), lifting V_{GS} due to the voltage drop on R_{SS} until $V_{GS} > V_{th}$, turning on the fin channel. I_{AVA} then transfers from the gate to the fin channel, initiating the avalanche through fin, which further dominates the entire avalanche process. This UIS test verifies that GaN Fin-JFETs can continuously accommodate a considerable I_{AVA} through the fin channel at the device BV_{AVA} that increases with T_j.

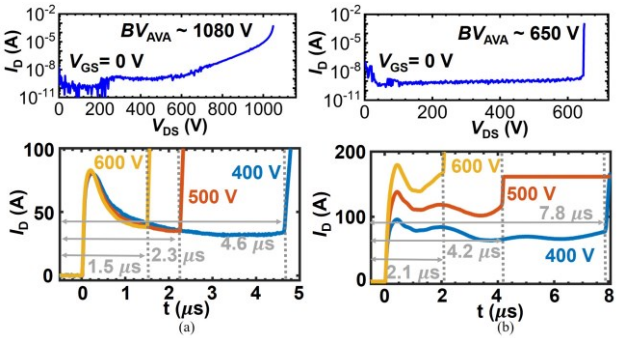


Fig. 8. The off-state I-V characteristics (top) and failure short-circuit test waveforms at a V_{BUS} of 400~600 V (bottom) of commercial (a) SiC MOSFETs (C3M0120065K) and (b) Si CoolMOS (IPZA60R180P7). In both tests, R_{ON} is 10 Ω and R_{OFF} is 2 Ω in the gate driver; the on-state gate drive voltage is 15 V. The t_{SC} of each test is marked in the waveform.

Finally, as the high-V_{BUS} short-circuit test data of Si and SiC devices are lacking in the literature, we tested the short-circuit capability of a 650-V SiC MOSFET (C3M0120065K) and a 600-V Si CoolMOS (IPZA60R180P7) at V_{BUS} higher than 400 V (Fig. 8). The tests were performed on the same short-circuit test board but with a MOS-type gate driver. At 600 V (below the BV_{AVA} of SiC MOSFETs and Si CoolMOS), their t_{SC} is around 1.5~2.1 µs. At V_{BUS} higher than 600 V, the two types of DUTs almost failed immediately with a device current reaching our measurement compliance and a shorting observed between all three terminals in each DUT. These test results suggest the lack of the short-circuit capability nearing BV_{AVA} in these devices.

V. Benchmark, Discussion, and Summary

Table II summarizes this work and prior reports on single-event and repetitive short-circuit capabilities of 600~700-V GaN, SiC and Si unipolar normally-off devices [2], [4], [5], [6], [22], [23]. Fig. 9 benchmarks their t_{SC} versus V_{BUS} capabilities. The GaN Fin-JFETs show the smallest specific R_{ON}, the highest t_{SC} and short-circuit energy density at 400 V (7.5 J/cm^2), no degradation in the repetitive 10 µs short-circuit tests, a failure-to-open signature, and unique short-circuit capabilities at V_{BUS} close to the device BV_{AVA}. These results set a new record for the GaN power transistor short-circuit capability and illustrate that GaN devices with appropriate designs can achieve comparable or even superior short-circuit capability when compared to Si and SiC MOSFETs and SiC cascode JFETs.

As a further discussion, we believe that the JFET structure is the key enabling factor for the high short-circuit capabilities

TABLE II. SUMMARY OF THE REPORTED SHORT-CIRCUIT TEST RESULTS OF 600~700-V NORMALLY-OFF UNIPOLAR GAN, SIC AND SI POWER TRANSISTORS.

Device	Type & Reference	Specific R_{on} (mΩ·cm^2)	Single Short Circuit Test				Repetitive Short Circuit Test				
			V_{bus} (V)	t_{SC} (μs)	E_{SC}[a] (J/cm^2)	Fail[b]	V_{bus} (V)	t_{SC} (μs)	Cycle period	Cycle number	Fail
Vertical GaN Fin-JFET (This work)		0.7	400 800	30.5 11.6	7.50 6.15	open	400	10	3 s	30,000	no
GaN HEMTs	Comm.[c] [2]	N/A	400	0.62	N/A	short	300	0.2	2 min	7	yes
	R&D [5]	N/A[d]	400	3	N/A	N/A					
	R&D [6]	19 Ω·mm[e]	400	4-10	N/A	N/A			N/A		
SiC/Si JFET cascode [22]		1.05	400	10	N/A	N/A	400	8	N/A	100	no
SiC MOSFET	Comm. [4]	N/A	400	13	N/A	open			N/A		
	R&D [23]	7.2	400	8.4	6.0	N/A					
Si CoolMOS	Comm. [23]	10	400	19	6.7	N/A			N/A		

Note: [a]critical short-circuit energy density. [b]failure signature. [c]commercial. [d]1.35X higher than commercial cascode HEMT. [e]~ 4.3 mΩ·cm^2 using a 20-μm source-to-drain length and 3-μm contact finger width.

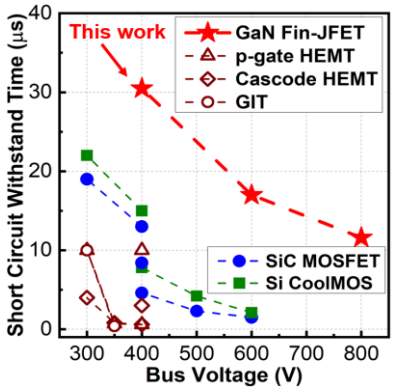


Fig. 9. t_{SC} *vs.* V_{BUS} benchmark for GaN Fin-JFETs and other 600~700 V GaN, SiC and Si devices. Data are from the literature reports in Table I and our measurements shown in Fig. 8.

observed in GaN Fin-JFETs. The JFET can effectively suppress $I_{D,SAT}$ under the short-circuit stress, and high short-circuit capabilities have been reported in SiC JFETs [24]-[27]. While the short-circuit performance of industrial SiC casode JFETs has been included in Table II, many other reports on normally-off and normally-on standalone SiC JFETs exist in the literature. Table III summarizes the reported short-circuit capabilities of 600 V and 1.2 kV standalone SiC JFETs, many of which show excellent t_{SC} at a bus voltage of 300-600 V. Note that of most of today's standalone SiC JFETs are normally-on, while the GaN Fin-JFET is normally-off. The viability and advantages of GaN Fin-JFET on realizing the normally-off operation have been explained in [10].

TABLE III. SUMMARY OF THE REPORTED SHORT-CIRCUIT TEST RESULTS OF 600-V and 1.2-kV SIC JFETs

Voltage Rating (V)	Operation Type	Temperature (°C)	Single Short Circuit Test			
			V_{bus} (V)	t_{SC} (μs)	E_{SC}[a] (J/cm^2)	Fail[b]
600	normally-on [24]	125	300	45	N/A	N/A
1200	normally-on [25]	25	600	300	N/A	N/A
1200	normally-on [26]	25	400	660	60	short
		350	400	6	N/A	N/A
1200	normally-off [27]	25	400	1440	44.6	short

Note: [a]critical short-circuit energy density. [b]failure signature.

In addition to reporting GaN Fin-JFET's breakthrough short-circuit capabilities, we also unveiled the key enabling device physics. Owing to the characteristics of the junction gate stack and the *R-C* interface gate driver, GaN Fin-JFET can effectively suppress its $I_{D,SAT}$ during the short-circuit withstanding process, thus enabling a long t_{SC}. The avalanche-through-fin mechanism allows for a large avalanche current through the fin channel and thus enables the unique short-circuit capability at a bus voltage close to the device BV_{AVA}. Our results show the great potential of vertical GaN Fin-JFETs for applications like EV powertrains, motor drives, and grids, due to their excellent robustness under the concurrent presence of short-circuit and overvoltage stresses.

REFERENCES

[1] R. S. Chokhawala, J. Catt and L. Kiraly, "A discussion on IGBT short-circuit behavior and fault protection schemes," in *IEEE Transactions on Industry Applications*, vol. 31, no. 2, pp. 256-263, Mar.-Apr. 1995.

[2] H. Li *et al*., "Robustness of 650-V Enhancement-Mode GaN HEMTs Under Various Short-Circuit Conditions," in *IEEE Transactions on Industry Applications*, vol. 55, no. 2, pp. 1807-1816, March-April 2019.

[3] US DRIVE Electrical and Electronics Technical Team Roadmap, Department of Energy, 2017. [Online]. Available: www.energy.gov

[4] N. Badawi, A. E. Awwad and S. Dieckerhoff, "Robustness in short-circuit mode: Benchmarking of 600V GaN HEMTs with power Si and SiC MOSFETs," *2016 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2016, pp. 1-7

[5] D. Bisi *et al*., "Short-Circuit Capability Demonstrated for GaN Power Switches," *2021 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2021, pp. 370-375.

[6] I. Hwang *et al*., "Estimation of Short Circuit Capability of GaN HEMTs Using Transient Measurement," in *IEEE Electron Device Letters*, vol. 42, no. 8, pp. 1208-1211, Aug. 2021

[7] J. Sun, J. Wei, Z. Zheng and K. J. Chen, "Short Circuit Capability Characterization and Analysis of p-GaN Gate High-Electron-Mobility Transistors Under Single and Repetitive Tests," in *IEEE Transactions on Industrial Electronics*, vol. 68, no. 9, pp. 8798-8807, Sept. 2021

[8] Y. Zhang and T. Palacios, "(Ultra)Wide-Bandgap Vertical Power FinFETs," in *IEEE Transactions on Electron Devices*, vol. 67, no. 10, pp. 3960-3971, Oct. 2020

[9] J. Liu *et al*., "1.2 kV Vertical GaN Fin JFETs with Robust Avalanche and Fast Switching Capabilities," *2020 IEEE International Electron Devices Meeting (IEDM)*, 2020, pp. 23.2.1-23.2.4

[10] J. Liu *et al*., "1.2-kV Vertical GaN Fin-JFETs: High-Temperature Characteristics and Avalanche Capability," in *IEEE Transactions on Electron Devices*, vol. 68, no. 4, pp. 2025-2032, April 2021.

[11] Y. Zhang *et al*., "Large-Area 1.2-kV GaN Vertical Power FinFETs with a Record Switching Figure of Merit," in *IEEE Electron Device Letters*, vol. 40, no. 1, pp. 75-78, Jan. 2019.

[12] "Driving CoolGaN™ 600 V high electron mobility transistors," Infineon. https://www.infineon.com/cms/en/product/power/gan-hemt-gallium-nitride-transistor/#!documents (accessed Nov. 17, 2021).

[13] E. Platania *et al*., "A Physics-Based Model for a SiC JFET Accounting for Electric-Field-Dependent Mobility," in *IEEE Transactions on Industry Applications*, vol. 47, no. 1, pp. 199-211, Jan.-Feb. 2011.

[14] Y. Xi and E. F. Schubert, "Junction–temperature measurement in GaN ultraviolet light-emitting diodes using diode forward voltage method," *Applied Physics Letters*, vol. 85, no. 12, pp. 2163–2165, Sep. 2004.

[15] B. Wang *et al*., "Low Thermal Resistance (0.5 K/W) Ga_2O_3 Schottky Rectifiers With Double-Side Packaging," in *IEEE Electron Device Letters*, vol. 42, no. 8, pp. 1132-1135, Aug. 2021

[16] A. Castellazi *et al*., "Gate-damage accumulation and off-line recovery in SiC power MOSFETs with soft short-circuit failure mode," in *Microelectronics Reliability*, vol. 114, no. 113943, Oct. 2020.

[17] J. Liu *et al*., "Surge Current and Avalanche Ruggedness of 1.2-kV Vertical GaN p-n Diodes," in *IEEE Transactions on Power Electronics*, vol. 36, no. 10, pp. 10959-10964, Oct. 2021.

[18] Y. Zhang *et al*., "Electrothermal simulation and thermal performance study of GaN vertical and lateral power transistors," in *IEEE Transactions on Electron Devices*, vol. 60, no. 7, pp. 2224–2230, Jul. 2013.

[19] L. Cao, J. Wang, G. Harden, H. Ye, R. Stillwell, A. J. Hoffman, and P. Fay, "Experimental characterization of impact ionization coefficients for electrons and holes in GaN grown on bulk GaN substrates," in *Applied Physics Letters*, vol. 112, p. 262103, Jun. 2018.

[20] R. Zhang, J. Kozak, M. Xiao, J. Liu, and Y. Zhang, "Surge-Energy and Overvoltage Ruggedness of p-Gate GaN HEMTs," in *IEEE Transactions on Power Electronics*, vol. 35, no. 12, pp. 13409-13419, Dec. 2020.

[21] Q. Song, R. Zhang, J. Kozak, J. Liu, Q. Li, and Y. Zhang, "Robustness of Cascode GaN HEMTs in Unclamped Inductive Switching," in *IEEE Transactions on Power Electronics*, early access online, Oct. 2021.

[22] A. Bhalla *et al*., "Ultra-high speed 7mohm, 650V SiC half-bridge module with robust short circuit capability for EV inverters," *2019 31st International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, 2019, pp. 191-194,

[23] A. Agarwal, A. Kanale and B. J. Baliga, "Advanced 650 V SiC Power MOSFETs With 10 V Gate Drive Compatible With Si Superjunction Devices," in *IEEE Transactions on Power Electronics*, vol. 36, no. 3, pp. 3335-3345, March 2021.

[24] V. Sundaramoorthy *et al*., "Short circuit ruggedness of 600 V SiC trench JFETs," *Mater. Sci. Forum*, vol. 1004, pp. 933–938, Jul. 2020.

[25] J. Lutz and R. Baburske, "Some aspects on ruggedness of SiC power devices," in *Microelectronics Reliability*, vol. 54, no. 1, pp. 49–56, Jan. 2014.

[26] N. Boughrara, S. Moumen, S. Lefebvre, Z. Khatir, P. Friedrichs, and J. C. Faugieres, "Robustness of SiC JFET in Short-Circuit Modes," in *IEEE Electron Device Letters*, vol. 30, no. 1, pp. 51-53, Jan. 2009.

[27] X. Huang, G. Wang, Y. Li, A. Q. Huang and B. J. Baliga, "Short-circuit capability of 1200V SiC MOSFET and JFET for fault protection," *2013 Twenty-Eighth Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2013, pp. 197-200.