Robust through-Fin Avalanche in Vertical GaN Fin JFET with Soft Failure Mode

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***Abstract*—We study the inherent ruggedness of the avalanche through the fin channel, a new avalanche mode in a vertical GaN power Fin-JFET, through single-pulse and repetitive avalanche circuit tests. By turning on the gate during avalanche, the major avalanche current path migrates from the p-GaN gate to the n-GaN fin channel. The single-pulse critical avalanche energy density (E_{AVA}) was measured to be 10 J/cm^2, which is the highest reported in GaN transistors. The Fin-JFET withstood over 3700 repetitive avalanche pulses at 70% of E_{AVA}. It exhibits a failure-to-open-circuit signature in single and repetitive avalanche. This soft failure mode allows the device to retain its full breakdown voltage, which is highly desirable for system robustness. By contrast, the through-gate avalanche in Fin-JFETs and the reported avalanche in Si and SiC transistors all show a destructive, failure-to-short-circuit signature. These results show the viability of soft avalanche failure in power devices, provide key robustness references for GaN devices, and suggest the fundamental superiority of moving the avalanche path away from the major blocking junction.**

***Index Terms*— power electronics, gallium nitride, avalanche, JFET, FinFET, unclamped inductive switching.**

I. Introduction

Avalanche capability is a critical metric for power devices. Avalanche is an impact ionization (I. I.) and multiplication phenomenon that allows the device to pass a high avalanche current (I_{AVA}) when sustaining the avalanche breakdown voltage (BV_{AVA}). This capability protects devices from the voltage overshoot in circuits and allows the dissipation of the circuit surge energy [1]. In a power device, I_{AVA} usually flows across the major blocking p-n junction, i.e., the peak electric field (E-field) location at BV_{AVA}. As a result, when high I_{AVA} induces a thermal failure, the blocking junction is usually damaged, yielding a failure-to-short-circuit (FTS, or *hard* [2]) signature. SiC and Si MOSFETs [3]–[8], JFETs [9], [10] and Si insulated-gate bipolar transistors (IGBTs) [11] have all been reported to fail short in avalanche tests.

Failure-to-open-circuit (FTO, or *soft*) is a signature opposite to the FTS [2], [12], in which a device retains its full blocking voltage after failure. FTO is preferred in system applications, particularly in multi-chip modules, as the chips in parallel with the failed device still enable the system to operate [2]. However, no FTO signature has been demonstrated in prior Si and SiC power devices in an avalanche failure.

For GaN transistors, avalanche capability was first realized in a fin-channel junction field-effect transistor (Fin-JFET) very recently [13], [14] (Fig. 1(a)). This device leverages the benefits of sub-micrometer fin channels [15] to realize the normally-off operation and a specific on-resistance (R_{ON}) smaller than SiC FETs [13]. In this Fin-JFET, two avalanche paths have been demonstrated: (a) through the p-GaN gate [13], [14], and (b) through the n-GaN fin channel [16]. The gated channel is OFF in the first avalanche path, similar to the avalanche in other FETs, and it is turned ON in the second path. While these two modes have been realized in different circuits [16], their inherent ruggedness remains unknown.

This work studies the inherent ruggedness of GaN Fin-JFETs in both avalanche modes, highlighting the repetitive circuit tests which were not reported before. Major new findings include (a) a record high critical avalanche energy density (E_{AVA}) in GaN devices and (b) a unique FTO signature in avalanche, which was not reported in any other power FET. The results provide new insights of avalanche in power devices.

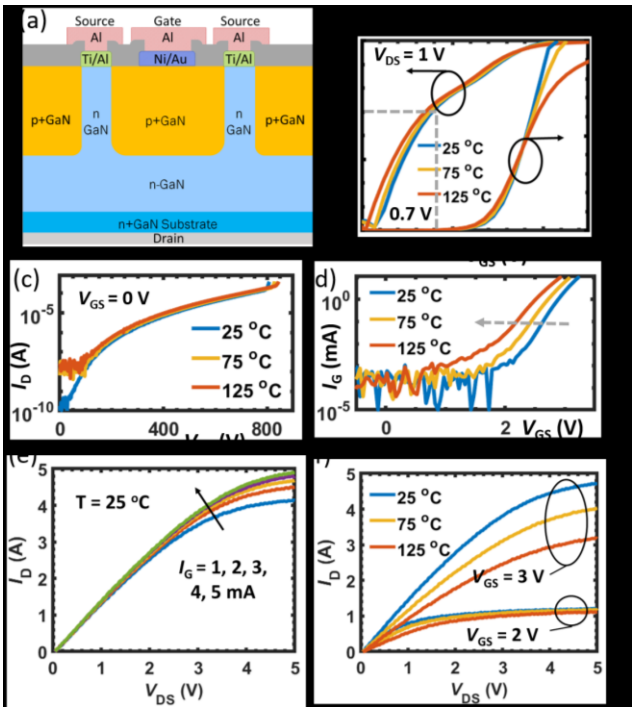

Fig. 1. (a) Schematic of the vertical GaN Fin-JFET. The DUT's (b) transfer, (c) OFF-state I_D-V_{DS} and (d) I_G-V_{GS} characteristics at 25-125 °C. Output characteristics with (e) various I_G and (f) various V_{GS} at 25-125 °C.

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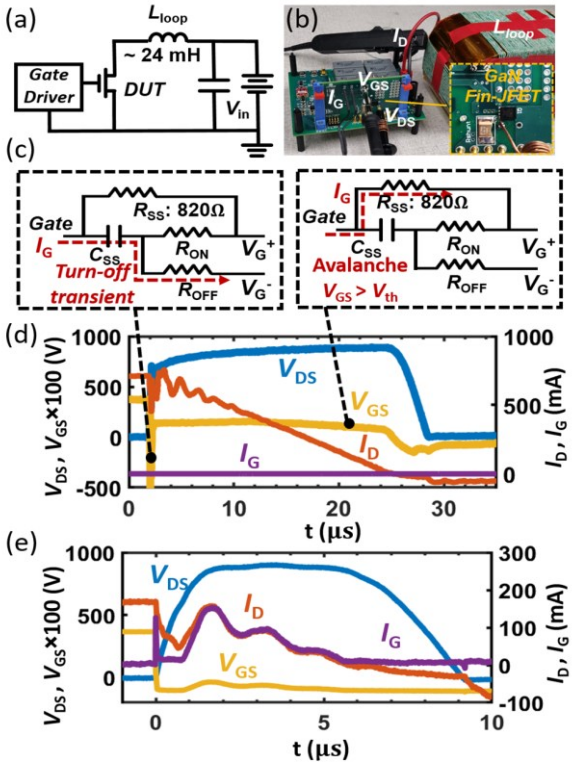

Fig. 2. (a) Circuit schematic and (b) setup of the UIS test. (c) the *RC*-interface gate driver and the illustration of current paths in the DUT's turn-OFF and avalanche processes. Typical (d) through-fin and (e) through-gate avalanche waveforms of the DUT under a load inductance of 24 mH.

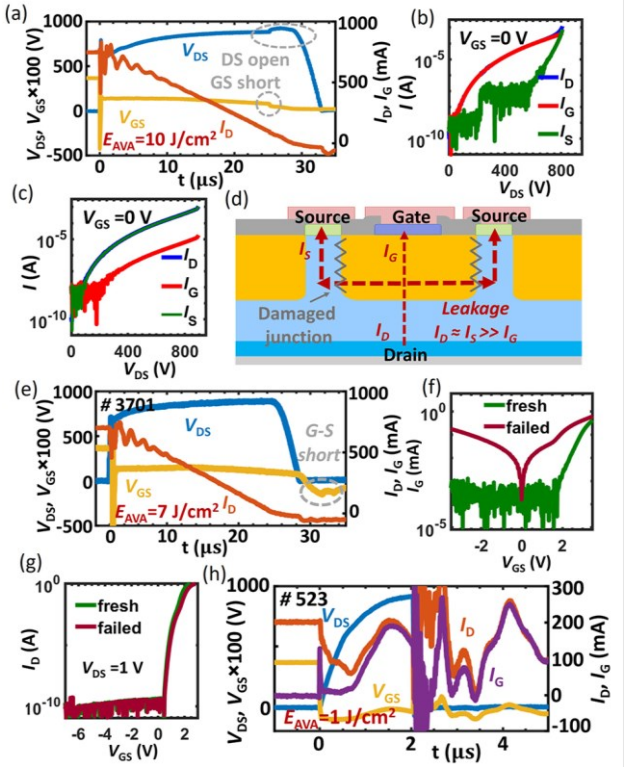

Fig. 3. (a) Failure waveform of a single-pulse through-fin avalanche. OFF-state *I-V* characteristics of (b) a fresh DUT and (c) the failed DUT. (d) Illustration of leakage current paths in the failed DUT. (e) Initial failure waveform in the repetitive through-fin avalanche test. (f) I_G-V_{GS} and (g) transfer characteristics of the fresh and failed DUTs after cycle #3701. (h) Failure waveform in the repetitive through-gate avalanche test, in which the DUT fails at cycle #523.

II. Device and Test Circuit

Fig. 1(a) shows the device under test (DUT), the 650-V class GaN Fin-JFET fabricated by NexGen Power Systems. Fig. 1(b) and (c) show the transfer and OFF-state I-V characteristics at 25, 75 and 125 ºC. The threshold voltage (V_{th}) is 0.7 V at 25 ºC extracted at a drain current (I_D) of 1 mA. The BV_{AVA} is ~800 V with a positive temperature coefficient. The DUT has an active area of 0.1 mm^2 and a TO-247-4 package.

Fig. 1(d) shows the gate current (I_G) versus gate-to-source bias (V_{GS}). The turn-on voltage is ~3 V extracted at I_G = 1 mA, which is close to GaN's bandgap, suggesting the good quality of the lateral p-n junction with low interface states [17]. This gate stack allows an effective hole injection into the fin channel, which is validated by output characteristics at various I_G (Fig. 1(e)). At higher I_G, the enhanced hole injection induces a stronger conductivity modulation, reducing R_{ON} and raising the saturation I_D. Fig. 1(f) shows the output characteristics at various V_{GS}, revealing a specific R_{ON} of 0.7 mΩ·cm^2.

The avalanche capability of power devices is usually tested in an unclamped inductive switching (UIS) circuit [1]-[11]. Fig. 2(a) shows the UIS circuit used in this work. A 24 mH inductor is connected with the DUT, and the input voltage (V_{in}) is set at 30 V. In the test, the DUT is first turned ON to charge the inductor. Then it is turned OFF, and the energy stored in the inductor drives the DUT into avalanche. Fig. 2(b) shows our UIS test setup. V_{GS}, I_D, and drain-to-source voltage (V_{DS}) are directly measured by probes. I_G is calculated by the voltage drop on a gate resistor in the driving circuit. A program is developed to control the repetitive UIS tests.

Two gate drivers were used to produce two avalanche modes in the UIS tests. A MOSFET gate driver with a 2 Ω gate resistor [14] was used to ensure $V_{GS} < V_{th}$ in avalanche, producing a through-gate avalanche. A *RC*-interface driver was used to produce the through-fin avalanche [16] (Fig. 2(c)), which consists of a capacitor (C_{SS}) and three gate resistors (R_{ON}, R_{OFF} and R_{SS}, with $R_{SS} >> R_{ON}$, R_{OFF}). During avalanche, I_{AVA} first goes through C_{SS} and R_{OFF}, charging C_{SS} until $V_{GS} > V_{th}$. Then the fin channel is turned ON, migrating I_{AVA} to the source. I_G then flows through the large R_{SS} to keep $V_{GS} > V_{th}$.

III. Experimental Results

Fig. 2(d) and (e) show the DUT's through-fin and through-gate avalanche waveforms in the UIS tests, respectively. In both waveforms, V_{DS} clamps at BV_{AVA}, and I_{AVA} gradually reduces to zero, exhibiting a textbook-like avalanche behavior. In Fig. 2(d), $V_{GS} > 1$ V and $I_G << I_{AVA}$, validating the through-fin avalanche. In Fig. 2(e), $V_{GS} < 0$ V and $I_G \approx I_{AVA}$, validating the through-gate avalanche.

The E_{AVA} of the through-fin avalanche was then studied by increasing the load current in the UIS test. Fig. 3(a) shows a typical failure waveform. Upon failure, V_{GS} reduces to zero, indicating a shorted gate-source (G-S) junction; the drain-source (D-S) remains open, and V_{DS} climbs to a slightly higher BV_{AVA}. To further probe the failure location, the source current (I_S), I_D and I_G of a fresh DUT and the failed DUT were measured at increased V_{DS} and zero V_{GS} on the curve tracer. For the fresh DUT (Fig. 3(b)), $I_D \approx I_G \gg I_S$, showing that the gate-drain (G-

D) junction is the main leakage path and the G-S junction remains OFF. For the failed DUT (Fig. 3(c) and (d)), $I_D \approx I_S \gg I_G$, proving the shorted G-S junction, which deviates the leakage current to the low-resistivity fin channel. Note that I_D is almost identical in the fresh and failed DUTs, suggesting that the G-D junction is intact in the failed DUT.

Interestingly, the failed DUT shows a BV_{AVA} higher than that of the fresh DUT (Fig. 3(d)). This higher BV_{AVA} can be explained by the shorted G-S junction, which eliminates the depletion of lateral p-n junction in the failed DUT and thus reduces the peak E-field at the fin bottom.

Four DUTs were then tested to failure. From the BV_{AVA}~I_{AVA} integral, E_{AVA} of three devices were calculated to be 10 J/cm^2, and 8 J/cm^2 for the last device. The capacitive energy was much smaller than E_{AVA} (0.11 J/cm^2 calculated from the V_{DS}~I_D integral in the capacitive charging stage [1]).

Repetitive UIS tests were then performed with a 3 s interval and 70% E_{AVA} in each cycle. No junction temperature built-up was observed, as confirmed by the thermal camera. Multiple DUTs were tested, and they all survived thousands of cycles with consistent behaviors. Here we describe a typical DUT that showed initial degradation in cycle #3701. The waveform suggests a G-S partial short (Fig. 3(e)). The post-cycle tests reveal an I_G increase at negative V_{GS} (Fig. 3(f)), while the gate control is retained at forward V_{GS} (Fig. 3(g)).

This DUT continued to withstand avalanche stress until the G-S junction is fully shorted in cycle #3705, in which the DUT cannot be turned ON. The BV_{AVA} is retained, revealing a FTO signature. This progressive FTO behavior can be explained by the increase in the number of fins that fail in the repetitive avalanche, with the G-S failed short in each fin.

By contrast, the DUTs tested in the through-gate avalanche failed with an FTS signature in single and repetitive tests. The E_{AVA} of the through-gate avalanche was measured to be ~1 J/cm^2. Fig. 3(h) shows the DUT failure waveform in the repetitive tests, revealing a destructive failure.

To understand the distinct failure behaviors in two avalanche modes, mixed-mode TCAD simulations were performed in Silvaco Atlas. The device model is based on [18]–[20] and the mixed-mode simulation setup based on [21] using the UIS circuit. All experimental waveforms can be replicated.

Fig. 4 shows the simulated contours of I. I. generation rate, E-field and current in two avalanche modes. In the through-gate avalanche (Fig. 4(a)-(d)), the locations of peak E-field, I. I. generation rates, and electron and hole currents are all at the G-D p-n junction. Hence, the junction damage due to high I_{AVA} and local heating leads to the device short failure.

In the through-fin avalanche (Fig. 4(e)-(h)), while the peak E-field is still at the G-D p-n junction, the peak I. I. location moves to the foot of the n-GaN fin. Electrons are pumped from the source, travel through the fin channel, and recombine with the I. I.-generated holes. Holes are also partially removed via the gate to maintain the small I_G. As a result, the high I_{AVA} stress congregates in the fin, and only a small hole current density is present at the junction around the fin corner.

As this I_{AVA} stress is away from the G-D junction, and the narrow fin prevents the punch-through, BV_{AVA} retains in the failed DUT. The current density in the junction region is much lower than that in the avalanche through gate, suggesting a much smaller electrothermal stress locally. This explains the higher E_{AVA} in the avalanche through fin.

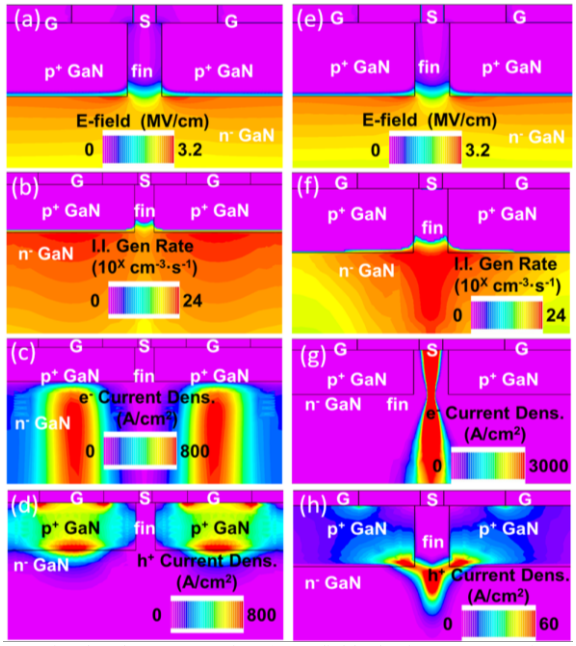

Fig. 4. Simulated contours of (a)(e) E-field, (b)(f) I. I. generation rate, (c)(g) electron current density, and (d)(h) hole current density in the Fin JFET. (a)-(d) in the left column correspond to the through-gate avalanche, and (e)-(h) in the right column correspond to the through-fin avalanche.

IV. Benchmark and Summary

Table I compares the avalanche test results of GaN Fin-JFET with those of Si superjunction MOSFETs [8], [22], SiC JFETs [10], and SiC MOSFETs [4], [6]. The E_{AVA} of GaN Fin-JFETs is the highest reported in GaN FETs, much higher than that of Si MOSFETs and comparable to SiC FETs. Despite the fewer survival cycles than Si and SiC MOSFETs, the GaN Fin-JFET shows an FTO signature in the through-fin avalanche, while all Si and SiC FETs show an FTS signature in avalanche. This shows the great promise of GaN Fin-JFETs in the applications like automotive powertrains and electric grids.

The broader implication of this work is that the I_{AVA} path can be tuned away from the major blocking p-n junction; this spatial separation of the high current stress and the peak E-field allows a new, robust avalanche mode with the desirable FTO signature.

TABLE I. SUMMARY OF REPORTED AVALANCHE ROBUSTNESS DATA OF GAN, SIC, AND SI UNIPOLAR POWER FETs

Device	Voltage Rating (kV)	E_{AVA} (J/cm^2)	Repetitive Avalanche			Failure signature
			E_{AVA}%[a]	Period	Cycle survived	
GaN Fin JFET	**0.65**	**10.0**	**70%**	**3 s**	**>3700**	**FTO**
Si CoolMOS	0.6-0.9	1.3 [22]	62% [8]	3 s	10000	FTS
SiC JFET[b]	1.2	18 [10]	90% [10]	4 s	1000	FTS
SiC MOSFET	1.2	7.5[c] [4]	<77%[d] [6]	0.5 s	80000	FTS

[a]Percentage of E_{AVA} used in repetitive tests; [b]Normally-ON device; [c]E_{AVA} extracted at an avalanche time similar to that of GaN Fin-JFETs; [d]Estimated using the single-pulse avalanche energy provided in the datasheet, which is expected to be lower than the true E_{AVA} of the device.

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