Vertical GaN Fin JFET: A Power Device with Short Circuit Robustness at Avalanche Breakdown Voltage

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***Abstract*—GaN high-electron-mobility transistors (HEMTs) are known to have no avalanche capability and insufficient short-circuit robustness. Recently, breakthrough avalanche and short-circuit capabilities have been experimentally demonstrated in a vertical GaN fin-channel junction-gate field-effect transistor (Fin-JFET), which shows a good promise for using GaN devices in automotive powertrains and electric grids. In particular, GaN Fin-JFETs demonstrated good short-circuit capability at avalanche breakdown voltage (BV_{AVA}), with a failure-to-open-circuit (FTO) signature. This work presents a comprehensive device physics-based study of the GaN Fin-JFET under short-circuit conditions, particularly at a bus voltage close to BV_{AVA}. Mixed-mode electrothermal TCAD simulations were performed to understand the carrier dynamics, electric field distributions, and temperature profiles in the Fin-JFET under short-circuit and avalanche conditions. The results provide important physical references to understand the unique robustness of the vertical GaN Fin-JFET under the concurrence of short-circuit and avalanche as well as its desirable FTO signature.**

***Index Terms*—gallium nitride, FinFET, JFET, short circuit, avalanche, failure analysis, TCAD simulations**

I. INTRODUCTION

Based on gallium nitride's (GaN) superior material properties, GaN power devices show a good trade-off between breakdown voltage and on-resistance (R_{ON}), fast-switching speed, and high-temperature operation capability. These advantages have enabled GaN devices to be increasingly adopted in many power electronics applications. However, GaN high-electron mobility transistors (HEMTs) have limited ishort-circuit (SC) robustness. The reported SC withstanding time (t_{SC}) of all types of commercial 600/650-V class GaN HEMT is less than 1 µs at a 400-V bus voltage (V_{BUS}) [3-5], which is lower than the usual system requirement and thereby limits their usage in automotive powertrains and power grids.

Significant efforts have been made to optimize GaN HEMT structures for more robust SC capability and understand the failure mechanisms. In [6], the device R_{ON}, saturation current ($I_{D,sat}$) and switching speed were traded for a t_{SC} of 3 µs at 400 V. However, this t_{SC} is still much smaller than the typical system requirement of 10 µs [7]. In [8], the SC failure in HEMT was found to be related to the propagation of the high electric field from gate to the drain. The faster propagation of electric field leads to shorter t_{SC}. As the failure is not thermally induced, the HEMT structure actually does not take the full advantage of the GaN material properties for sustaining high temperatures. Therefore, it is necessary to explore the SC robustness of GaN devices with architectures different from HEMT.

Good progress has been made in vertical GaN transistors recently. Breakdown voltages of 1.2-2 kV have been demonstrated on current-aperture electron transistors [9,10], trench MOSFETs [11,12] fin-channel MOSFETs [13,14] and fin-channel junction field-effect transistors (Fin-JFETs) [15-17]. All these devices show a normally-off operation. The maximum current reaches 100 A [11], and specific R_{ON} is as low as 0.82 mΩ·cm^2 [16]. Among all reported vertical GaN devices, the Fin-JFET shows excellent potential for industrial applications and is being commercialized by NexGen Power Systems. With sub-micrometer fin-channels and gate-all-around structures, GaN Fin-JFET has a high channel density, which enables a smaller specific R_{ON} and superior switching performance as compared to the similarly-rated SiC MOSFETs [15]-[17].

In addition to excellent static and switching performance, vertical GaN Fin-JFETs also demonstrate breakthrough SC and avalanche robustness [18,19]. The t_{SC} was measured to be 30.5 µs at a 400-V V_{BUS} with a failure-to-open-circuit (FTO) signature. Additionally, at V_{BUS} near the device avalanche breakdown voltage (BV_{AVA}), the device retains excellent SC robustness with a t_{SC} over 10 µs. This was the first report of a power device with robust SC capability at its BV_{AVA} [18].

Vertical GaN Fin-JFET also has been reported to be the first avalanche-capable GaN power transistor, as characterized by the unclamped inductive switching (UIS) circuit [15,17,19]. Two different avalanche modes were identified, with the avalanche current (I_{AVA}) going through the p-GaN gate [15,17] or the n-GaN fin and source [16,19], respectively. In particular, by using an RC interface gate driver, the I_{AVA} path can be tuned from the p-GaN gate to the fin channel and source [16]. In this through-fin avalanche, the maximum critical avalanche energy (E_{AVA}) of GaN Fin-JFET was reported to be 10 J/cm^2 with a desirable FTO signature [19].

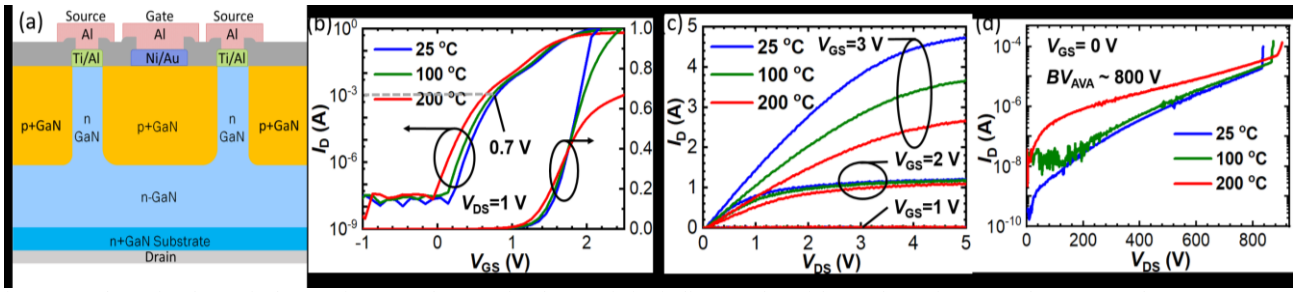

Fig. 1. (a) Schematic of a vertical GaN Fin-JFET. (b) Transfer characteristics in linear and semi-log scale. V_{th} is extracted as 0.7 V at the 1-mA I_D at 25 °C (c) Output characteristics at V_{GS} from 1 V to 3 V. (d) Off-state I-V characteristics, with the BV_{AVA} being around 800 V at 25 °C.

Despite experimental demonstrations, the detailed device physics enabling the robust SC capability of Fin-JFETs has not been fully explained. In this work, we present the carrier dynamics, electric field distributions and temperature evolutions inside the Fin-JFET during the SC process, with a focus on understanding the enabling physics for the SC at BV_{AVA} and the FTO signature, as well as on the correlation between the avalanche and SC in GaN Fin-JFET.

This paper is organized as follows. Section II reviews the key experimental results. Section III describes the models of the mixed-mode electrothermal TCAD simulations used in this work. Section IV and V discuss the critical device physics enabling the SC and avalanche performance, respectively. Section VI reveals the mechanisms of the FTO signature. Section VII concludes the paper.

II. Review of Key Experimental Results

A. Device Characteristics

Fig. 1(a) shows a schematic of the device under test (DUT): the 650-V class vertical GaN Fin-JFET fabricated on 100-mm GaN substrates. The device is a NexGen design and manufactured at NexGen's New York fabrication facility. The JFET features an array of ~1 µm high n-GaN fin channels and p^+-GaN gate-all-around structure. The static characteristics and working principles of vertical GaN Fin JFET have been reported in [15-17]. The active area is 0.1 mm^2 and the DUTs are assembled in the standard TO-247 packages. Fig. 1(b) and (c) show the DUT's transfer and output characteristics at 25 °C, 100 °C and 200 °C, respectively, revealing a 0.7 V threshold voltage (V_{th}) at a drain current (I_D) of 1 mA, a 0.7 Ω R_{ON} and a ~4.7 A saturation current at a gate-to-source voltage (V_{GS}) of 3 V. The off-state drain-to-source I_{DS}-V_{DS} characteristics (Fig. 1(d)) show a non-destructive BV_{AVA} of 800 V at 25 °C with a positive temperature coefficient.

B. Short-circuit and avalanche test setup

Fig. 2(a) shows the test circuit diagram. In SC tests, no external inductor is connected in the circuit. A small stray inductance (48 nH) of the PCB layout allows rapid current rise when the DUT is switched on, which emulates the shoot-through condition in applications. In avalanche tests, the UIS circuit is implemented, in which a 24 mH inductor is used to provide the surge energy that drives the DUT into the avalanche mode. In both tests, an *RC* interface gate driving circuit is used (Fig. 2(b)), which is the same as the driver in device switching applications [15]. In this driver, a capacitive current provided by C_{SS} enables fast turn-on while an 820-Ω R_{SS} suppresses the quiescent gate current (I_G) and reduces driver's loss. Fig.2 (c) shows the test setup. A 810 µF capacitor bank stabilizes V_{BUS}. During the test, DUT V_{DS}, V_{GS} and I_D are directly measured by probes, I_G is calculated from the voltage drop across R_{SS}.

An additional protection setup was used for the SC test at a V_{BUS} close to the DUT's BV_{AVA}. A 24VV10 converter from PICO is connected to the input nodes as the voltage source. V_{BUS} is gradually increased until V_{DS} cannot be further raised, indicating that BV_{AVA} is reached. The converter output current compliance limits the I_{AVA} to be under 0.6 mA, ensuring that the DUT is not damaged in the off-state avalanche.

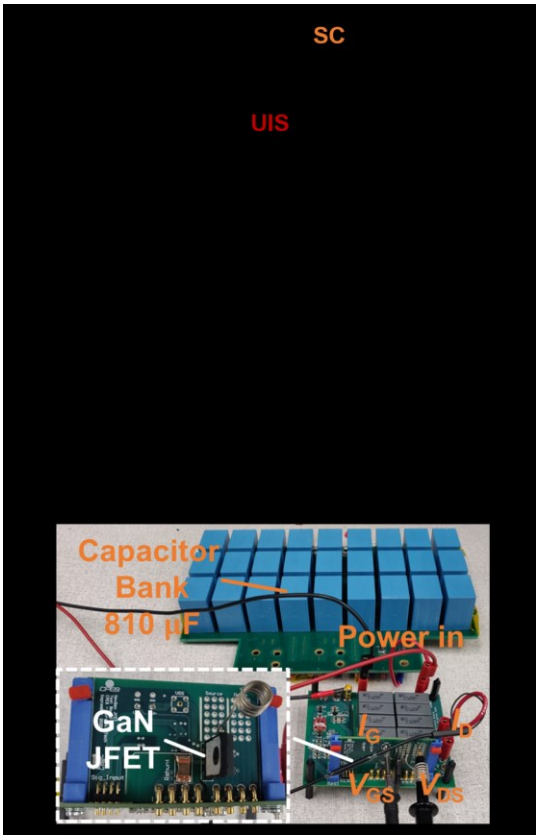

Fig. 2. (a) Schematic of the test circuit. In SC tests, the stray inductance is 48 nH. In UIS tests, an external 24 mH inductor is connected. (b) Schematic of the RC interface gate driving circuit used in the tests. V_G^+ is 8 V and V_G^- is -2 V. (c) Photo of the test setup.

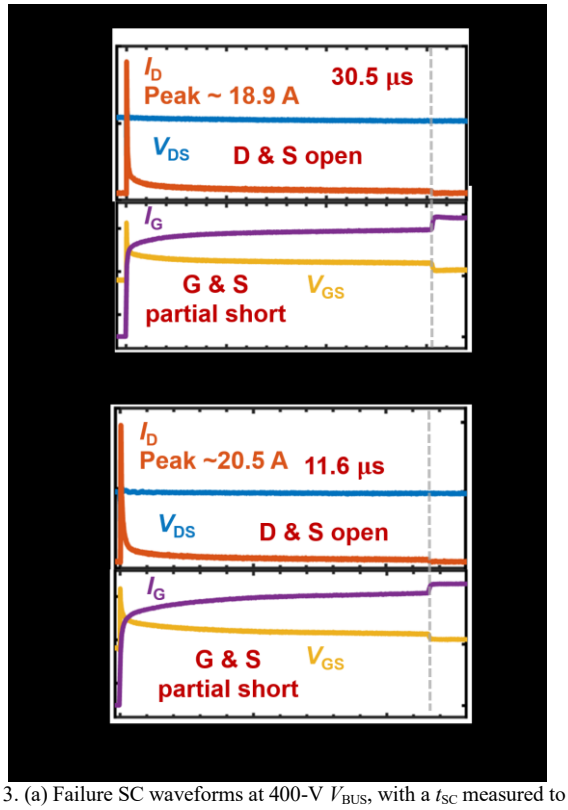

Fig. 3. (a) Failure SC waveforms at 400-V V_{BUS}, with a t_{SC} measured to be 30.5 µs. (b) Failure SC waveforms at 800-V V_{BUS}, with the t_{SC} measured to be 11.6 µs. DUTs fail gate-to-source short and drain-to-source open in both testing conditions.

C. Short circuit test resutls

All DUTs survived 10-µs SC test at a V_{BUS} increased from 400 V to the DUT's BV_{AVA} (800 V) and showed no degradation after the test. DUTs were then driven to failure by gradually increasing the turn-on time in the SC test. A two-minute relaxation time between each test was applied to ensure that DUTs were back in fresh state before each SC pulse. Fig. 3(a) and (b) show the failure waveforms at 400 V and BV_{AVA}, respectively, revealing a t_{SC} of 30.5 µs at 400 V and 11.6 µs at BV_{AVA}. The test waveforms feature a rapid rise of I_D, followed by a quick decrease of the saturation current ($I_{D,sat}$). The $I_{D,sat}$ decrease in GaN Fin-JFET is much faster as compared to GaN HEMTs and Si/SiC MOSFETs. Upon failure, V_{DS} stays at V_{BUS} while V_{GS} drops to zero, suggesting a gate-source (G-S) shorting and gate-drain (G-D) junction open. This is confirmed by the off-state I-V characteristics shown in Fig. 4, revealing the preservation of BV_{AVA} in the failed DUT.

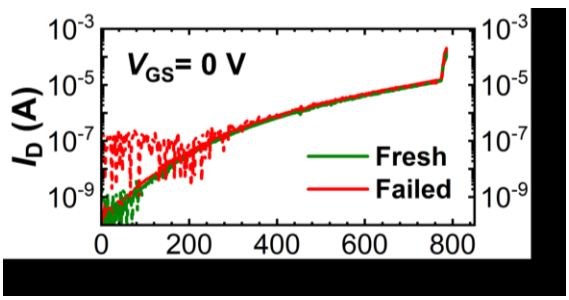

Fig. 4. Off-state I-V characteristics of the fresh and failed DUT. After failure, the DUT maintains the BV_{AVA} while the gate leakage increases.

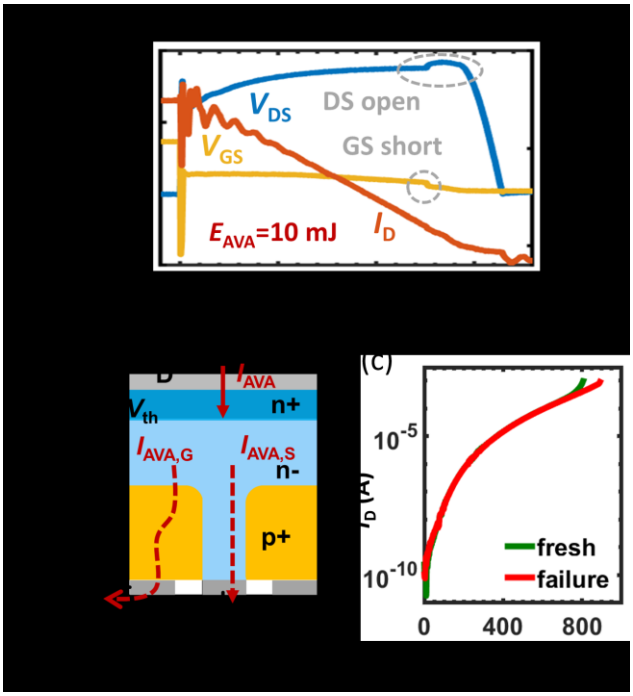

Fig. 5. (a) Typical avalanche failure waveforms in the UIS test with the RC gate driver. (b) Illustration of the avalanche current paths. The voltage drop across R_{SS} lifts V_{GS} to exceed V_{th}. Majority of I_{AVA} then flows through the Fin channel. (c) Off-state I-V characteristics of a fresh DUT and a failed DUT after the UIS test., revealing that the BV_{AVA} is retained.

D. Avalanche (UIS) test resutls

Fig. 5(a) shows the typical failure waveforms in the UIS test. During the avalanche, V_{GS} is raised to a positive value. The avalanche current paths are illustrated in Fig. 5(b): right after the turn-OFF, the avalanche first occurs at the pn junction between the gate and drain, and the voltage drop on R_{SS} raises V_{GS} to exceed the DUT's V_{th}, turning on the n-GaN fin channel; subsequently, the majority of I_{AVA} flows through the fin with a small I_{AVA} through the gate to maintain $V_{GS} > V_{th}$.

Similar to the SC test, upon failure, V_{GS} reduces to zero, indicating a shorted G-S junction and an open D-S junction. V_{DS} climbs to a slightly higher BV_{AVA} as revealed by the off-state I-V characteristics shown in Fig. 5(c). This higher BV_{AVA} can be explained by the absence of depletion region charge in the shorted G-S junction, which reduces the peak electric field at the pn junction edge. Note that the increase in BV_{AVA} is more pronounced with an increased number of the failed fins. As the BV_{AVA} of the DUTs failed in the SC test remains nearly unchanged (see Fig. 4), it can be inferred that less fins are damaged in the SC test. This is probably because that, during the SC test, the DUT's V_{DS} is fixed at 800 V, while in the UIS test, the DUT's V_{DS} is tied to BV_{AVA}, which increases with the elevated temperature during the avalanche process and thereby induces a slightly stronger overvoltage stress.

It is worth highlighting that the DUT shows a FTO signature in both SC and avalanche tests. This FTO signature is very favorable in system applications, as the failed device still blocks voltage, protecting the system from further damage and retaining the system functionality in the case of parallel devices or multi-chip modules [20].

III. Simulation Setup

To probe the internal electrostatics and carrier dynamics in the Fin-JFET at any transient of the above circuit tests, physics-based, electrothermal, mixed-mode TCAD simulations are performed in Silvaco Atlas. The electrothermal models are similar to [21]; the device avalanche models are based on those described in [15], [22], and the impact ionization coefficients are extracted from [23]. The key material parameters and the relevant models are summarized in Table I.

TABLE I. KEY MODELS IN THE ELECTRO-THERMAL SIMULATION

Parameter	Simulation Model
GaN electron mobility ($cm^2 \cdot V^{-1} \cdot s^{-1}$)	Drift layer: $800\times(T_L/300)^{-1.25}$ Substrate: $100\times(T_L/300)^{-1.25}$
GaN k_T ($W \cdot cm^{-1} \cdot K^{-1}$)	$2\times(T_L/300)^{-1.3}$
Thermal resistance ($W \cdot cm^{-2} \cdot K^{-1}$)	Top surface: 2 Bottom surface: 0.1
Impact ionization coefficients (cm^{-1})	Electron: $4.48\times10^8\times\exp(-3.39\times10^7/E)$ Hole: $7.13\times10^8\times\exp(-1.46\times10^7/E)$

T_L: lattice temperature (in Kelvin); E: electric field.

In the mixed-mode simulation, the circuit parameters are defined to be the same as those in experimental setups, and the device unit-cell structure is tuned to match the DUT's static characteristics. Fig. 6(a) shows a simulated I_D waveform in the SC test at 400 V with a pulse width of 30 µs, with all key signatures in a good agreement with experimental waveforms.

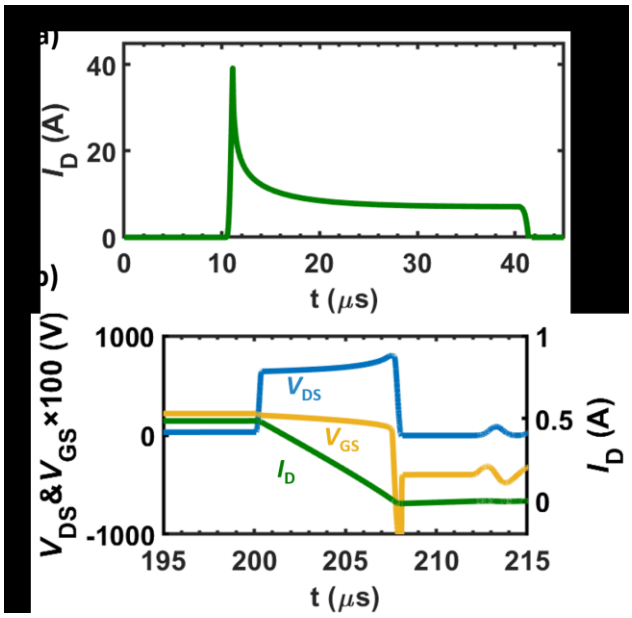

Fig. 6. Simulated waveforms of the (a) I_D in a SC test and the (b) V_{GS}, V_{DS} and I_D in a UIS test.

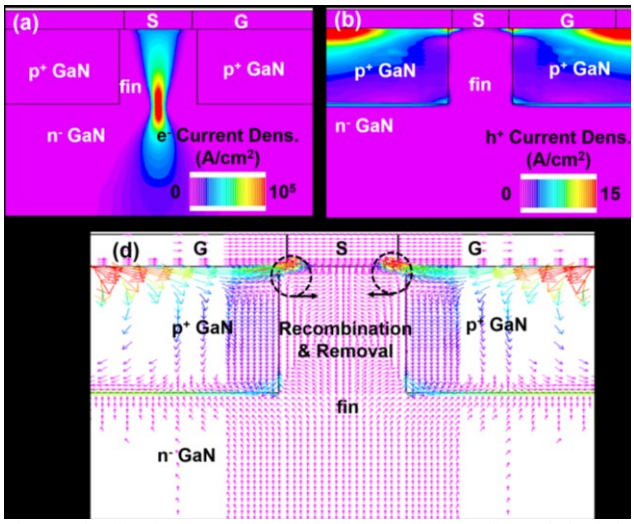

Fig. 7. Simulated contours of (a) electron current density and (b) hole current density and (c) hole current vectors in the SC condition (t = 10 µs) at a V_{BUS} of 400 V.

As another example of the calibration, Fig. 6(b) shows the simulated UIS waveforms. In the UIS simulation, to ease the numerical convergence, the V_{GS} signal is directly defined to be a positive value during the avalanche, replicating the avalanche-through-fin process observed experimentally.

IV. Carrier Dynamics in Short-Circuit Test

A. Short-circuit at 400 V

Fig. 7 shows the simulated contours of the electron and hole currents at the SC transient at V_{BUS} = 400 V (t = 10 µs), unveiling the carrier dynamics in the SC condition at a usual V_{BUS} in applications. The short-circuit current is maintained by the electron drift in the n-GaN fin channel, with a peak current density at the foot of the fin channel (Fig. 7(a)). As the G-S junction is forward biased, holes are injected from p-GaN gate to the source near the device surface, comprising a small hole current. The hole dynamics are illustrated by the simulated contours (Fig. 7(b)) and vectors (Fig. 7(c)) of the hole current.

B. Short-Circuit at BV_{AVA}

The carrier dynamics become more complicated in the SC at BV_{AVA}, as the role of impact ionization (I. I.) starts to be significant. As shown in Fig. 8(a), the contour of the electron current density is similar to that in the SC at 400 V, except additional current crowding at the lateral G-S p-n junction near the surface, which suggests a higher level of recombination there. As shown in Fig. 8(b), the I. I. rate is found to peak at the foot of the fin-channel, suggesting the generation of holes there, which is not present in the SC at 400 V.

Resulting from the I. I., two major hole removal and recombination paths are formed, as illustrated in the contours of the hole current density (Fig. 8(c)) and the vectors of the hole current (Fig. 8(d)). In one path, the I. I. generated holes are recombined in the fin channel with the electrons pumped from the source. In the other path, the I. I. generated holes are pushed into the p-GaN gate; subsequently, these holes are either expelled to the source or injected to the top portion of the n-

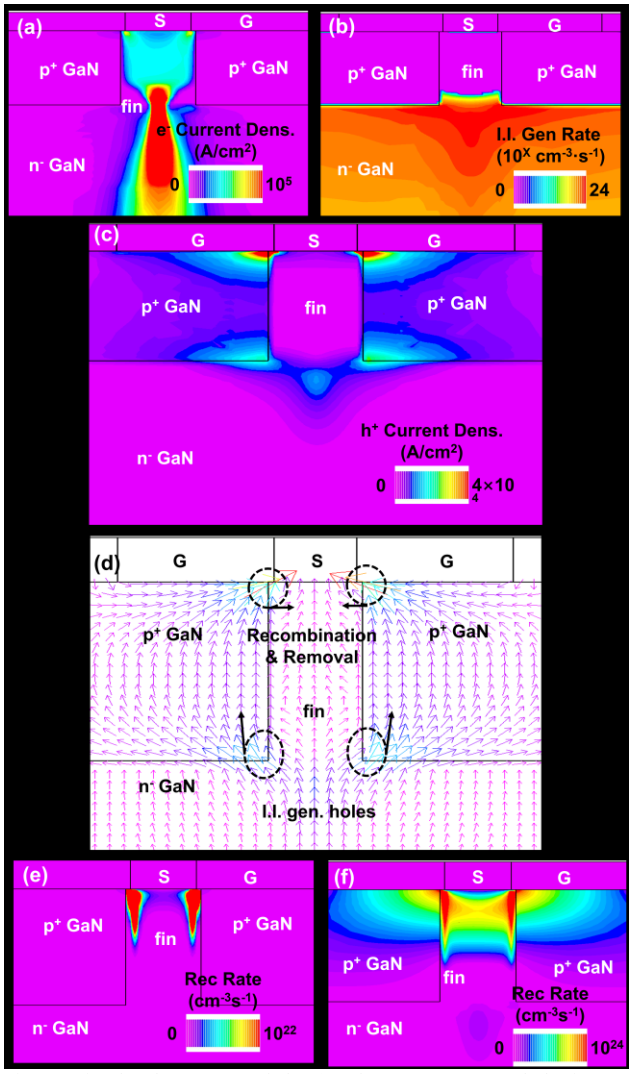

Fig. 8. Simulated contours of the (a) electron current and (b) impact ionization rate under the SC condition at BV_{AVA} (800 V). (c) Simulated contours of the hole current density and (d) the distribution of the hole current vectors under the SC condition at BV_{AVA}, revealing two major removal paths for the I. I. generated holes. Simulated contours of the recombination rate under the SC condition (e) at 400 V and (f) at BV_{AVA}. Recombination rate is much higher at BV_{AVA} due to the removal of the I. I generated holes.

GaN fin channel due to the forward-biased G-S p-n junction. Note that, from the hole current density contours, the second path is dominant. As a further proof of these hole dynamics, Fig. 8(e) and (f) compare the simulated distribution of the recombination rate in the SC transient at 400 V and BV_{AVA}. It is evident that, at BV_{AVA}, a much stronger recombination is present in the G-S junction, validating the enhanced hole injection due to the additional holes generated in the I. I.

It should be mentioned that the effective removal of holes is a key enabling factor for the SC capability near BV_{AVA}. Otherwise, the hole accumulation will lead to the device degradations or failures, which has been observed in lateral GaN HEMTs [24]. Also, it should be noted that at 800 V V_{bus}, the I. I. is expected to be most pronounced at the starting stage of the SC withstanding process. As the device SC prolongs, the

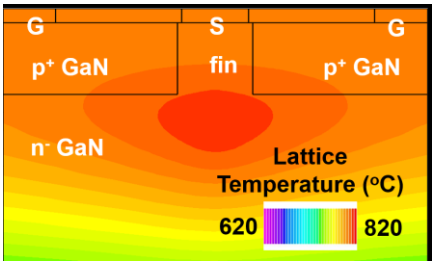

Fig. 9. Simulated lattice temperature contour in the SC test, showing that the peak temperature is located at the foot of the fin-channel.

device T_j increase would raise BV_{AVA}, thereby suppressing I. I. This dynamic protects the Fin-JFET under the SC condition at a V_{BUS} near BV_{AVA}.

C. Intrinsic Current Limitation Mechanisms

As highlighted in Section II.*C*, a key feature of the Fin-JFET when withstanding the SC stress is the fast decrease of $I_{D,sat}$, which is believed to be a critical enabling factor for a much longer t_{SC} as compared to GaN HEMTs. Now we use the TCAD simulations to probe the physics behind this current limiting phenomenon.

Fig. 9 shows the simulated lattice temperature (T_j) contours in the Fin-JFET under the SC condition, revealing a peak T_j located at the foot the fin channel. This peak T_j location coincides with the locations of the peak current density and the narrowest current path (see Figs. 7(a) and 8(a)). Hence, it is evident that the foot of the fin channel is the key limiting location of $I_{D,sat}$ under the SC condition. The local $I_{D,sat}$ at the foot of the fin channel can be calculated from formula (1):

$$I_{D,sat} = q * n * A * v_{sat} \quad (1)$$

where q is carrier charge, n is carrier density, A is the cross-section area of the narrowest current path, and v_{sat} is the saturation velocity. Due to the high electric field at the foot of the channel [25], velocity saturation is expected to be reached.

Fig. 10(a) shows the simulated carrier contour under the SC condition at 400 V. Due to the depletion and high electric field, the n at the foot of the fin channel is lower than that in the top portion of the fin channel. Fig. 10(b) shows the extracted n in a lateral cutline at the foot of the fin channel at V_{DS} of 3 V and 400 V, revealing a smaller n at the foot of the fin channel at 400 V.

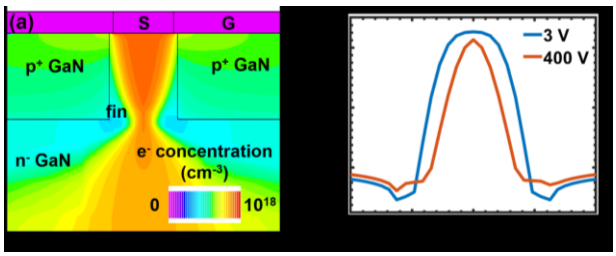

Fig. 10. (a) Simulated electron contour in 400 V short circuit condition. (b) Extracted electron concentration of a lateral cutline at the foot of the fin channel under 3 V and 400 V short circuit condition, revealing a smaller n at 400 V.

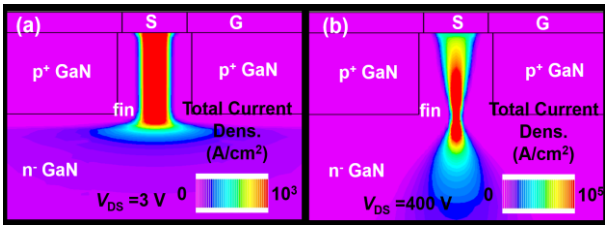

Fig. 11. Simulated contours of the total current density at V_{DS} of (a) 3 V and (b) 400 V. Current path is narrowed at high bias, particularly at the foot of the fin channel, due to the expansion of the depletion region.

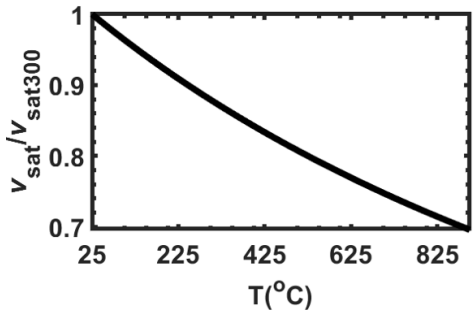

Fig. 12. Calculated v_{sat} dependence on temperature.

At the foot of the fin channel, A is also affected by V_{DS}. Fig. 11 shows the simulated contours of the total current density at V_{DS} of 3 V and 400 V. The width (and A) of the current path at the foot of the fin channel is significantly reduced at high V_{BUS}.

Finally, v_{sat} also decreases with the increased T_j, which can be modeled by the formula (2) [26]:

$$v_{sat}(T) = \frac{v_{sat300}}{(1-B) + B * \left(\frac{T}{300}\right)} \quad (2)$$

where v_{sat300} represents the saturation velocity at T_j = 300 K, and B is a temperature coefficient. For GaN, B is extracted as 0.15 in [27] and [28]. The calculated dependence of v_{sat} on T is plotted in Fig. 12. At the simulated maximum T_j of ~820 °C, v_{sat} decrease to ~ 70% of v_{sat300}, further limiting the $I_{D,sat}$.

The above analyses illustrate the inherent device physics of the Fin-JFET regarding the self-limitation of $I_{D,sat}$. Many of these analyses are also applicable to explaining the excellent SC robustness experimentally reported in SiC JFETs [29]-[32]. In addition to these inherent device physics, the *RC* interface driver used in this work is also favorable to $I_{D,sat}$ limitation. In the SC process, the elevated T_j enhances the forward current of the G-S pn junction and increases I_G, which further increases the voltage drop on R_{SS} and thereby decreases the device V_{GS}.

V. Carrier Dynamics in Avalanche Test

Building on the explained carrier dynamics under the SC condition at BV_{AVA}, we explore the carrier dynamics under the avalanche (UIS) test condition in this section. From the device point of view, these two test conditions both drive the Fin-JFET into a state under concurrence of SC and avalanche; hence the carrier dynamics could be very similar. From the circuit test point of view, there are two major differences between the SC and UIS tests: (a) the UIS circuit allows the DUT's V_{DS} to keep up with BV_{AVA}, which may increase during the test, while the SC circuit fixes the DUT's V_{DS} at V_{BUS}; (b) the *RC* gate driver applies a negative bias in the UIS test but a positive bias in the SC test.

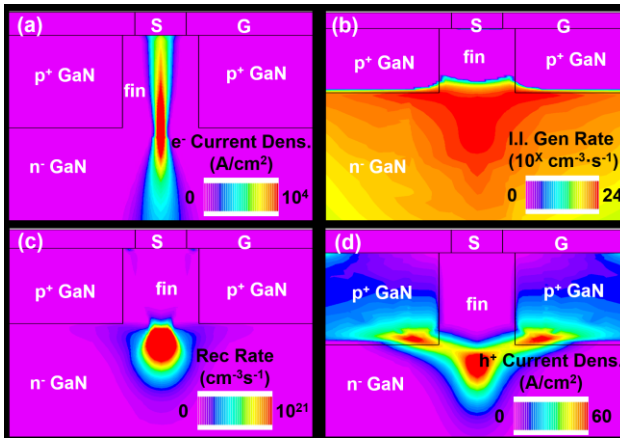

Fig. 13. Simulated contours of (a) electron current density, (b) impact ionization rate, (c) recombination rate, and (d) hole current density under the UIS condition.

Fig. 13 show the simulated contours of current density, I. I. generation rate, and recombination rate under a UIS condition. The contours of electron current (Fig. 13(a)) and I. I. generation rate (Fig. 13(b)) are very similar to those under the SC condition at BV_{AVA} (see Fig. 8(a) and (b)), revealing the same "avalanche through fin" nature.

However, under the UIS condition, the contours of the hole current and recombination rate are different. As shown in Fig. 13(c) and (d), the hole current and recombination rate both peak at the foot of the fin channel, while they peak at the G-S junction close to the surface in the SC test at BV_{AVA} (see Fig. 8(c)-(f)). Under the UIS condition, the I.I.-generated holes are removed through the p-GaN gate without further injection into the n-GaN fin channel. As a result, there is minimal recombination near the source. Because the applied driver voltage is negative, during the UIS test, an I_G flowing out of the gate is constantly needed to maintain the voltage drop on R_{SS} to ensure $V_{GS} \geq V_{th}$. This I_G is supported by the hole removal from the p-GaN gate.

Note that, as I_G is usually small (~mA range), the opposite polarity of I_G is not expected to impact the DUT's robustness in two tests. The device failures under SC and UIS tests both show a FTO signature. The reported critical energy density of the DUT is also similar in these two tests, being ~7.5 J/cm^2 in the SC test [18] and 8~10 J/cm^2 in the UIS test [19].

VI. Failure-to-Open-Circuit Mechanisms

The discussions in Section IV and V suggest that the desirable FTO signature in both SC and UIS tests is correlated to the avalanche-through-fin process in the Fin-JFET. In this section, we explore the device physics enabling the FTO signature of GaN Fin-JFETs in the avalanche-through-fin process. As power MOSFETs usually exhibit a failure-to-short-circuit (FTS) signature in avalanche, we first show the TCAD simulation of a generic MOSFET, and then compare it with the GaN Fin-JFET.

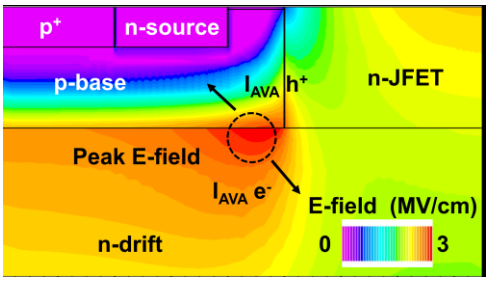

Fig. 14. Simulated electric field contours in the junction region of a SiC MOSFET, and the illustration of the avalanche current. I_{AVA} travels through the main blocking pn junction.

A. Conventional Power MOSFETs

Fig. 14 shows the simulated electric field contours in the junction region of a generic SiC power MOSFET when V_{DS} is close to its BV_{AVA}. This simulation is based on our prior TCAD simulations calibrated for 1.2-10 kV SiC MOSFETs [33], [34]. The location of peak electric field is revealed to be at the junction between the p-base and n-type drift region. Hence, during avalanche, I. I. is expected to peak at this p-n junction with the generated holes being extracted through the p-base and source and the generated electrons being extracted through the drift region and drain. Thus, I_{AVA} flows across this p-n junction, the major electric field blocking junction at BV_{AVA}.

The avalanche failure of a power MOSFET is usually due to the I_{AVA}-induced thermal runaway or the latch-up (i.e., the turn-on of the parasitic npn bipolar junction transistor due to the lateral flow of I_{AVA} in the p-base channel). Owing to the coincidence of the locations of peak I_{AVA} and peak electric field, the I_{AVA}-induced failure would usually lead to the destructive damage of the blocking junction, thereby shorting the drain and source. Similar failure processes are expected in the IGBT. This explains the fact that, in the literature, Si and SiC MOSFETs [35], JFETs [36] and Si IGBTs [37] have all been reported to fail short in avalanche tests.

Note that the FTO signature has also been reported in some SiC MOSFETs at a relatively low V_{BUS} SC test when the thermal failure occurs in the gate oxide layer [38]. However, when V_{BUS} is higher and I. I. happens, the peak current location will transition from the MOS channel to the p-n junction. This causes SiC MOSFETs to show minimal SC capabilities at a V_{BUS} higher than its rated voltage [18].

B. GaN Fin-JFET

Based on the above discussions on power MOSFETs, it is speculated that the key enabling physics for the FTO signature of GaN Fin-JFETs is the spatial separation between the peak I_{AVA} stress and the peak electric field stress. As shown in Figs. 8, 9 and 13, when V_{DS} approaches BV_{AVA}, in either the SC or the UIS test conditions, the major current stress and peak T_j are located in the fin channel. Whereas, as shown in Fig. 15, under these conditions, the peak electric field location is at the G-D p-n junction. The locations of the peak current (and thermal) stress and the peak electric field stress are separated by depletion regions at the foot of the fin channel.

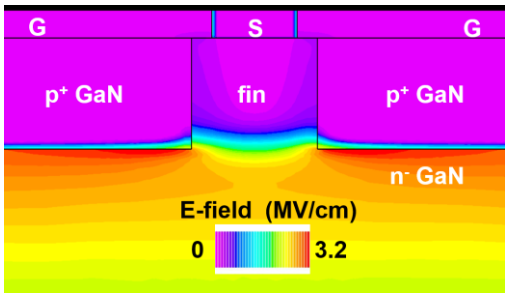

Fig. 15. Simulated E-field distribution in GaN Fin-JFETs at BV_{AVA}.

As presented in Section II, the Fin-JFETs failed in the SC and UIS tests exhibited a shorted G-S, suggesting the failure due to the current (and thermal) stress. As this location is different from the blocking p-n junction, the BV_{AVA} retains, enabling a FTO signature.

VII. Conclusions and Summary

This work presents comprehensive device physics that enables breakthrough SC and avalanche performance recently reported in vertical GaN Fin-JFETs. The Fin-JFET shows an inherent current limitation mechanism, which enables the record high t_{SC} demonstrated in GaN devices. Moreover, the Fin-JFET shows a unique robustness under the concurrence of SC and avalanche, demonstrated in both the UIS test and the SC test at a V_{bus} close to BV_{AVA}. Despite the slightly different hole dynamics within the device under these two test conditions, the key enabling physics is the avalanche-through-fin process, in which the major I_{AVA} path is through the n-GaN fin instead of the blocking p-n junction as present in other power transistors (e.g., MOSFETs). Finally, the spatial separation of the peak I_{AVA} (and thermal) stress from the blocking p-n junction enables a FTO signature of Fin-JFET in SC and avalanche tests. This FTO signature is greatly desirable for power electronics systems. These results also provide many new insights for the robustness of power devices.

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