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ABSTRACT

The outstanding properties of Gallium Nitride (GaN) have enabled considerable improvements in the performance of power devices compared to traditional silicon technology, resulting in more efficient and highly compact power converters. GaN power technology has rapidly developed and is expected to gain a significant market share in an increasing number of applications in the coming years. However, despite the great progress, the performance of current GaN devices is still far from what the GaN material could potentially offer, and a significant reduction of the device on-resistance for a certain blocking voltage is needed. Conventional GaN high-electron-mobility-transistors are based on a single two-dimensional electron gas (2DEG) channel, whose trade-off between electron mobility and carrier density limits the minimum achievable sheet resistance. To overcome such limitations, GaN power devices including multiple, vertically stacked 2DEG channels have recently been proposed, showing much-reduced resistances and excellent voltage blocking capabilities for a wide range of voltage classes from 1 to 10 kV. Such devices resulted in unprecedented high-power figures of merit and exceeded the SiC material limit, unveiling the full potential of lateral GaN power devices. This Letter reviews the recent progress of GaN multi-channel power devices and explores the promising perspective of the multi-channel platform for future power devices.

I. INTRODUCTION

Gallium Nitride (GaN) devices have shown outstanding potential for power conversion applications, thanks to the excellent material properties, such as the large critical electric field and high electron mobility.[1–4] The use of GaN has enabled power devices with much-improved performance compared to the best-in-class conventional Si devices. Currently, the most common GaN power device architecture is based on the lateral High-Electron-Mobility-Transistors (HEMTs), which relies on the difference in polarization fields between GaN and an $Al_xGa_{1-x}N$ barrier to form a high-mobility and large-density two-dimensional electron gas (2DEG) channel. Despite the great potential and recent progress of GaN power technology, the performance of lateral GaN devices is still far from what the material could offer with further improvements, requiring a significant reduction of the specific on-resistance ($R_{ON,sp}$) while maintaining high voltage blocking capability (defined by the breakdown voltage, V_{BR}) in the off-state, which is typically summarized by the Baliga's figure of merit (FOM) as $V_{BR}^2/R_{ON,sp}$.[5,6] To further reduce the device $R_{ON,sp}$, heterostructures with considerably lower sheet resistance (R_{sh}) should be demonstrated. However, a significant decrease in R_{sh} is hindered by the trade-off between the semiconductor mobility (μ) and carrier density (N_s) in conventional structures based on a single 2DEG channel.

A promising approach to address the N_s vs μ trade-off is the use of multi-channel heterostructures,[7–18] in which several barrier/channel layers are stacked to achieve multiple 2DEGs [Figs. 1(a)–1(c)]. The distribution of a large number of carriers in several high-mobility parallel channels enables increasing N_s without degrading μ and results in a significant reduction in R_{sh} with respect to conventional single quantum-well structures. However, increasing N_s results in a larger negative threshold voltage (V_{TH}) and reduces the V_{BR} due to the more difficult electric field management, which are major challenges for power devices. In particular, common planar gating and field plate (FP) techniques that are well adapted for single-channel structures no longer work for high N_s multi-channel structures, due to the more challenging depletion of carriers in the multiple channels.[9,13,15] New 3D gate and field plate architectures have been successfully proposed

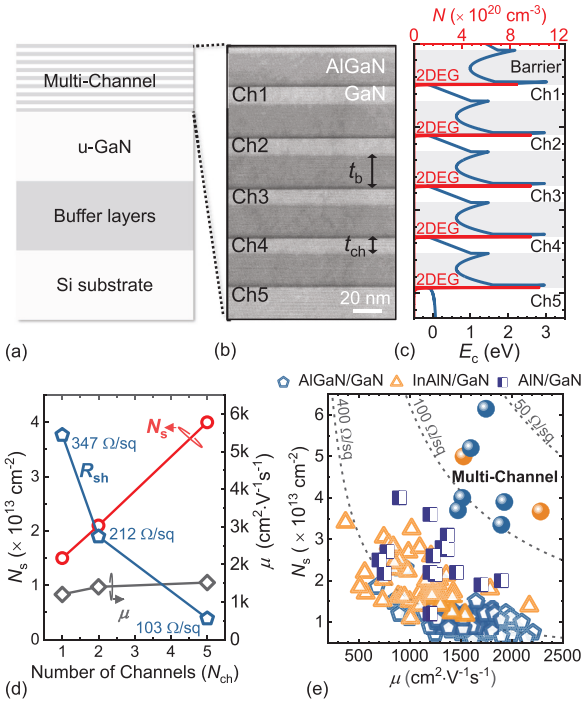

FIG. 1. (a) Schematics and (b) TEM cross section of a multi-channel heterostructure and (c) corresponding band structure, and (d) N_s, mobility, and R_{sh} as a function of the number of channels in multi-channel structures. (e) N_s vs μ for single- and multi-channel (round points)[10,14–16,28] heterostructures in the literature. Reproduced with permission from Nela *et al.*, Nat. Electron. **4**, 284–290 (2021). Copyright 2021 Springer Nature.

to solve these challenges.[9,12,13,15–17] Based on these concepts, power devices realized on a multi-channel platform have shown excellent potential with significantly improved performance compared to single-channel devices.[9,12,13,15–20] In addition, multi-channel devices have already successfully demonstrated key features for any power device such as enhancement-mode operation,[15,20,21] large blocking voltage capabilities with reduced leakage current,[15,17,19] and good stability during switching operation.[15,18,21] These results validate the enormous potential of multi-channel GaN power devices as a viable and promising solution for high-performance future power devices. The goal of this Letter is to review the different architectures and solutions for multi-channel devices proposed in the literature and to discuss the future perspective of this technology.

II. MULTI-CHANNEL HETEROSTRUCTURE DESIGN

A key feature of the multi-channel platform is the ability to significantly increase the carrier concentration without degrading the mobility. In conventional single-channel heterostructures, there is a trade-off between N_s and μ since largely populated channels suffer from increased carrier scattering,[22] which reduces μ and ultimately limits the minimum achievable sheet resistance. By spreading a large N_s into several vertically stacked channels, this trade-off can be overcome, which enables increasing N_s without impacting the mobility of the structure, thus achieving much reduced R_{sh} [Fig. 1(d)]. Several multi-channel structures based on this approach have been demonstrated, clearly showing the potential of this technology to reach unprecedented R_{sh}[7,14,15,23–28] [Fig. 1(e)].

However, meticulous care should be taken in properly designing the multi-channel heterostructure to achieve the desired sheet resistance. In particular, several variables can be adjusted, including barrier (t_b) and channel (t_{ch}) thicknesses, doping, and barrier material [Figs. 1(a) and 1(b)]. Two main requirements should be considered when choosing the best set of variables, namely, populating all embedded channels and minimizing the total thickness of the stack to facilitate the fabrication of the device.

Different approaches have been proposed to address these challenges, i.e., undoped structures,[16,28] *n*-type doping of the barrier,[12,13,15] and high-polarization barrier material compared to conventional AlGaN (e.g., InAlN[7,10] or AlN[7]), each of which presents advantages and drawbacks.

The use of an intrinsic structure requires a clear understanding of the polarization contribution at each barrier/channel interface and a careful tuning of the GaN channel and barrier thickness to avoid unpopulated buried channels.[29] However, multi-channel structures based on this approach have been successfully demonstrated, showing sheet resistances down to 58 Ω/sq for a ten-channel structure.[28] The main advantage of such an approach is the absence of any dopants. On the contrary, these structures typically require a thick structure, with large periods ($t_{ch} + t_b$) ∼ 80–100 nm. Such a thick stack, if several channels are considered, poses challenges to the device fabrication, especially in the case of tri-gate structures, due to the large aspect ratio required.

An alternative strategy consists of doping the AlGaN barrier.[9,12,13,15,18,26] In this case, the carrier concentration is determined by the density of dopants introduced rather than by the polarization contributions. This enables easier control of N_s and also a considerable reduction of the required stack period, to only ∼40 nm. For instance, multi-channel heterostructures with R_{sh} of 83 Ω/sq and a total thickness of only 130 nm have been demonstrated by this method.[9,15] Yet, this strategy involves the introduction of a large density of dopants in the barrier, which may impact the blocking capabilities of the device.

Finally, a third approach is to employ materials with larger polarization fields compared to conventional AlGaN as the barrier layer, such as AlN or InAlN [Fig. 2(a)]. This can be applied both to doped and undoped structures and enables achieving larger N_s with a reduced stack thickness[29] [Fig. 2(b)]. For instance, R_{sh} of only 37 Ω/sq has been demonstrated by a ten-channel undoped AlN/GaN heterostructure with a total stack thickness of ∼500 nm.[7] Moreover, the use of barrier material such as lattice-matched $In_{0.17}AlN$ enables, in principle, the growth of as many channels as desired[10] without issues regarding strain relaxation or cracking, which can occur in case of large stress is present in the structure.[10,30] The main challenge of such approaches is to achieve large electron mobility and good control of the growth quality in AlN and InAlN structures, which can be challenging by metalorganic chemical vapor deposition (MOCVD). However, development in this field is ongoing, and multi-channel structures based on lattice-matched materials, such as $In_{0.17}AlN$, have a great potential to further increase the number of channels and reduce the overall R_{sh}.

Overall, multi-channel structures provide a large number of variables that can be adjusted to achieve optimal features for specific

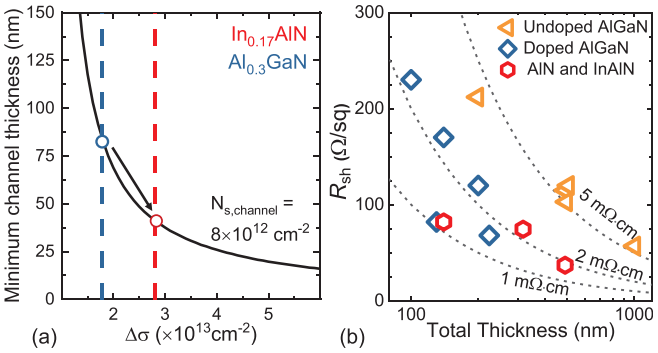

FIG. 2. (a) Minimum channel thickness for intrinsic structures depending on the polarization difference between GaN and barrier material. (b) R_{sh} as a function of the total channel stack thickness for multi-channel structures without doping,[15,16,28] with doping,[15,26] and with AlN or InAlN barrier.[7,10,68]

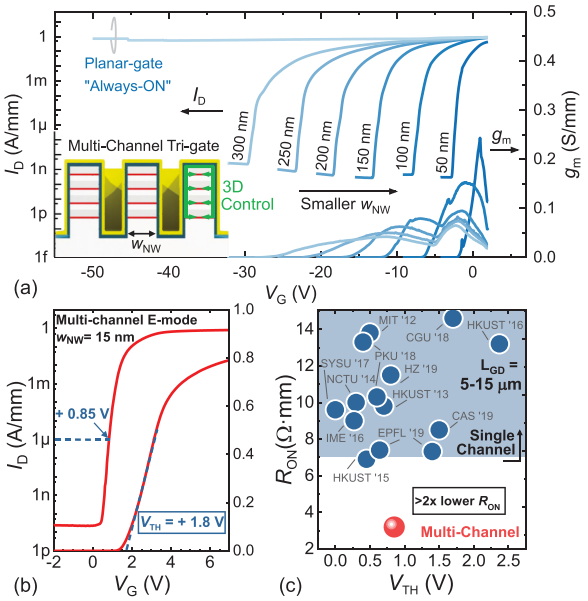

FIG. 3. (a) Transfer curves for multi-channel Tri-gate devices having different nanowire widths. (b) Transfer curve for an E-mode multi-channel device with w_{NW} of 15 nm. (c) V_{TH} vs R_{ON} benchmark for single- and multi-channel E-mode HEMTs. Reproduced with permission from Nela *et al.*, Nat. Electron. **4**(4), 284–290 (2021). Copyright 2021 Springer Nature.

applications, offering a complete set of tools to the device designer. All of these several different strategies presented in the literature have shown the great potential of the multi-channel platform to significantly reduce the sheet resistance without sacrificing the mobility, thus resulting in a promising platform for high-performance power devices.

III. MULTI-CHANNEL CONTROL AND V_{TH} ENGINEERING

The much-improved conductivity enabled by the multi-channel platform would be of little value if it could not be controlled and modulated. However, the multi-channel 3D structure requires new approaches to achieve proper control of all of the embedded channels. In particular, conventional planar gates are not able to deplete all embedded channels simultaneously due to the electric field shielding from the topmost channels and the large separation between the gate electrode and the bottom 2DEG channels. Multi-channel devices based on planar gates have shown very negative threshold voltages [Fig. 3(a)] and breakdown of the gate stack even before turning off all multiple channels, depending on the specific heterostructure. Yet, the ability to control all of the channels and to tune the device V_{TH} is crucial both to achieve high ON/OFF ratio transistors, ideally with enhancement-mode (E-mode) operation, and to properly design field plates to manage the high electric fields.

Under this point of view, the use of tri-gate architectures,[8,31–33] in which the gate region is nanostructured in nanowires conformably covered by a gate metal [inset in Fig. 3(a)], has shown excellent potential to tune V_{TH} also in multi-channel devices, for both RF[8] and power applications.[13,15] The tri-gate structure around the multi-channel nanowires offers a superior electrostatic control, thanks to its 3D architecture, which enables simultaneous side-gate control of all of the embedded channels.

This results in a shift of the threshold voltage toward less negative values and in an improved ON/OFF ratio as the width of the nanowire is reduced and the capacitive coupling through the tri-gate sidewalls increases[9,13,15] [Fig. 3(a)]. Such an approach can even be used to achieve positive V_{TH} and E-mode operation [Fig. 3(b)], which is fundamental for any power transistor to ensure fail-safe operation. As shown in Ref. 15, when the nanowire width is reduced to a few tens of nanometers, the carrier depletion from the nanowire sidewalls becomes dominant, resulting in fully depleted nanowires below ~30 nm, despite the very large N_s of the multi-channel structure (3.9×10^{13} cm^{-2} for this heterostructure). Based on this approach and a large work function gate metal,[33] full E-mode devices with V_{TH} of 1.8 V from linear extrapolation (0.85 V at 1 μA/mm) have been demonstrated, showing the feasibility of E-mode multi-channel devices[15] [Fig. 3(b)]. In addition, excellent V_{TH} stability both at high temperatures and during switching operation has been presented for these devices, proving the robustness of such an approach.[15,21] Multi-channel nanowires have also been shown to maintain large mobility even for small widths of a few tens of nanometers,[15] which ensures minor degradation of the device's on-state performance. Thanks to the much reduced multi-channel sheet resistance, E-mode devices based on this approach have resulted in on-resistance (R_{ON}) of only 3.2 Ω mm for L_{GD} of 10 μm, corresponding to an unprecedented low $R_{ON,sp}$ of 0.46 mΩ cm^2, which represents a significant advance compared to single-channel devices present in the literature and leads to a considerable improvement of the R_{ON} vs V_{TH} trade-off [Fig. 3(c)].

An alternative approach to achieve multi-channel E-Mode HEMTs has been recently proposed by employing an integrated Cascode structure. As shown in Figs. 4(a)–4(c), this Multi-Channel Monolithic-Cascode HEMT (MC^2-HEMT) monolithically integrates a low-voltage (LV), normally-off HEMT based on a single 2DEG channel, and a high-voltage (HV), normally-on HEMT based on stacked 2DEG multi-channel.[20] A plurality of Ohmic vias functions as the effective drain for the single-channel LV-HEMT and the source for the multi-channel HV-HEMT. The HV-HEMT gate is connected to the LV-HEMT source, forming a cascode, i.e., a configuration that employs the LV device for the gate control of the HV device.[34] A gate

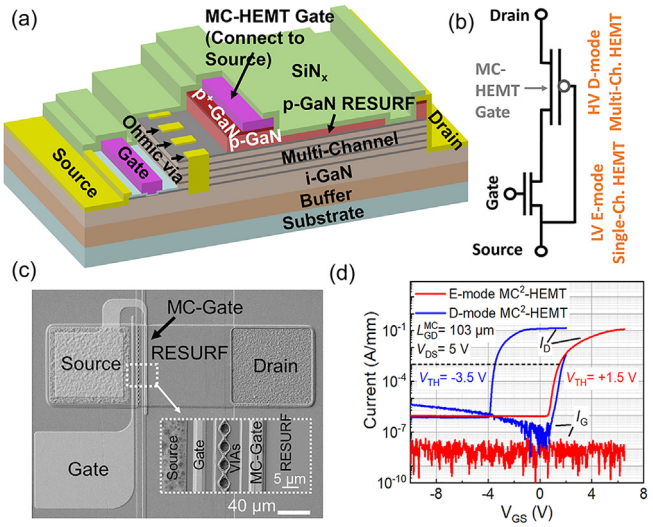

FIG. 4. (a) Schematic and (b) equivalent circuit model of the MC^2-HEMT. (c) SEM top-view image of a fabricated MC^2-HEMT highlighting the integrated Cascode configuration. (d) Transfer characteristics of a 10-kV MC^2-HEMT without and with gate recess in the LV-HEMT, resulting in D-mode and E-mode operations, respectively. Reproduced with permission from Xiao *et al.*, in *IEDM Technical Digest* (2021), p. 5.5. Copyright 2021 IEEE.

recess is implemented in LV-HEMT to realize the normally off operation [Fig. 4(d)]. This MC^2-HEMT can exploit the low sheet resistance of multi-channels, realize a normally off gate control, and completely shield the gate region from the high electric field. Note that, in addition to Ohmic vias, the LV- and HV-HEMTs could be also connected through a regrown n-GaN contact or AlGaN/GaN channel at the sidewall. Future work is needed to explore these variations in the interconnect design.

As compared to the fin-gate counterparts,[35] this integrated cascode structure obviates the need for the sub-micron lithography at a price of the additional on-resistance from the LV-HEMT. Hence, the MC^2-HEMT is particularly attractive for multi-kilovolts devices. The MC^2-HEMTs show a threshold voltage of over 1.5 V at 1 mA/mm and a low $R_{ON,sp}$ of 40 mΩ cm^2 for a gate–drain distance for the HV-HEMT (L_{GD}^{MC}) of 103 μm (which corresponds to a V_{BR} over 10 kV).

IV. OFF-STATE ELECTRIC FIELD MANAGEMENT

In addition to small R_{ON} and E-mode operation, power devices need to ensure high V_{BR} by properly managing the large off-state electric fields. Efficient field management is even more important for lateral multi-channel devices due to the large N_s and the highly conductive structure. The 3D structure and enhanced carrier concentration of the multi-channel platform require novel strategies to this end since conventional FPs are typically not suitable for multi-channel devices. Indeed, as shown in Fig. 3(a), devices with a planar gate electrode either show very negative V_{TH} or break before even being depleting all channels,[15] depending on the specific multi-channel heterostructure. For this reason, a conventional, oxide-based, planar FP is often not effective in protecting the gate/anode electrode and results in an early breakdown of the device. An effective strategy that has been proposed to address this issue is the use of tri-gate and slanted tri-gate FPs[36,37] [Fig. 5(a)]. By tuning the width of the nanowire, the V_{TH} of the tri-gate FP can be shifted to smaller, less negative values [Fig. 3(a)], which avoids any breakdown of the FP stack and more effectively protects the gate electrode. Moreover, by designing a nanowire with a slanted profile, which can be easily achieved in a single lithographic step, the threshold voltage of the tri-gate FP can be gradually increased, greatly improving the electric field distribution [Fig. 5(b)]. Multi-channel devices on GaN-on-silicon substrates based on this approach have shown greatly improved V_{BR} up to 1300 V compared to planar FPs, along with low leakage current, well below 1 μA/mm for L_{GD} of 10 μm [Fig. 5(c)], leading to state-of-the-art high-power figures of merit of 4.6 GW cm^{-2} for D-mode devices and 3.8 GW cm^{-2} for E-mode devices.

In addition to the excellent dc performance, multi-channel devices can also achieve promising switching behavior with reduced current collapse, which is fundamental for any power device. By properly passivating the nanowire sidewalls with a conformal Si_3N_4 layer (left inset in Fig. 6), multi-channel devices with reduced dynamic on-resistance ($R_{ON,dyn}$) were demonstrated, up to large off-state stress voltages[18] (Fig. 6). A similar increase in $R_{ON,dyn}$ compared to reference single-channel devices was achieved based on academic processes[18] (Fig. 6), which suggests that further reduction of the current collapse in multi-channel devices down to the level of current commercial HEMTs is possible by optimizing the process and passivation layer. While further work is required to investigate the exact impact of the C-doped GaN buffer on $R_{ON,dyn}$ in multi-channel devices, some considerations can be drawn. On the one hand, multi-channel heterostructures can be grown employing the same buffer layer as for conventional

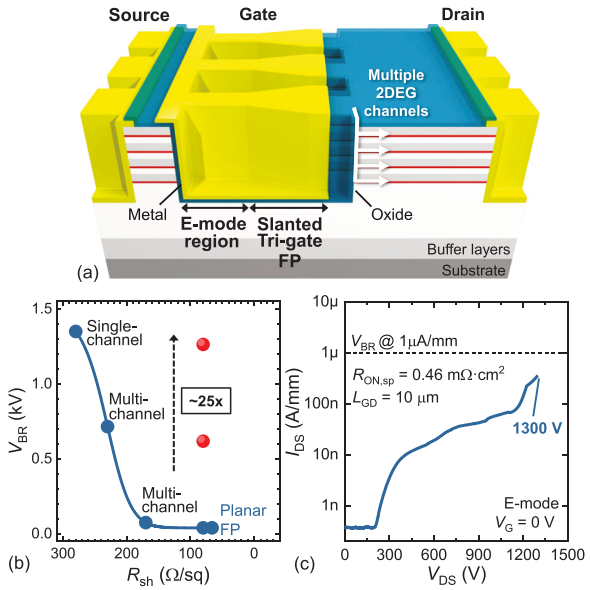

FIG. 5. (a) Schematics of a multi-channel device with a slanted tri-gate field plate. (b) V_{BR} as a function of the heterostructure sheet resistance for devices with conventional planar FPs, tri-gate FP, and slanted tri-gate FP. (c) Off-state current as a function of the drain voltage for an E-mode multi-channel device based on a tri-gate architecture. Reproduced with permission from Nela *et al.*, Nat. Electron. **4**(4), 284–290 (2021). Copyright 2021 Springer Nature.

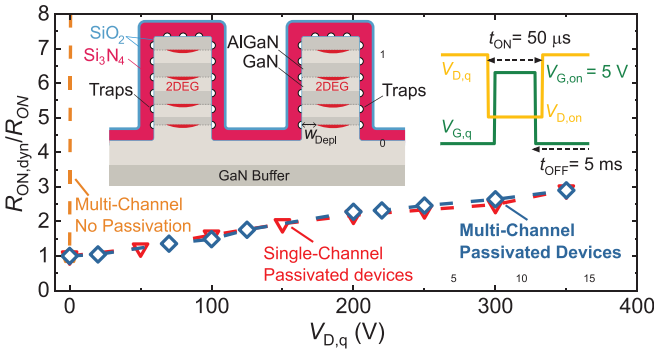

FIG. 6. Normalized dynamic on-resistance as a function of the drain off-state voltage stress for multi-channel devices and single-channel references. The top-left inset shows the conformal passivation layer around the multi-channel nanowires, while the top right inset presented the double pulse measurement employed to determine $R_{ON,dyn}$. Reproduced with permission from Nela *et al.*, IEEE Electron Device Lett. **42**(1), 86–89 (2021). Copyright 2021 IEEE.

single-channel power devices, which enables adopting the same strategies to reduce the impact of the C-doped buffer on $R_{ON,dyn}$.[3,38] On the other hand, as shown in Fig. 3(a), a planar gate electrode is not effective in modulating all of the embedded channels. For the same reason, one could expect that the impact of the back-gating mechanism from the C-doped buffer would mainly affect the 2DEG concentration of the bottom channel without reducing significantly the upper 2DEGs, thus resulting in a milder impact on $R_{ON,dyn}$ compared to single-channel devices.

Alternative strategies to manage the off-state field have also been proposed based on a *p*-type material acting as a field plate. Inspired by the efficacy of using p–n junctions for E-field management in vertical devices, e.g., Junction Barrier Schottky (JBS) diodes[39,40] and JFETs,[41,42] an alternative edge termination for multi-channel devices using the epitaxial *p*-GaN has been proposed [Fig. 7(a)].[16] Benefited from the vertical depletion enabled by the p–n junction, the E-field lines spread out, and their distribution becomes more uniform. The peak E-field is moved from the Schottky contact to the *p*-GaN edge, thereby shielding the Schottky contact from the high electric field. Meanwhile, the *p*-GaN compensates for the 2DEG charges near the contact, further reducing the E-field gradient. This *p*-GaN termination is compatible with the *p*-gate HEMT foundry process and can potentially allow the hole injection, and thus, high device robustness.[43]

In addition to suppressing the E-field crowding at the device edge, improving the average E-field in the lateral "drift region" is also critical to upscaling V_{BR}. Super-junction and reduced-surface-field (RESURF) structures have been employed in conventional single-channel power devices to reduce net charges and E-field gradients.[44] A *p*-GaN RESURF structure of a similar nature has been proposed for the multi-channel wafers comprising net donors,[17] as shown in Fig. 7(b). As compared to the *p*-GaN termination, this RESURF layer extends to near the cathode, and its acceptor charges balance the net donor charges in the multi-channel at high voltage.[17] This charge balance can be experimentally realized by controlling the *p*-GaN thickness. This RESURF design has enabled a doubling of the average lateral E-field. The multi-channel Schottky barrier diodes (SBDs) on GaN-on-sapphire substrates, with a 123-μm anode-to-cathode

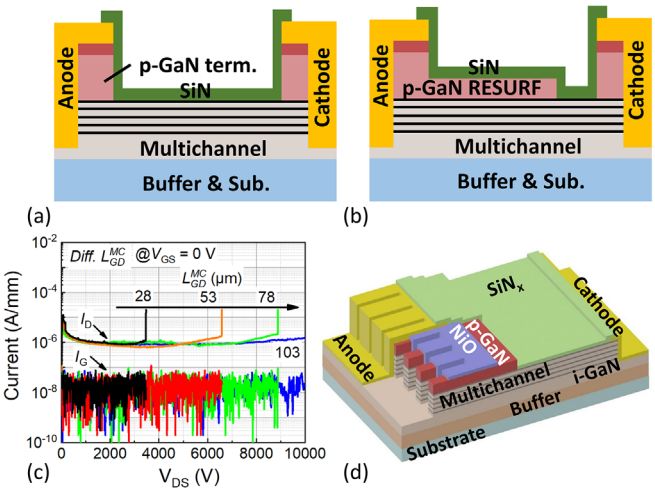

FIG. 7. Schematic of multi-channel diodes with (a) *p*-GaN edge termination and (b) *p*-GaN RESURF structure. (c) Off-state I–V characteristics of the MC^2-HEMT employing a *p*-GaN RESURF layer as a function of the gate-to-drain distance. (d) Schematics of a multi-channel device with a 3D junction-fin-anode. Part (c) reproduced with permission from Xiao *et al.*, in IEDM Technical Digest (2021), p. 5.5. Copyright 2021 IEEE.

distance (L_{AC}), show a V_{BR} over 10 kV and a R_{ON} of 39 mΩ cm^2, which is 2.5-fold lower than the R_{ON} of the state-of-the-art 10-kV SiC JBS diodes. Applied to the MC^2-HEMTs, this technique enables a large average lateral E-field of 1.24 MV/cm and a high V_{BR} over 10 kV [Fig. 7(c)][20] with a specific R_{ON} of 40 mΩ cm^2, which is 2.5-fold smaller than that of 10 kV SiC MOSFETs and below the 1D SiC unipolar limit.[20] The MC^2-HEMTs with various V_{BR} were reported to show the highest Baliga's FOMs in all 6.5-kV+ power transistors.[20]

The leakage current reduction, especially in SBDs, is another challenge facing multi-channel devices due to the concurrence of high E-field and parallel current channels. Also, under this point of view, tri-gate technology has shown great performance. By tuning the width of the tri-gate, the threshold voltage of the tri-gate FP can be precisely adjusted [Fig. 3(a)], and the voltage drop over the Schottky barrier minimized.[37,45,46] Based on this approach, tri-anode/tri-gate multi-channel SBDs have demonstrated very low leakage current ~1 nA/mm up to off-state voltages of 600 V.[12] In addition, tri-gate technology can also be combined with other techniques, such as the use of a *p*-type material,[47] to ease the lithographic requirements. For instance, a 3D junction-fin-anode structure was recently proposed.[19] Fig. 7(d) comprises p–n junctions wrapping around the multi-2DEG-fins, which is similar to the recently demonstrated junction tri-gate and can provide a stronger depletion of the 2DEG channel as compared to planar p–n junctions.[48–50] At reverse biases, the junction-fin shields the Schottky contact from the high biases; the leakage current of the entire multi-channel diode can be made equal to that of a single-channel sidewall SBD biased at a few volts.[19] In the prototyped device, the junction-fin structure comprises *p*-GaN on top of the fin and p-type nickel oxide at the fin sidewalls.[19] The resulting SBD shows a V_{BR} up to 5.2 kV, a specific R_{ON} of 13.5 mΩ cm^2, a current up to 1.5 A, and a leakage current of 1.4 μA/mm at 80% V_{BR}.[19]

In conclusion, the several strategies proposed in the literature showcase the promise of multi-channel technologies for power

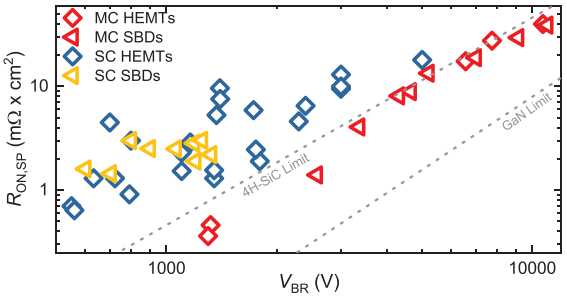

FIG. 8. $R_{ON,SP}$ vs V_{BR} benchmark for state-of-the-art single (SC) and multi-channel (MC) GaN HEMTs and SBDs. The GaN limit has been evaluated for $R_{sh} = 300$ Ω/sq.

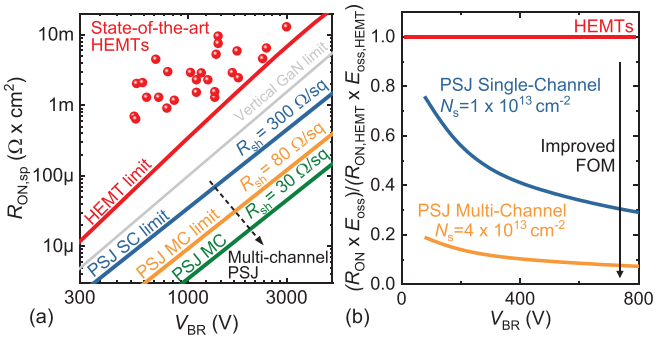

FIG. 9. (a) $R_{ON,SP}$ vs V_{BR} benchmark for HEMTs and PSJs with single and multiple channel heterostructures (SC and MC, respectively). The solid lines represent the calculated theoretical limits for each architecture, while the performance of state-of-the-art HEMTs single-channel devices in the literature is reported in red dots. (b) Ratio between the $R_{ON} \times E_{oss}$ figure of merit for single- and multi-channel PSJs compared to conventional HEMTs. Reproduced with permission from Nela *et al.*, IEEE J. Electron Devices Soc. **9**, 1066 (2021). Copyright 2021 Authors, licensed under a Creative Commons Attribution (CC BY) license.

devices, resulting in a considerable improvement of the $R_{ON,SP}$ vs V_{BR} trade-off for a wide range of voltage ratings, surpassing the 1D 4H-SiC material limit and leading to unpreceded high-power figures of merit (Fig. 8).

V. FUTURE PERSPECTIVES

Despite the significant progress presented above, multi-channel technology still presents several promising future directions open to be explored. A very interesting perspective is represented by applying the polarization super-junction (PSJ) concept[51–56] in which a charge-balanced drift region leads to an ideally flat off-state electric field profile. Multi-channel PSJs would enable a complete decoupling of the on-resistance from the breakdown voltage, resulting in a tremendous improvement of both the $R_{ON,sp}$ vs V_{BR} and R_{ON} vs E_{oss} figures of merit[51,57] [Figs. 9(a) and 9(b)], where E_{oss} is the energy stored in the device output capacitance. Different approaches can be followed to achieve multi-channel PSJs. On the one hand, an undoped multi-channel heterostructure naturally results in charge balance between holes in the two-dimensional hole gases (2DHGs) and electrons in the 2DEGs due to the matching polarization charges.[51,57] On the other hand, alternating *n*- and *p*-type doping of the barrier and channel, similarly to conventional super junctions, has also been proposed,[58] which is, however, challenging for GaN due to the inefficient activation in *p*-GaN doping. In addition to the heterostructure design, further improvements of the contact to the embedded 2DHGs are required, either by regrowth of a *p*-GaN layer or by proper design and annealing of the metal stack. Despite their difficulty, these technological challenges are possible to be overcome in a short time and a successful demonstration of multi-channel PSJs would result in a groundbreaking improvement of the dc and switching performance of the device, with an impact similar to super junctions for silicon devices.

In addition to more established GaN-based n-FETs, multi-channel structures can be very beneficial also for material platforms suffering from relatively low conductivity. For instance, GaN *p*-FETs based on a multi-channel approach have shown improved current capabilities,[25,59] representing a possible solution toward GaN CMOS logic.

Moreover, the multi-channel platform is particularly promising for ultra-wide bandgap (UWBG) semiconductors such as gallium oxide (Ga_2O_3), high-Al AlGaN, AlN, and diamond, which are being actively investigated for the next generation of power electronics.[60] Owing to a larger bandgap, these materials promise a theoretical critical electric field (E_C) higher than that of GaN and SiC. Several UWBG 2D carrier channels are available, including the 2DEG in $Al_xGa_{1-x}O/Ga_2O_3$ and $AlN/Al_xGa_{1-x}N$ as well as the 2DHG in diamond. A peak electric field higher than the E_C of GaN has been experimentally demonstrated in several high-voltage UWBG devices.[61–63]

Despite the high E_C, the resistivity of the demonstrated UWBG channels is still much higher than the GaN counterpart. For example, the R_{sh} of the state-of-the-art AlGaO/GaO and high-Al AlGaN channels are 5300–13 000[64–66] and 1800–8000 Ω/sq,[67] respectively, which are about 5–30 times higher than the R_{sh} of the single-channel AlGaN/GaN. Hence, the multi-channel platform is an excellent candidate for UWBG power devices, as it can exploit the high E_C of UWBG materials while effectively reducing the channel R_{sh}. Moreover, almost all the epitaxy and device technologies for GaN-based multi-channel devices can be seamlessly transferred to future UWBG counterparts.

Due to the distinct maturity levels of these different material systems, it is difficult to identify an ultimately superior candidate. To determine the potential of multi-channel UWBG devices, one can consider a practical $R_{ON,sp}$ vs V_{BR} limit, i.e., $R_{ON,sp} = R_{C,sp} + R_{sh}V_{BR}^2/E_{AVE}^2$,[16] where $R_{C,sp}$ is the specific contact resistance and E_{AVE} is the average lateral electric field. A UWBG HEMT with a twofold higher E_{AVE} (~2.5 MV/cm) is predicted to exceed the performance of a single-channel GaN HEMT by stacking three or more channels. To enable a comparable performance with similar channel numbers, a threefold higher E_{AVE} needs to be realized in the UWBG HEMTs. These trade-offs provide useful guidance for future developments of the UWBG multi-channel epitaxy and devices.

In conclusion, multi-channel devices offer tremendous potential for future power devices. GaN-based multi-channel devices have demonstrated unprecedented high-power figures of merit in a wide voltage range, significantly outperforming conventional single-channel devices and surpassing the performance 1D limit of 4H-SiC. Most importantly, such performances have been achieved in combination with key requirements for power devices such as E-mode operation and stable switching performance, which proves the potential of the technology. On the horizon, the application of the multi-channel platform to new technologies, such as polarization super junctions and UWBG

semiconductors, promises further groundbreaking improvements in the performance of future multi-channel power devices.

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AUTHOR DECLARATIONS

Conflict of Interest

The authors have no conflicts to disclose.

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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