(Invited) Breakthrough Avalanche and Short Circuit Robustness in Vertical GaN Power Devices

ECS Transactions, 108 (6) 11-20 (2022)
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(Invited) Breakthrough Avalanche and Short Circuit Robustness in Vertical GaN Power Devices

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Power devices are highly desirable to possess excellent avalanche and short-circuit (or surge-current) robustness for numerous power electronics applications like automotive powertrains, electric grids, motor drives, among many others. Current commercial GaN power device, the lateral GaN high-electron-mobility transistor (HEMT), is known to have no avalanche capability and very limited short-circuit robustness. These limitations have become a roadblock for penetration of GaN devices in many industrial power applications. Recently, through collaborations with NexGen Power Systems (NexGen), Inc., we have demonstrated breakthrough avalanche, surge-current and short-circuit robustness in NexGen's vertical GaN p-n diodes and fin-shape junction-gate field-effect-transistors (Fin-JFETs). These large-area GaN diodes and Fin-JFETs were manufactured in NexGen's 100 mm GaN-on-GaN fab. The demonstrated avalanche, surge-current and short-circuit capabilities are comparable or even superior to Si and SiC power devices. Additionally, vertical GaN Fin-JFETs were found to fail to open-circuit under avalanche and short-circuit conditions, which is highly desirable for the system safety. This talk reviews the key robustness results of vertical GaN power devices and unveils the enabling device physics. Fundamentally, these results signify that, in contrast to some popular belief, GaN devices with appropriate designs can achieve excellent robustness and thereby encounter no barriers for applications in electric vehicles, grids, renewable processing, and industrial motor drives.

Introduction

Gallium nitride (GaN) has recently become a mainstream material for power electronics. Lateral GaN high-electron-mobility transistors (HEMTs) have been commercialized for 15-650 V power electronics applications. They are now seeing rapid adoption in power supplies, data centers, Lidar systems, and fast charging systems in consumer electronics (1). In addition to lateral GaN HEMTs, vertical GaN devices have been extensively studied for 600-1700 V applications, and several devices are close to commercialization (2-4). These vertical GaN devices can be fabricated on either large-diameter free-standing GaN substrates (5) or low-cost Si or sapphire substrate (4). On the horizon is the high-voltage (1.7-10 kV) GaN devices based on the vertical structure or lateral multi-channel platform (6). Multi-channel GaN Schottky barrier diodes (7-9) and enhancement-mode (E-mode) HEMTs (10) have been demonstrated up to a voltage class of 10 kV. The 10

kV GaN diodes and transistors have shown performance well below the 1-D SiC limit (9,10). These results show the great potential of GaN power devices for a greatly expanded application space.

To expand the application of all commercial and R&D GaN devices, their robustness under abnormal operations is a key gap to address. For power transistors, typical robustness requirements include the avalanche capability, which evaluates the device capability to withstand overvoltage and surge-energy stress, and short-circuit capability, which evaluates the device capability to withstand overcurrent while blocking high voltage or being in forward/reverse conductions. For power rectifiers, in addition to avalanche capability, surge-current robustness is essential, which evaluates the diode capability to withstand abnormally high forward current. These capabilities are particularly indispensable for the applications that require device stressful operations, such as electric vehicle automotive powertrains, electric grids, and motor drives.

Unfortunately, the robustness of commercial lateral GaN HEMTs is known to be inferior to SiC and Si power transistors. GaN HEMTs have no avalanche capability and rely on their overvoltage margin to withstand the overvoltage and surge-energy stress in power circuits (11-14). Different from the nondestructive avalanche breakdown, GaN HEMTs fail destructively in overvoltage and surge energy stress with a inconstant boundary dependent on switching frequency (13-15). In addition, GaN HEMTs have limited short-circuit capabilities. The short-circuit withstanding time of all commercial 600/650 V rated GaN HEMTs is below 1 μs at a bus voltage of 400 V, which is much smaller than the typical 10-μs system requirement (16). Finally, there is no report on the robustness of lateral AlGaN/GaN power diodes. Due to these facts, there is a popular belief in the power electronics community that GaN devices are inherently unrobust.

Recently, our group, in collaboration with NexGen, has demonstrated breakthrough avalanche, short-circuit, and surge-current robustness in the vertical GaN rectifiers and transistors manufactured by NexGen on 100-mm GaN-on-GaN fab. We made several world's first demonstrations, e.g., the first avalanche capability in GaN transistors, the first short-circuit robustness with a withstanding time 10× higher than GaN HEMTs, the first surge-current capability in GaN rectifiers, and the first failure-to-open-circuit signature in avalanche. Most of these demonstrations are based on power circuits instead of static device characterizations, thereby showing the device true robustness in applications. In addition, industrial packaged devices are used in all these demonstrations. Hence, our results convincingly show the viability of realizing a robustness in vertical GaN devices that is comparable or even superior to Si and SiC transistors.

Avalanche of GaN p-n Diodes: Capabilities and Criteria

P-n junction is a building block for many advanced power rectifiers [e.g., junction barrier Schottky diodes (17)] and transistors (e.g., MOSFETs, JFETs, IGBTs), Hence, the robustness of p-n junction diodes has become critical performance indicators for a group of power devices built on a common material platform (18). We first studied the avalanche and surge current robustness of vertical GaN p-n diodes and explored their possible trade-offs with reverse recovery.

Fig. 1(a) shows the schematic of NexGen's 1.2 kV vertical GaN p-n diodes. These diodes were assembled in a standard TO-220 package with an active device area of 1.39 mm^2 (18,19). Static characterizations show a turn-on voltage close to GaN's bandgap, a non-destructive breakdown voltage (BV) increasing with temperature (Fig. 1(b), and a differential on-resistance (R_{ON}) decreasing with temperature (Fig. 1(c)). The positive temperature coefficient of BV suggests the avalanche capability.

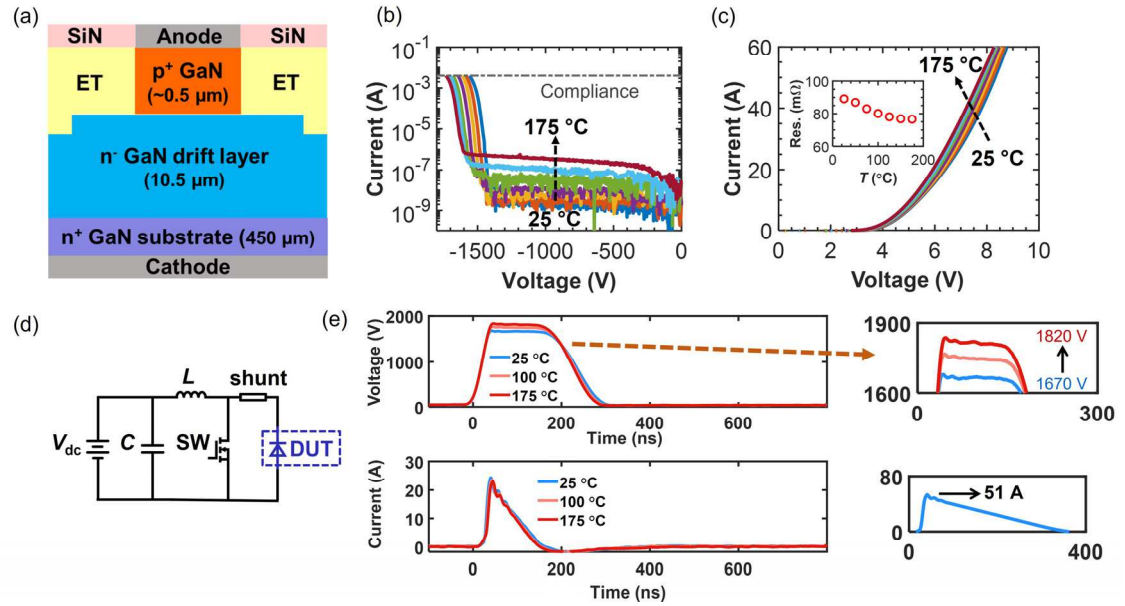

Figure 1. (a) Schematic of vertical GaN p-n diodes and their (b) off-state I_D-V_{DS} characteristics and (c) forward transfer characteristics. The inset of (c) shows the temperature dependence of the differential on-resistance. (d) Diagram of the UIS circuit. (e) The UIS voltage/current waveforms, with a zoom-in view of the voltage waveform and a UIS waveform showing the maximum I_{AVA}.

The avalanche tests were performed in an unclamped inductive switching (UIS) circuit (Fig. 1(d)), which is a widely-used method (and JEDEC standard) to characterize the avalanche capability of power devices (11,18,19). The UIS waveforms show a textbook-like avalanche behaviors, with the device voltage clamped at the avalanche breakdown voltage (BV_{AVA}) and the device current gradually reduced to zero, dissipating the energy through avalanching (Fig. 1(e)). The UIS tests reveal a ~1.7 kV BV_{AVA}, 51 A max avalanche current (I_{AVA}), and 63 mJ avalanche energy (E_{AVA}). These values are among the highest reported in GaN power diodes. The critical E_{AVA} density is determined to be 7.56 J/cm^2, which is similar to SiC rectifiers (18).

An interesting phenomenon that we observed for some diodes is the discrepancy in the BV_{AVA} measured in the quasi-static I-V characteristics (on curve tracer) and in the UIS circuit tests (19). A lower BV_{AVA} was observed in the I-V curves (with low current compliance) as compared to the UIS results and the difference is up to 400 V. A trap mediated avalanche model was proposed to explain it. The BV_{AVA} in I-V curves is believed to be induced by avalanche-assisted trap-filling in the edge termination region, while the BV_{AVA} in the UIS test reflects the robust avalanche at the main p-n junction. The detailed experimental and simulation results are presented in (19). *The key learning is that the UIS circuit test is a more accurate approach to characterize the true* BV_{AVA}

and E_{AVA} of power devices at the major junction, as the large I_{AVA} is expected to fill the available traps at the edge termination immediately after the avalanche starts.

Surge Current Robustness of GaN p-n Diodes

To characterize the surge current robustness of GaN p-n diodes, we have built a customized surge current circuit as detailed in (18,20). A 10-ms-wide half-sinusoidal surge current was generated, according to the JEDEC standard. Fig. 2(a) shows the current/voltage waveforms of the vertical GaN diode in surge current tests with increased peak currents. The DUT failed during the 56-A surge current pulse with a voltage hump at ~6 ms. Fig. 2(b) plots the switching I–V locus of each surge current test. Up to the 53-A surge, the I–V loop remains anticlockwise, due to the decreased R_{ON} at elevated temperatures. The loop becomes clockwise in the 56-A test, indicating a significant R_{ON} rise at the failure transient.

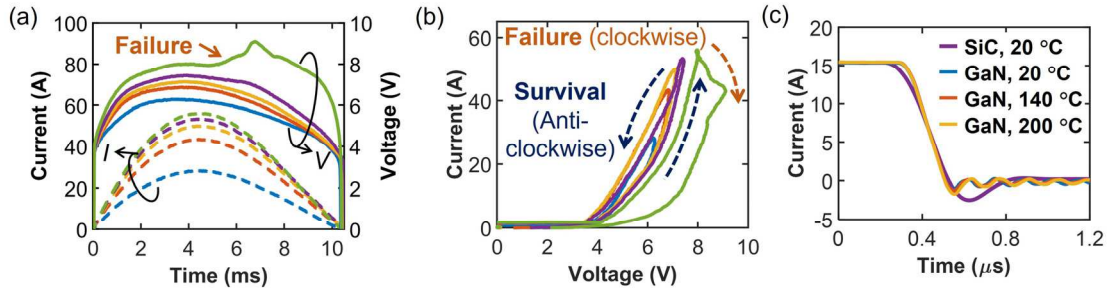

Figure 2. (a) Current/voltage waveforms and (b) switching *I-V* locus of the surge current test of vertical GaN p-n diodes. (c) Reverse recovery waveforms of a vertical GaN p-n diode and vertical SiC p-n diode at various temperatures up to 200 °C.

To explore if the high surge current and avalanche robustness in vertical GaN p-n diodes is due to conductivity modulation, reverse recovery tests were conducted for these diodes at temperatures up to 200 °C. A SiC p-n diode (body diode of a commercial 1.2 kV MOSFET) was tested as a reference. The test results are shown in Fig. 2(c), revealing almost no reverse recovery in vertical GaN p-n diodes. Through detailed analysis, we found that the negative temperature coefficient of differential R_{ON} in vertical GaN p-n diodes is due to the enhanced acceptor ionization instead of hole injection and conductivity modulation (18). This suggest that, unlike SiC and Si p-n diodes, which usually boost the electrothermal ruggedness by introducing bipolar current and trading off the switching characteristics, GaN p-n junctions are not limited by such a trade-off. The GaN p-n diodes show comparable electrothermal ruggedness when compared to SiC p-n diodes, at the same time exhibiting small bipolar conduction and, thus, superior switching characteristics at high temperatures.

Avalanche Robustness of GaN Fin-JFETs

Among various vertical GaN transistors, 1.2-kV fin-channel MOSFETs (Fin-MOSFETs) and Fin-JFETs have shown superior static and switching performance as compared to similarly rated SiC MOSFETs (2,21-24). These performance advancements are attributed to the superior material properties of GaN and the employment of sub-micrometer multi-gate fin channels, which enable high channel density, E-mode

operation, and superior gate control (1,2). Recently, NexGen's vertical GaN Fin-JFETs have demonstrated a specific R_{ON} of 0.82 mΩ·cm^2, a threshold voltage (V_{TH}) of 2 V, a BV_{AVA} over 1700 V, a ~10 ns switching time in 600-V/4-A double-pulse tests, and good thermal stability up to 200 °C (23,24). Fig. 3(a) shows the cell structure of the vertical GaN JFET, which consists of an array of ~1-µm-high n-GaN fin-shaped channels surrounded by the inter-fin p$^+$-GaN gate regions. The p$^+$-GaN regions are commonly connected. Fig. 3(b) shows the device transfer characteristics, revealing an E-mode operation. Fig. 3(c) shows the device off-state I-V characteristics, revealing a non-destructive BV with a positive temperature coefficient, which suggests an avalanche capability. The detailed device characteristics at elevated temperatures up to 200 °C are reported in (24).

To evaluate the avalanche robustness, the GaN JFET was characterized in the UIS test with a standard MOSFET driver (Fig. 3(d)). Fig. 3(e) shows the UIS waveforms, revealing a textbook-like avalanche waveform with V_{DS} clamped at BV_{AVA} and I_{AVA} gradually reduced to zero. The failure UIS test reveals a critical E_{AVA} to be 7.44 J/cm^2, which is comparable to the state-of-the-art E_{AVA} of SiC MOSFETs. *This was the first demonstration of the avalanche capability in a GaN transistor* (23,24).

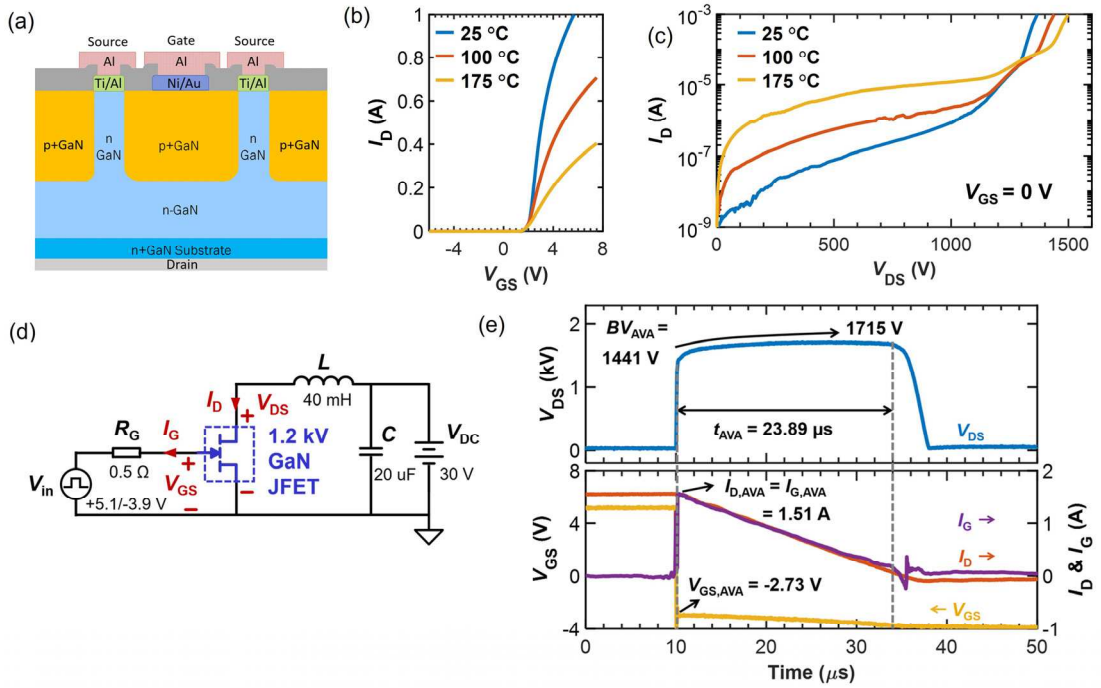

Figure 3. (a) Schematic of vertical GaN Fin-JFETs. (b) Typical transfer characteristics at temperatures up to 200 °C. (c) Off-state I-V characteristics at temperatures up to 200 °C. (d) Circuit diagram of the UIS test circuit with a MOSFET driver. (e) UIS waveform of the 1.2-kV vertical GaN Fin-JFET.

Despite the robust avalanche capability, I_{AVA} flows through the gate in vertical GaN Fin-JFETs. This avalanche path differs from that of power MOSFETS (via the source) and may pose challenges in gate driver reliability. To address this issue, we demonstrated that I_{AVA} in GaN Fin-JFETs can be tuned to flow through the source, by using either a MOSFET driver with a large gate resistance or an *RC*-interface driver (Fig. 4) (25). These

drivers turn on the fin channel during the device avalanche and guide I_{AVA} to flow primarily through the low-resistance fin channel. The carrier dynamics within the GaN JFET under the two avalanche paths have been unveiled by physics-based mixed-mode electrothermal simulations, and the details are presented in (25). The critical E_{AVA} in both paths was found to be comparable with the state-of-the-art SiC MOSFETs. Additionally, the *RC*-interface driver was shown to outperform the MOSFET driver for vertical GaN JFETs, not only for normal switching applications (23) but also for avalanche robustness (25).

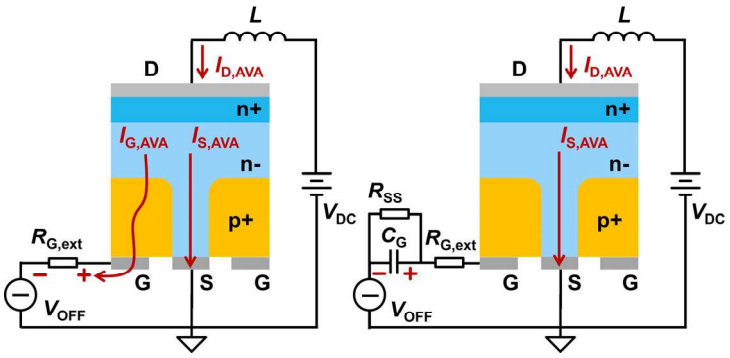

Figure 4. Illustration of the "avalanche-through-gate" (left) and "avalanche-through-fin" (right) processes in vertical GaN Fin-JFETs when a standard MOSFET driver and a *RC*-interface driver is employed, respectively.

Short-Circuit Robustness of GaN Fin-JFETs

The Fin-JFETs characterized in the short-circuit test has a rated voltage of 600-700 V with a specific R_{ON} of 0.7 mΩ·cm^2 and a BV_{AVA} of 800 V. A customized short-circuit test platform has been built with several key designs (Fig. 5(a)) (26): a) a bus voltage of 400 V up to 800 V (device BV_{AVA}); here 400 V represents the usual bus voltage for 600-700 V devices; b) a high slew rate (di/dt) enabled by the low stray inductance, which mimics the shoot through in power electronics systems; c) an *RC*-interface gate driving circuit, which is identical to that used for the device's switching operations (23).

GaN Fin JFETs were tested to failure at different bus voltages, and a short-circuit withstand time (t_{SC}) of 30.5 µs was measured at 400 V (Fig. 5(b)), 17.0 µs at 600 V, and 11.6 µs at 800 V (i.e., the BV_{AVA} at 25 °C) (Fig. 5(c)) (26). *These t_{SC} are the longest reported in all 600-700 V rated normally-off unipolar power transistors.* Upon failure, V_{DS} shows no change; I_D and V_{GS} drop to zero; and I_G increase. These behaviors imply a drain-to-source open and gate-to-source partial shorting. This signature was confirmed by static characterizations of the failed DUT (Fig. 5(d)), in which BV_{AVA} was retained. This failure-to-open-circuit signature is highly desirable for system applications, as the failed device still blocks voltage, retaining system functionality in the case of parallel devices or multichip modules. In addition to single pulse test, repetitive 10 µs, 400 V short-circuit tests were also performed for GaN Fin-JFETs, which showed no degradation after 30,000 cycles (26). The GaN Fin-JFETs were also found to be able to survive thousands of pulses in repetitive short-circuit tests at 10 µs, 600 V, a voltage close to its voltage rating (27). Repetitive short-circuit tests at such a high bus voltage have not been reported in prior literature for any other power device.

As far as we know, this is the first report of the short-circuit capability of a power transistor at a bus voltage close to its BV_{AVA}. To understand this unique feature of GaN Fin-JFETs, we performed TCAD simulations in Silvaco, and the detailed simulation results are presented in (26). The simulation unveils the enabling device physics to be the 'avalanche-through-fin' process. In the simulated short-circuit transient at 800 V (t = 11 µs), the impact ionization generation rate was found to peak at the foot of the fin channel (Fig. 5(e)). The holes generated in the impact ionization are removed via the p-GaN gate, and these holes also facilitate electrons to be pumped from the source to recombine with them (Fig. 5(f)). This "avalanche-through-fin" process accommodates a large I_D flowing through the fin channel into the drift region and thereby a good short-circuit capability at BV_{AVA}. Other key device physics that enables exceptional short-circuit capabilities in vertical GaN Fin-JFETs, such as the saturation current self-limitation and gate-driver interplays, are detailed in (26,27).

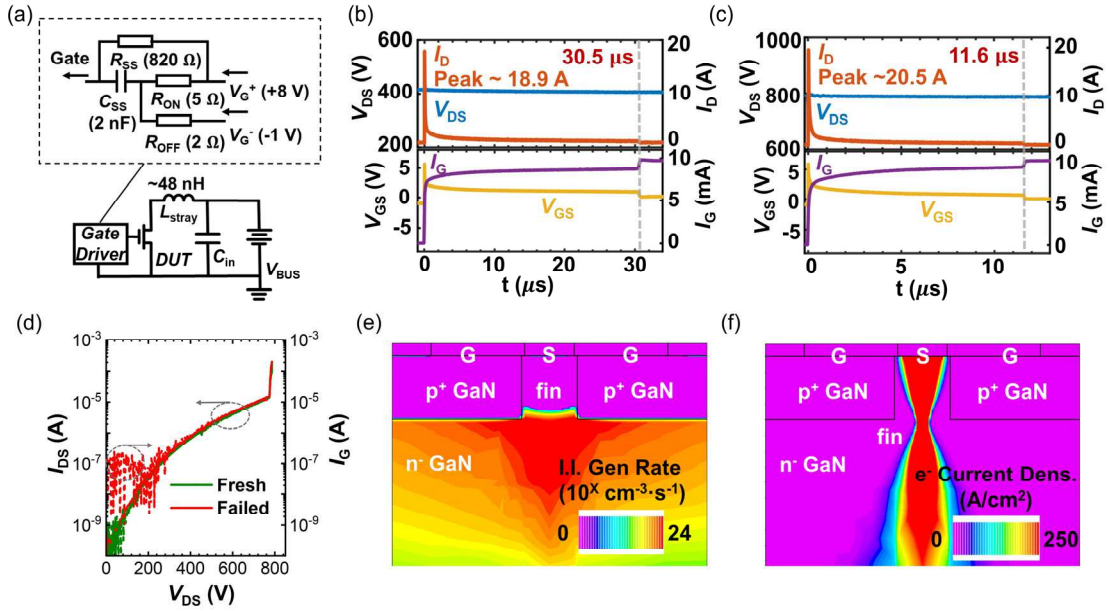

Figure 5. (a) Circuit diagram of the short-circuit test setup. Failure short-circuits waveforms at a bus voltage of (b) 400 V and (c) 800 V. (d) Off-state I_{DS}-V_{DS} characteristics of the failed device and a fresh device. Simulated contours of (e) impact ionization generation rate and (f) electron current density under the short-circuit condition at a bus voltage close to BV_{AVA}.

Failure-to-open-circuit Signature

The above discussions suggest that vertical GaN Fin-JFETs are inherently robust under the concurrence of avalanche and short-circuit stresses. In addition to under the short-circuit stress, the vertical GaN Fin-JFET was also found to exhibit a failure-to-open-circuit (FTO) signature under the through-fin avalanche (29). This FTO signature is desirable for system applications, at the same time, very interesting from the device physics standpoint, as in prior literature all Si and SiC power transistors were reported to show a failure-to-short-circuit (FTS) signature under the avalanche condition (29) with most of them showing a FTS signature under the short circuit condition (28).

The detailed works on understanding the unique FTO signature of vertical GaN Fin-JFETs under the through-fin avalanche and short-circuit conditions are presented in (29) and (28), respectively. Here we use the through-fin avalanche condition as an exemplar case to briefly introduce the key enabling device physics. In a power device, I_{AVA} usually flows across the major blocking p-n junction, i.e., the peak electric field location at BV_{AVA}. As a result, when high I_{AVA} induces a thermal failure, the blocking junction is usually damaged, yielding an FTS signature.

In the through-fin avalanche of vertical GaN Fin-JFETs (Fig. 6), while the peak electric field is still at the gate-drain p-n junction, the peak impact ionization location moves to the foot of the n-GaN fin. Electrons are pumped from the source, travel through the fin channel, and recombine with the holes generated in impact ionization. As a result, the high I_{AVA} stress congregates in the fin, and only a small hole current density is present at the junction around the fin corner. As this I_{AVA} stress is away from the gate-drain junction, and the narrow fin prevents the punch-through (30), BV_{AVA} retains in the failed DUT, enabling a FTO signature.

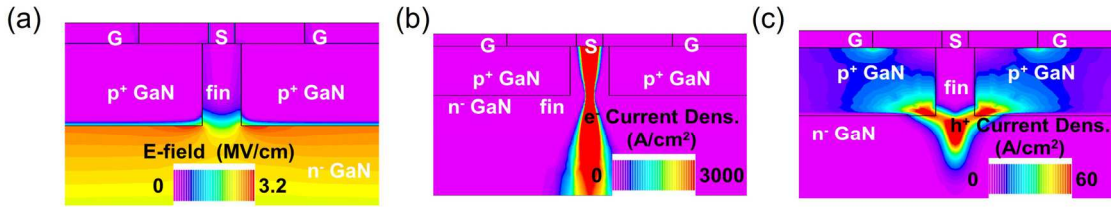

Figure 6. Simulated contours of (a) electric field, (b) electron current density, and (c) hole current density under the through-fin avalanche condition.

Conclusion

In recently three years, through collaborations with NexGen, we have demonstrated breakthrough avalanche, surge-current and short-circuit robustness in vertical GaN p-n diodes and Fin-JFETs manufactured by NexGen in 100 mm GaN-on-GaN fab. The demonstrated avalanche, surge-current and short-circuit capabilities are comparable to or even superior to Si and SiC power devices. Additionally, vertical GaN Fin-JFETs show FTO signatures under avalanche and short-circuit conditions, which is highly desirable for the system safety. These results reshape people's perspectives on GaN device robustness and reliability, show great potential of vertical GaN power devices for numerous power electronics applications, and provide new insights into the power device design for robustness that would be also beneficial to other power devices based on various semiconductor materials.

Acknowledgement

The authors acknowledge the close collaboration with NexGen Power Systems Inc. as well as the collaboration with Silvaco for device simulations. The work at Virginia Tech is partially supported by the National Science Foundation under Grant EECS-2045001 and the Center for Power Electronics Systems Power Management Consortium.

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