Exceptional Repetitive-Short-Circuit Robustness of Vertical GaN Fin-JFET at High Voltage

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***Abstract*—The concern on the insufficient short circuit (SC) capability of GaN high-electron-mobility transistors (HEMTs) blocks the adoption of commercial GaN devices in many applications. Recently, superior SC robustness was demonstrated in a vertical GaN Fin-JFET with a short circuit withstanding time over 30 µs at 400 V bus voltage (V_{BUS}), showing great potential for motor drives and EV powertrain applications. This work presents the first study on the repetitive SC robustness of 650-V rated vertical GaN Fin-JFETs at a V_{BUS} of 400 V and 600 V. The GaN Fin-JFET survived 30,000 cycles of 400 V, 10 µs SC stresses without any degradation in device performance. At a 600 V V_{BUS}, it survived over 8,000 cycles of 10 µs SC stresses before an open failure with the avalanche breakdown voltage retained. This failure-to-open-circuit feature is highly desirable for system safety considerations. Besides, an increase in gate leakage was observed along the 600 V test, which can be used as a screening factor to anticipate the failure in applications. This is the first report of exceptional repetitive SC robustness at a V_{BUS} up to 600 V in a 600-700 V rated power device.**

Keywords—gallium nitride, FinFET, JFET, short circuit, repetitive test, degradation, failure analysis

I. Introduction

The unique device properties of Gallium nitride (GaN) high-electron mobility transistors (HEMTs) making them great choices in power applications. Equipped with high breakdown voltage from the high critical electric field of GaN, small specific on resistance ($R_{ON,sp}$) from the high carrier mobility in two-dimensional electron gas (2-DEG) channel and small device gate charge (Q_G), GaN HEMTs are commercialized to 900 V with smaller device capacitance and on resistance compared to similar rated Si & SiC MOSFET, enabling high frequency switching in megahertz. Therefore, adopting GaN HEMTs in power systems fits the miniaturization requirement, which potentially increases the power density and the system efficiency as well.

However, a major concern blocking GaN's penetration in many applications is the short-circuit (SC) robustness, a key requirement for power devices in applications such as electric vehicle powertrains and power grids. The typically required short circuit withstanding time (t_{SC}) is 10 µs for the protect circuit to intervene and clear the fault. The current commercial GaN HEMT has limited SC robustness. The reported t_{SC} of all mainstream commercial 600/650-V GaN HEMTs is below 1 µs at the 400 V bus voltage (V_{BUS}) [1-3], and they catastrophically fail in only a few SC cycles [4]. A 3 µs t_{SC} was reported in R&D GaN HEMTs, however, it is still far below the 10 µs system requirement, while device on resistance (R_{ON}) saturation current ($I_{D,sat}$) and switching speed were sacrificed [5]. Further studies found the SC failure in GaN HEMT is related to the propagation of high electric field [6, 7], this non-thermal failure suggests the insufficient SC robustness could be an intrinsic issue originated from the lateral GaN HEMT structure.

Recently, we demonstrated exceptional SC robustness in a 650-V vertical GaN fin-channel junction field effect transistor (Fin-JFET), which showed a single-event t_{SC} of over 30 µs at 400 V as well as a failure-to-open-circuit (FTO) signature [8]. These results clear the SC roadblock for GaN-based transistors. Beyond single-event test, repetitive SC robustness is also important for system applications. In this work, we extend our previous study to repetitive SC robustness for the 650-V class vertical GaN Fin-JFET. It was found that the device under test (DUT) survived 30,000 cycles of 400 V, 10 µs SC pulses without degradation in performance. At 600 V V_{BUS}, DUTs survived over 8,000 cycles of 10 µs repetitive SC pulses before an FTO. After the initial failure, DUTs could still withstand multiple SC cycles without further damage. Finally, a gradual increase in gate leakage current (I_G) was observed in repetitive test, which can be used as a key screening factor of device degradation and maintain system reliability.

II. Single-event Short Circuit Test

A. Device under test and test setup

Fig. 1 shows the cross-section schematic of the 650-V rated normally-off GaN Fin-JFET designed and fabricated by NexGen Power Systems. The DUT features a array of ~ 1 µm deep n-GaN fin-channel with p^+-GaN gate-all-around structure. The working principles and gate driving strategies are similar to the ones reported in [8-10]. The active area is 0.1 mm^2 and the DUTs are assembled in either TO-247-4 packages or surface mounted DFN 56 packages. Different packages show no influence on SC test results.

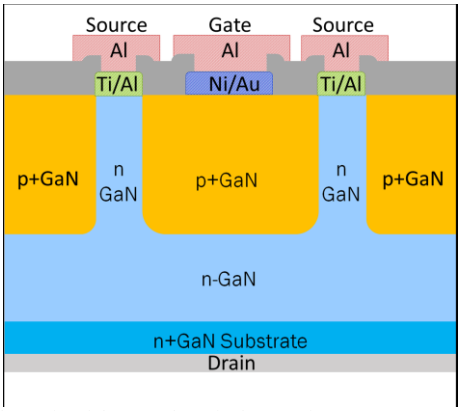

Fig. 1. Schematic of the tested vertical GaN Fin-JFET (not to scale).

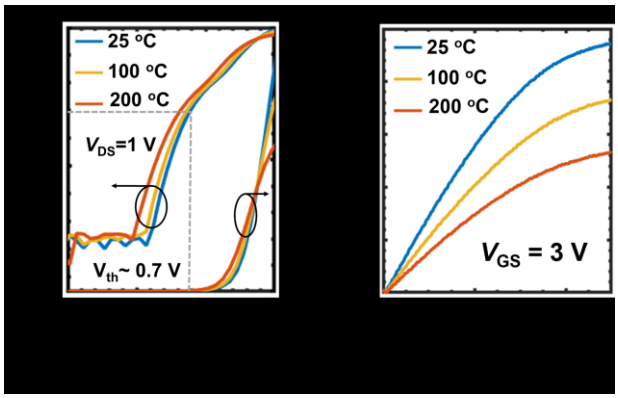

Fig. 2. (a) Transfer and (b) output characteristics of the DUT. The V_{th} is 0.7 V and the R_{ON} is 0.7 Ω.

Fig. 2 shows the transfer and output characteristics of the DUT at 25 ºC, 100 ºC and 200 ºC, respectively. DUT shows a normally off operation with an 0.7 V extracted threshold voltage (V_{th}) at a drain current (I_D) of 1 mA at 25 ºC. R_{ON} is 0.7 Ω ($R_{ON,sp}$ of 0.7 mΩ • cm^2) in the linear region at gate-to-source voltage (V_{GS}) of 3 V at 25 ºC. $I_{D,sat}$ is ~ 4.8 A at 25 ºC.

Fig. 3(a) shows the SC test circuit. To best mimic the SC shoot through, no external inductor was connected in the circuit while the stray inductance from PCB layout was measured to be 48 nH. An RC interface gate driving circuit was implemented (Fig. 3(b)), which is the same as the one used in GaN FinJFET switching applications [9]. In the tun-on transient, both DUT gate capacitance (C_G) and C_{SS} are charged through the 5 Ω R_{G-ON} until the gate pn junction conducts current (~ 3.5 V V_{GS}). The excessive voltage is then sustained

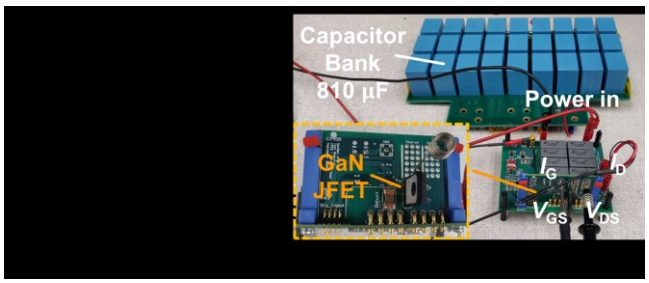

Fig. 3. (a) Schematic of the SC test circuit. (b) Schematic of the RC interface gate driving circuit with all component values marked. (c) Photo of the test setup.

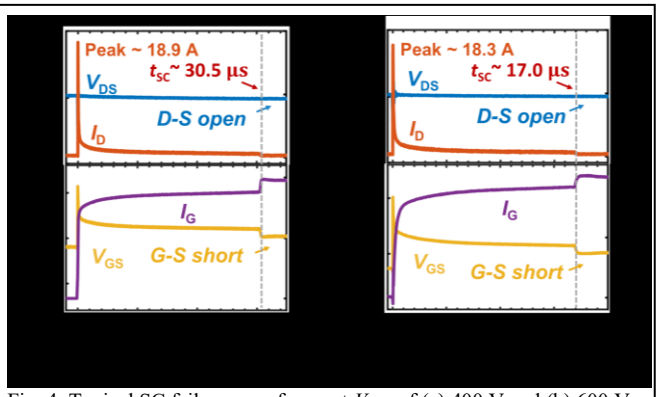

Fig. 4. Typical SC failure waveforms at V_{BUS} of (a) 400 V and (b) 600 V. DUTs failed drain-to-source open in both tests.

by C_{SS}. In turn-off transient, the charge stored in C_{SS} quicky compensates with Q_G, providing a negative voltage spike for fast turn-off [11]. All these designs in the test enables fast switching and high current slew rate (di/dt).

B. *Single-event SC test results*

Fig. 4 shows the typical failure waveforms at 400 V & 600 V V_{BUS}. In both tests, V_{DS} stayed at V_{BUS} after failure occurred, V_{GS} dropped to 0 and I_G rose, indicating a gate-to-source (G-S) short and drain-to-source (D-S) open failure nature. The recorded t_{SC} is 30.5 µs at 400 V and 17.0 µs at 600 V. This FTO signature was then confirmed by the curve tracer characterization shown in Fig. 5. Failed DUT retained avalanche capability after the failure, with a slight increase in I_G.

Comparing to the SC robustness reports of similar voltage rated Si & SiC power MOSFETs in [2, 8, 12], where the t_{SC} is usually under 10 µs at 400 V. GaN Fin-JFET exhibits the longest t_{SC} which results from the inherent advantages of the Fin-JFET structure. From the discussion in [14], Fin-JFET structure can effectively reduce the thermal stress in SC event, manifested as a fast decrease of $I_{D,sat}$ shown in Fig. 4. Besides, the peak electro-thermal stress is tuned away from the main blocking pn junction, which results in the favorable FTO signature in single-event SC test.

III. Repetitive Short Circuit Test

Repetitive short circuit test was first performed at 400 V and V_{BUS} was then increased to 600 V to further explore DUT's robustness. In both tests, the SC duration was set to 10 µs each pulse and period was 3 s. Test setup was the same as described

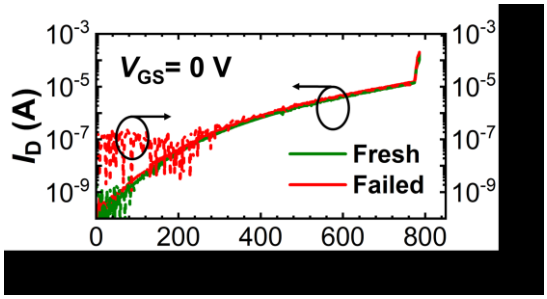

Fig. 5. Off-state I-V characterization of the fresh and failed DUT.

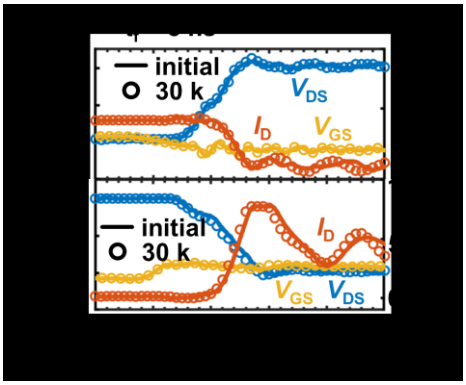

Fig. 6. Turn-off and turn-on switching waveforms before and after 30,000 cycles of 400 V, 10 µs short circuit stress.

in Fig. 3.

In 400 V test, no failure was found after 30,000 cycles of SC stress. Before and after the test, DUT was put in a 400 V, 4 A double pulse test (DPT). Fig. 6 shows the turn-on and turn-off waveforms of fresh & tested DUT in the DPT, and they overlap with each other, indicating the DUT performance showed no degradation.

In 600 V repetitive test, DUT survived over 8,000 SC cycles. The failure initiated in cycle #8786. Shown in Fig. 7, V_{GS} rises from negative value to zero, implying a G-S partial short while D-S remained open. The final failure state was reached and maintained in cycle #9785, in this stage, DUT can still withstand short-circuit stress with a lower I_D: after the DUT is pulsed on, V_{GS} quickly dropped to 0 due to the partial shorted G-S terminals. As a result, the thermal stress in the short circuit test is reduced and the DUT would not suffer from further damage. This non-destructive and "progressive" failure can be understood from the output characteristics shown in Fig. 8: the gate functionality retained in failed DUT, while comparing the stage of before (cycle #8785) and after (cycle #8786) the initial failure and after the final failure (cycle #9785), consistent decrease in I_D was observed, validating the failure is a gradual accumulation in the number

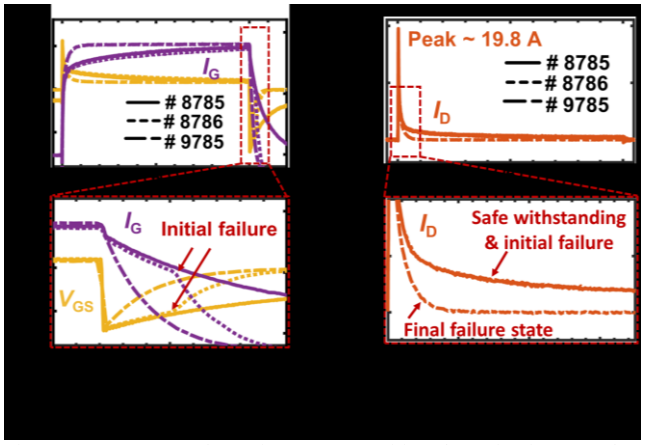

Fig. 7. V_{GS} & I_G waveforms in 600 V repetitive short-circuit tests. The failure initiates in cycle # 8786. (b) I_D waveforms in 600 V repetitive short-circuit tests, I_D quickly reduces to 0 in the final failure state due to the partial shorted G-S junction.

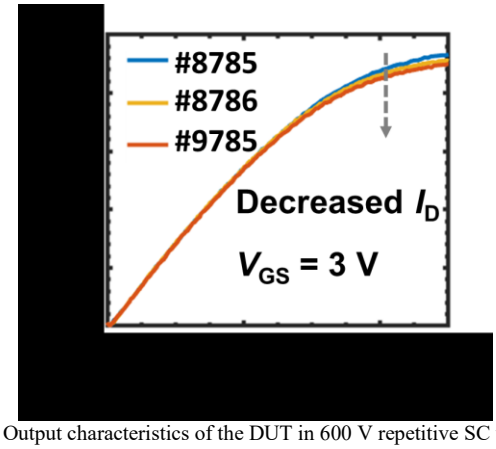

Fig. 8. Output characteristics of the DUT in 600 V repetitive SC tests.

of failed fins.

To understand the degradation/failure mechanisms. DUTs were characterized periodically to track any possible parameter shift in another 600 V repetitive test. Fig. 9(a) shows the I_G drift in off-state I-V characteristics. A gradual increase in the gate leakage current is observed as the repetitive SC test prolongs. Meanwhile, the I_D drift (Fig. 9(b)) was found to be much smaller than I_G. Therefore, I_G current path is located between gat and source, the lateral pn junction was deteriorated in the repetitive short-circuit test at 600 V, which eventually caused the device failure.

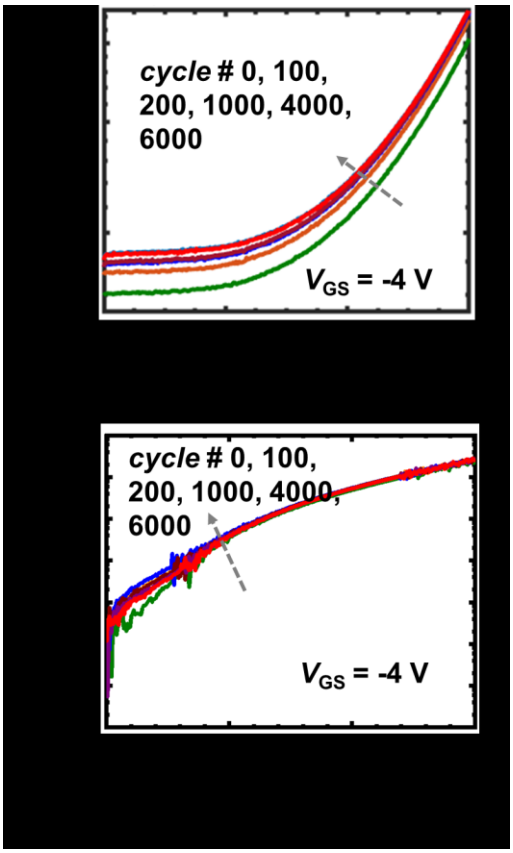

Fig. 9. Drift in (a) gate leakage and (b) drain leakage in 600 V repetitive short circuit test.

IV. Conclusions

This work presents the first comprehensive study on repetitive short circuit robustness of vertical GaN Fin-JFET. 650-V class GaN Fin-JFETs withstand 30,000 cycles of 400 V 10 μs short circuit stress without suffering from any degradation in performance. In higher voltage test at 600 V, GaN Fin-JFETs survived over 8,000 cycles. Degradation was identified between lateral gate-to-source junction, which leads to a G-S short and D-S open failure signature. This non-destructive failure is highly desired in applications as it protects the whole system from catastrophic failure in abnormal events. We show great advantages of implementing vertical GaN Fin-JFETs in future applications for a more robust power system, especially in which power devices are likely exposed to harsh conditions, such as EV powertrain and power grids.

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