

# Activating thick buried p-GaN for device applications

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**Abstract**— Many emerging GaN electronic and optoelectronic devices comprise p-GaN layers buried below n-GaN or AlGaN. The activation of these buried p-GaN layers usually relies on the lateral hydrogen diffusion through the etched mesa sidewalls, which is known to induce non-uniform acceptor distributions. However, the acceptor profile, electric field (E-field) blocking capability, and leakage current mechanisms of the sidewall activated p-GaN layer have not been fully understood. This work addresses these knowledge gaps by fabricating vertical GaN p-n diodes with a thick (3.8  $\mu\text{m}$ ) p-GaN. Two activation schemes were performed to allow the hydrogen diffusion through sidewalls and the top surface, respectively. For the sidewall activation, an analytical model was developed to depict the spatial distribution of the activated acceptor and the temporal evolution of this distribution with the increased annealing time. This model was validated using the C-V characteristics of the fabricated diodes with various radii. Under reverse biases, the breakdown E-field and leakage current of the sidewall-activated diodes were found to be determined only by the edge area with the highest activation efficiency. The leakage mechanism agrees with the trap-assisted tunneling model, and the peak junction E-field can exceed 3 MV/cm, both being similar to those of surface-activated diodes. These results provide critical information for the design and processing of advanced GaN devices with the buried p-GaN.

**Index Terms**— Gallium nitride, p-n diode, power electronics, p-GaN, activation, leakage current, breakdown voltage, MOCVD

## I. INTRODUCTION

P-type GaN has become a critical building block in many GaN devices [1], [2], e.g., diodes [3]–[6], high electron mobility transistors (HEMTs) [7]–[11], current-aperture vertical electron transistors (CAVETs) [12], MOSFETs [13], [14], and JFETs [15], [16]. These GaN devices use p-n junctions for electrostatic control [11]–[13], electric field (E-field) management [3]–[7], [12]–[15], and conductivity modulation [16], [17]. While p-GaN is often the topmost layer, it is buried below n-type GaN in many devices, e.g., CAVETs, trench MOSFETs, and tunnel-junction light emitting diodes [18]–[21]. Meanwhile, emerging devices like superjunction transistors [22]–[24] and reduced-surface-field (RESURF) HEMTs [25] require thick p-GaN layers (at least several micron-meters) below n-GaN or AlGaN.

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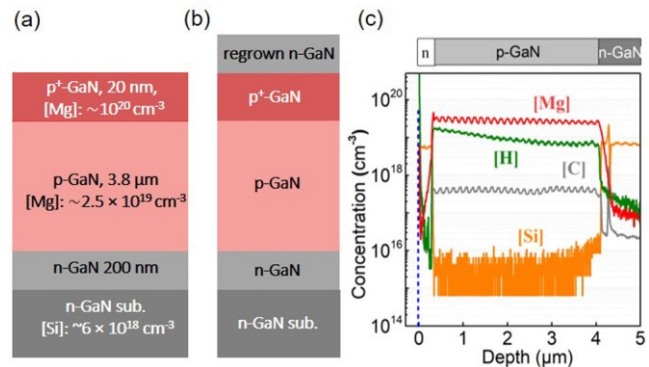


Fig. 1. Schematic of the (a) as-grown epitaxial structure and (b) the structure with a regrown n-GaN layer. (c) SIMS data of [Mg], [H], [Si] and [C] concentrations in the n-p-n structure after the n-GaN regrowth.

P-GaN is usually epitaxially grown by metal organic chemical vapor deposition (MOCVD) using the acceptor magnesium (Mg). However, the hydrogen (H) in MOCVD forms Mg-H complexes and passivates [Mg] acceptors [26]. A post-growth annealing is routinely used to activate p-GaN, which breaks Mg-H bonds, allowing the [H] to diffuse to the ambient through the top p-GaN surface. However, this through-surface activation is not viable for buried p-GaN due to a very high [H] diffusion barrier in n-GaN [26]. Even after p-GaN is activated, any further MOCVD epitaxy will re-passivate it [27]. As a solution, molecular beam epitaxy was used for regrowing the top layers after p-GaN activation [19]. However, the sample transfer between multiple chambers has been widely reported to introduce impurities [28]–[30].

A more popular solution for the buried p-GaN activation is the lateral [H] diffusion through the etched mesa sidewalls [10], [17], [23], [27], [28]. Li *et al.* found that the full activation can only be achieved in a small device area with a dimension of 10–20  $\mu\text{m}$  [27]. This suggests that the buried p-GaN in large-area devices is likely to be partially activated. Recently, Narita *et al.* studied the [H] diffusion dynamics in larger-area buried p-GaN [31]. However, vast knowledge gaps persist on the acceptor profile, E-field blocking capability, and leakage current mechanisms of this partially-activated, non-uniform p-GaN. Addressing these gaps is critical to any GaN device comprising the buried p-GaN, particularly for power electronic devices.

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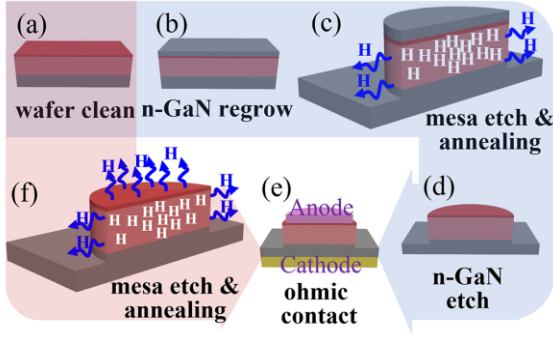


Fig. 2. Major fabrication steps of GaN diodes (a)-(e) with sidewall activation (blue background arrow) and (f) with surface and sidewall activations (red background arrow).

This work probes the dopant profile and electrical characteristics of a sidewall-activated buried p-GaN layer, by characterizing vertical GaN p-n diodes comprising it. Different from prior works [27], [31], [32], a thick p-GaN is employed to avoid its punch-through and allow the study of its leakage mechanisms. Thick buried p-GaN is also essential for future superjunction and RESURF devices. The surface potential mapping by the Kelvin probe force microscopy (KPFM) was used to confirm the partial activation. A model for the activation profile was established and calibrated by C-V characteristics of the fabricated diodes with various radii. The reverse breakdown and leakage mechanisms of the diodes with non-, sidewall-, and surface- (i.e., fully) activated p-GaN layers are also unveiled.

## II. FABRICATION PROCESS

The epitaxial structure consists of a 20 nm  $p^+$ -GaN layer ([Mg]:  $1 \times 10^{20} \text{ cm}^{-3}$ ), a 3.8  $\mu\text{m}$  p-GaN layer ([Mg]:  $\sim 2.5 \times 10^{19} \text{ cm}^{-3}$ ) and a 200 nm n-GaN layer ([Si]:  $7.5 \times 10^{18} \text{ cm}^{-3}$ ) grown on GaN substrates by MOCVD [Fig. 1(a)]. On top of some samples, a 300 nm n-GaN layer ([Si]:  $5 \times 10^{18} \text{ cm}^{-3}$ ) was regrown in MOCVD, which prevents the [H] diffusion through top surfaces [Fig. 1(b)]. Fig. 1(c) shows the concentrations of [Mg], [H], [Si] and [C] in a sample with the regrown n-GaN cap measured by secondary-ion mass spectrometry (SIMS). A high [H] concentration of  $\sim 10^{19} \text{ cm}^{-3}$  is exhibited in the p-GaN layer after the n-GaN regrowth.

Fig. 2 shows the major fabrication steps of vertical GaN p-n diodes. After the wafer cleaning (Fig. 2(a)) and n-GaN regrowth (Fig. 2(b)), a 5  $\mu\text{m}$  deep mesa etch was performed using a Cr/Ni hard mask and  $\text{Cl}_2$  gas, in which 10 nm Cr is used to enhance the adhesion and reduce the stress, followed by a rinse in 5% TMAH to remove the etch damages [33]. The activation annealing was at 800  $^\circ\text{C}$  in  $\text{N}_2$  for 0.5-1 hours (Fig. 2(c)). Then the n-GaN cap layer was etched (Fig. 2(d)), followed by the formation of the anode by Pd/Ni/Au with a 600  $^\circ\text{C}$  annealing in  $\text{N}_2$  for 5 minutes. The cathode was formed by Ti/Al/Ni/Au (Fig. 2(e)). A control diode was fabricated without n-GaN caps during the p-GaN activation, allowing the via-surface [H] release and thus a full activation (Fig. 2(f)). Another control diode without p-GaN activation was also fabricated. The radii of all three types of diodes range from 5  $\mu\text{m}$  to 100  $\mu\text{m}$ .

## III. MATERIAL AND DEVICE CHARACTERIZATIONS

The activated acceptor ( $N_A$ ) profile in the sidewall-activated p-GaN was first probed by KPFM, which enables nanometer-

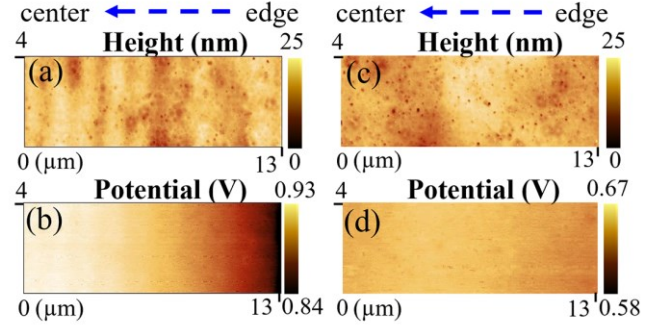


Fig. 3. (a) Surface morphology and (b) potential on a sidewall-activated p-GaN. (c) Surface morphology and (d) potential on a fully-activated (i.e., surface-activated) p-GaN.

scale mapping of surface potentials [34] and has been recently employed to map the dopant profiles in GaN p-n junctions [35], [36]. The KPFM measurement was performed in a Bruker DIMENSION system with a SCM-PIT-V2 tip. The n-GaN substrate was grounded. The cantilever measured the surface topography in the first scan and followed the stored surface topography at a certain lift height (100 nm) during the second interleave scan to record the electrostatic force that reflects the surface potential under an ac bias applied to the tip. The ac bias frequency was set to be the tip resonant frequency, and a DC bias was applied on the feedback loop to compensate the work function difference between the tip and the sample surface. Before the KPFM characterization, the  $p^+$ -GaN cap layer and Ohmic metal were etched, followed by a long TMAH treatment to reduce the etch damage [30].

Fig. 3(a) and (b) show the p-GaN surface morphology and potential, respectively, after the sidewall activation for 0.5 hours. The surface potential increases from the diode edge towards the center without correlations to morphology features, suggesting a non-uniform  $N_A$  distribution that decreases from the edge towards the center. Note that, due to the impact of surface states and surface band bending,  $N_A$  gradients can only be qualitatively reflected but difficult to be quantitatively derived from the surface potential profile [35]. Fig. 3(c) and (d) show the surface morphology and potential of a fully activated p-GaN (i.e., by surface activation), revealing a nearly uniform surface potential with a magnitude lower than that shown in Fig. 3(b). This suggests a uniform and higher  $N_A$  in the fully activated p-GaN as compared to the sidewall-activated one.

Fig. 4(a) shows the I-V characteristics of the sidewall activated diodes with a radius ( $R$ ) of 5  $\mu\text{m}$  and 50  $\mu\text{m}$  as well as the fully (surface) activated diode with a  $R$  of 5  $\mu\text{m}$ . All three diodes show good rectifying behaviors. The forward current of the two diodes with  $R = 5 \mu\text{m}$  are similar, while that of the sidewall-activated diodes with  $R = 50 \mu\text{m}$  is much lower. This suggests a strong radius dependence on the average activation ratio in the sidewall-activated diodes. The slightly higher turn-on voltage in the sidewall activated diode is due to the inferior Ohmic contact formed on the etched p-GaN surface.

Fig. 4(b)-(e) show the I-V characteristics of the fully (surface)- and sidewall-activated diodes with  $R$  of 5-50  $\mu\text{m}$ . As the leakage current along the etched sidewall is a concern in some GaN devices [37], [38], the fully-activated diodes are examined first. The current densities of fully-activated diodes are proportional to the area instead of perimeter, validating that

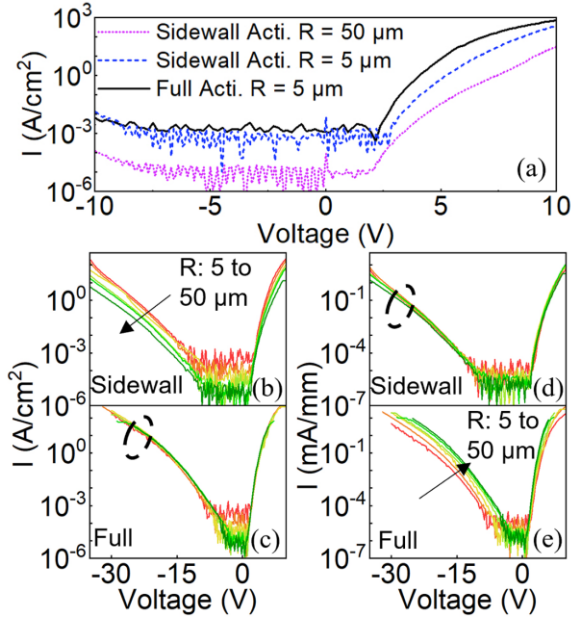


Fig. 4. (a) I-V characteristics of fully- and sidewall-activated diodes with a radius of 5 and 50  $\mu\text{m}$ . The lower noise current density for  $R = 50 \mu\text{m}$  diode is due to the same noise floor of the curve tracer normalized to a larger area. I-V characteristics of the (b) sidewall and (c) fully activated diodes with radii from 5 to 50  $\mu\text{m}$ , normalized to the anode area. The same I-V curves for (d) sidewall and (e) fully activated diodes normalized to the perimeter.

the leakage current is dominated by the bulk junction, and that along the etched sidewall is minimal. By contrast, the current densities of the sidewall-activated diodes normalized to the area show a large discrepancy, while those normalized to the perimeter overlap. These results further confirm the non-uniform  $N_A$  with a high activation efficiency near the sidewall.

#### IV. ACCEPTOR MODEL AND CALIBRATION

In this section, we establish a [H] diffusion model in the buried p-GaN to quantify the spatial and temporal profile of the activation ratio ( $\eta$ ), i.e., the ratio between the activated acceptor  $N_A$  and the total ionizable acceptor concentration ( $N_A^0$ ). Here  $N_A^0$  was extracted to be  $1 \times 10^{19} \text{ cm}^{-3}$  from the C-V data of the fully-activated diodes. Note that,  $N_A^0 < [\text{Mg}]$  is commonly observed in p-GaN with  $[\text{Mg}] > 10^{19} \text{ cm}^{-3}$ . This is because there are two types of Mg-H complexes: the metastable one leading to the Mg acceptor after annealing (i.e., corresponding to  $N_A^0$ ), the other one being stable and electrically inactive [39].

In circular diodes, the [H] concentration can be depicted by a generic diffusion equation in the cylindrical coordinate [26]:

$$D \frac{1}{r} \frac{\partial}{\partial r} \left( r \frac{\partial [H]}{\partial r} \right) = \frac{\partial [H]}{\partial t} \quad (1)$$

where  $r$  is the radial distance,  $t$  is the annealing time, and  $D$  is the [H] diffusion coefficient. The diffusion along the axial direction can be ignored due to a much lower  $D$  for [H] in n-GaN as compared to that in p-GaN [31]. A boundary condition in the center that describes the zero [H] concentration gradient and the other one depicting the sidewall diffusion barrier as well as the initial [H] concentration can be written as [26]:

$$\frac{\partial [H]}{\partial r} \Big|_{r=0,t} = 0 \quad (2)$$

$$\frac{d}{dt} \left( \frac{[H]_{r=R,t=0}}{[H]_{r=R,t}} \right) = A \quad (3)$$

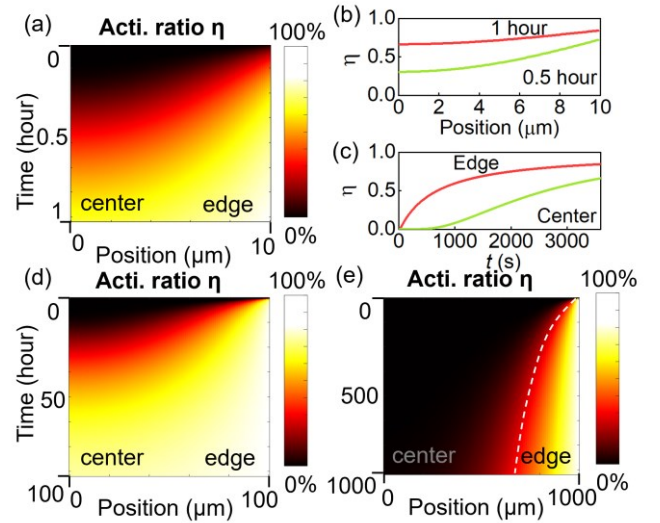


Fig. 5. (a) Spatial-temporal contour of  $\eta$  for a sidewall-activated p-GaN with  $R = 10 \mu\text{m}$ . (b) Extracted  $\eta$  profile along a radius direction after 0.5- and 1-hour activation. (c) Temporal evolution of  $\eta$  at the device edge and center. Spatial-temporal contour of  $\eta$  for (d)  $R = 0.1 \text{ mm}$  p-GaN up to 100 hours of activation and (e)  $R = 1 \text{ mm}$  p-GaN up to 1000 hours of activation.

$$[H]_{r,t=0} \approx N_A^0 = 1 \times 10^{19} \text{ cm}^{-3} \quad (4)$$

where  $A$  is a constant related to the sidewall surface barrier for [H] desorption. The model calibration (will be detailed soon) produces a  $D$  of  $1.4 \times 10^{-10} \text{ cm}^2 \text{ s}^{-1}$  and an  $A$  of  $1.5 \times 10^{-3} \text{ s}^{-1}$  for our samples. In (4), we assume that almost all  $N_A^0$  is initially passivated by [H]. This assumption was validated by the C-V measurements of a non-activated diode, in which an acceptor concentration of  $1 \sim 2 \times 10^{17} \text{ cm}^{-3}$  was extracted. This suggests an initial  $\eta$  of only 1~2%. The SIMS profile in Fig. 1 also reveals an average [H] concentration of  $\sim 1 \times 10^{19} \text{ cm}^{-3}$ , which is similar to  $N_A^0$ , further supporting (4).

Fig. 5(a) shows the modeled  $\eta$  as a function of  $r$  and  $t$  in a sidewall-activated p-GaN with  $R$  of 10  $\mu\text{m}$ . Fig. 5(b) shows two cutlines of the  $\eta$  spatial distribution after 0.5 and 1 hours annealing. After 1 hour annealing,  $\eta$  is close to 84% near the edge and  $\sim 66\%$  in the center. Fig. 5(c) shows two cutlines of the  $\eta$  temporal evolution at the edge and center. The activation first occurs at the edge and saturates early there; the activation in the center shows an initial delay and ramps up later.

Fig. 5(d) and (e) show the modeled spatial-temporal distribution of  $\eta$  for two larger p-GaN regions with a  $R$  of 0.1 and 1 mm. A 100-hour annealing is predicted to fully activate the former p-GaN, while a 1000-hour annealing is still insufficient for the latter p-GaN. As shown in Fig. 5(e), for a large  $R$ , the contour of the activation boundary in the cylindrical coordinate roughly follows a  $t \propto d^2$  relation, where  $d$  is the radial distance to the sidewall. This suggests a fast increase in  $t$  that is required to fully activate a larger p-GaN area.

To calibrate our model, C-V characteristic were measured for the sidewall-activated diodes with various radii after 1 hour activation, which were then compared with the modeled C-V curve using the profile of the ionized acceptor concentration ( $N_A$ ) extracted above. Note that the C-V measurement directly extracts  $N_A$ ; by contrast, I-V characteristics are usually affected by incomplete ionization and contact resistance and thereby less suitable for model calibration.



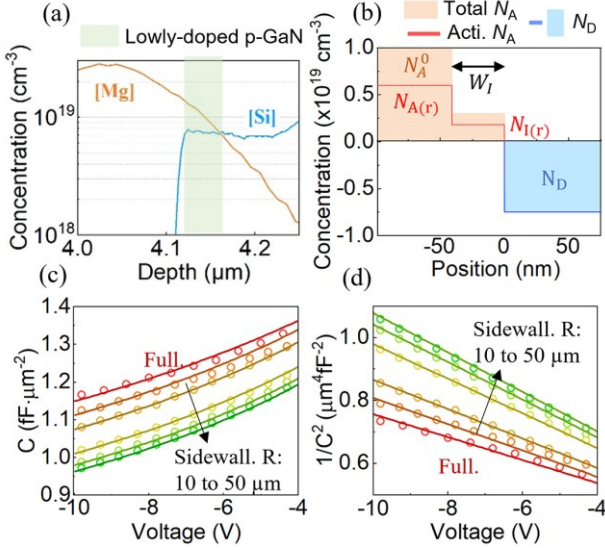


Fig. 6. (a) Zoom-in view of the [Mg] and [Si] profile near the p-n junction. (b) Simplified model for the interfacial p-GaN region, consisting of a lowly doped region with an effective acceptor concentration  $N_{I(r)}$  and a width  $W_I$ ; the ionized acceptor (red line) is lower than the total acceptor concentration due to the non-100% activation efficiency. (c) C-V characteristics and (d)  $1/C^2$ -V plot of the fully activated diodes (red) and sidewall activated device with  $R$  from 10 to 50  $\mu\text{m}$  (orange to green) after 1 hour activation. The solid lines are modeling results and circular symbols are experimental results.

If the dopant profile near the p-n junction is scrutinized, one can find that the junction may not be best described as an abrupt junction. As shown in Fig. 6(a), while [Si] increase is sharp, [Mg] shows a tailing effect, producing a  $\sim 50$  nm wide region with [Mg] > [Si]. As the interface is not our main focus, for the capacitance modeling, we used a lowly doped p-GaN region with an effectively average  $N_A$  to represent this gradient p-GaN region close to the p-n junction. As shown in Fig. 6(b), the acceptor/donor concentration along the vertical axis ( $Z$  axis with  $Z = 0$  at the p-n junction) can be written as

$$\begin{aligned} N_{A(r)} &= N_A^0 - [H](r) = \eta(r) \cdot N_A^0 & (Z < W_I) \\ N_{I(r)} & & (W_I < Z < 0) \\ N_{D(r)} &= N_D & (Z > 0) \end{aligned} \quad (5)$$

where  $N_{A(r)}$  and  $\eta(r)$  are the  $N_A$  and  $\eta$  at the radius  $r$ ;  $N_{I(r)}$  and  $W_I$  are the effective  $N_A$  and width of the interfacial region with gradient doping;  $N_D$  is the donor concentration in n-GaN.

The model in (5) was first applied to fit the C-V data of the fully-activated diodes (Fig. 6(c)), the model of which is based on a 100%  $\eta(r)$ . The fitting gives a  $N_I = 0.3 \cdot N_A^0$  and  $W_I = 41$  nm, which generally accord with the SIMS data shown in Fig. 6(a). For sidewall-activated diodes with the  $N_A$  dependent on  $r$ , we assume the same  $W_I$  and a  $r$ -dependent  $N_I$  that follows  $N_{I(r)} = 0.3 \cdot N_{A(r)}$ . Note that, at a reverse bias  $V$ , the  $N_{A(r)}$  profile will produce a depletion width dependent on  $r$  and a non-planar depletion front in p-GaN, and the total depletion capacitance ( $C_V$ ) can be calculated by integrating the specific capacitance ( $c_{(r,V)}$ ) along  $r$  up to  $r = R$ :

$$c_{(r,V)} = \frac{\epsilon}{W_{dep}} = \sqrt{\frac{\epsilon^2 q N_{A(r)} N_D}{2\epsilon(N_{A(r)} + N_D)(\phi_{bi} - V) + \delta(r)}} \quad (6)$$

$$C_V = \int_0^R 2\pi r c_{(r,V)} dr \quad (7)$$

where  $W_{dep}$  is the local depletion width,  $\phi_{bi}$  is the built-in potential of the GaN p-n junction, and  $\epsilon$  is GaN's permittivity.  $\delta(r)$  is a term related to the lowly-doped p-GaN close to the junction. Based on the Poisson equation as well as the E-field and potential continuity,  $\delta(r)$  can be calculated as

$$\delta(r) = qW_I^2(N_{A(r)}N_D + N_{A(r)}N_{I(r)} - N_{I(r)}^2 - N_DN_{I(r)}) \quad (8)$$

The modeled C-V characteristics based on (1)-(8) for fully-activated diodes and sidewall-activated diodes with various radii show a good agreement with the experimental C-V data of the counterpart devices (Fig. 6(c)). The aforementioned  $D$  and  $A$  values that provide the best fitting are also consistent with prior reports ( $D = 10^{-8} \sim 10^{-11}$  cm<sup>2</sup>/s [21], [27], [31],  $A \sim 10^{-3}$  /s [26], [31]). Here the C-V calibration was performed at reverse biases below -4 V to ensure that the depletion region has extended beyond the junction region into the bulk p-GaN region, i.e., the region of our interest in this work.

For these diodes that comprise the p-GaN with non-uniform  $N_{A(r)}$ , interestingly, their  $1/C^2 \sim V$  data shows a good linearity similarly to the uniformly-doped diodes, as shown in Fig. 6(d). This suggests the viability to extract a radius-average  $N_A$  that will give rise to the same  $C$  as  $N_{A(r)}$  does for a  $r$  range from 0 to  $R$ . Note that, despite the feasibility of such extraction using the slope of  $1/C^2 \sim V$  data, their x-axis intercept is  $R$  dependent and larger than  $\phi_{bi}$  of GaN p-n junction, due to the  $\delta(r)$  term.

## V. BREAKDOWN AND LEAKAGE MECHANISM

Despite the knowledge of the  $N_{A(r)}$  profile, the breakdown and leakage mechanisms of the partially activated p-GaN remain unclear. TCAD simulations were performed in Silvaco Atlas for GaN p-n diodes with such a  $N_{A(r)}$  profile. The device models are based on our prior reports [24], [40], and the  $N_{A(r)}$  profile is implemented through fine meshing. Fig. 7(a) shows the simulated E-field in a sidewall-activated GaN p-n diode with  $R = 10$   $\mu\text{m}$  and  $t = 0.5$  hour at a reverse bias of -10 V, revealing a peak E-field at the device edge.

To probe the leakage mechanisms, the reverse leakage current ( $I_R$ ) normalized to device perimeter is plotted against the peak E-field at the edge ( $E_{peak}$ ). Similar to the capacitance derivation,  $E_{peak}$  can be derived using the modeled  $N_{A(r)}$ :

$$E_{peak} = \frac{qW_I N_D (N_{I(R)} - N_{A(R)}) + \epsilon q N_{A(R)} N_D / c_{(R,V)}}{(N_{A(R)} + N_D)\epsilon} \quad (9)$$

where  $c_{(R,V)}$  is calculated from (6). Fig. 7(b) and (c) show the  $I_R$  v.s.  $E_{peak}$  characteristics converted from the experimental I-V characteristics for two sidewall-activated diodes with  $R$  of 10 and 75  $\mu\text{m}$  at various temperatures from 20  $^\circ\text{C}$  to 150  $^\circ\text{C}$ . The annealing time of two diodes are both 0.5 hours. Note that p-GaN in both diodes are partially activated.  $N_{A(R)}$  is determined by our model to be  $7.2 \times 10^{18}$  cm<sup>-3</sup> for  $R = 10$   $\mu\text{m}$  after 0.5 hour activation [see Fig. 5(b)].

Although most area of the 75  $\mu\text{m}$  diode is not activated, its  $I_R$  characteristics is almost identical to that of the 10  $\mu\text{m}$  diode. This suggests that the leakage current is dominated by the edge area with the highest  $\eta$ . Note that, as the activation first occurs at the edge area [see Fig. 5(c)], the local  $\eta$  is modeled to be similar in the diodes with different  $R$ .

Fig. 7(d) and (e) show the  $I_R$  v.s.  $E_{peak}$  characteristics of the fully(surface)-activated and non-activated diodes. Here  $I_R$  is

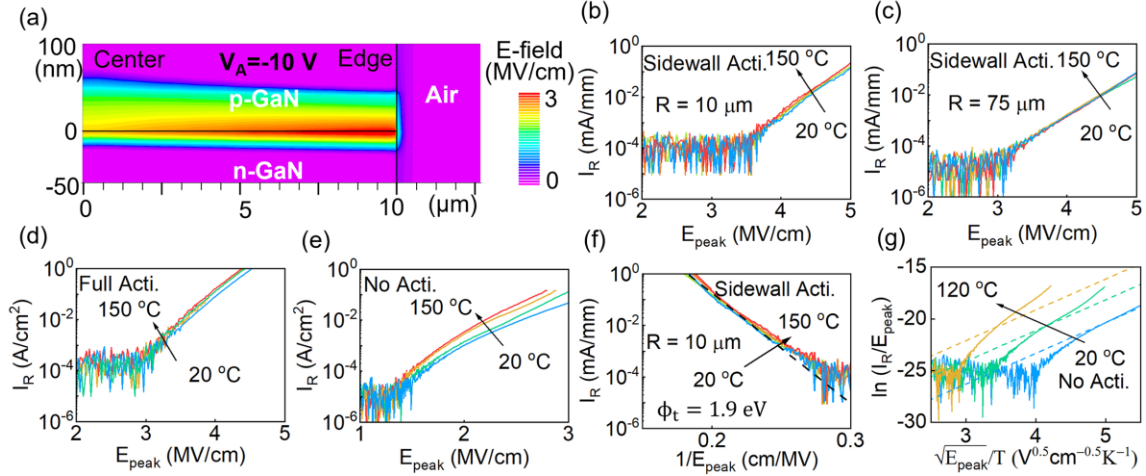


Fig. 7. (a) Simulated E-field contours in a sidewall-activated p-n diode with  $R = 10 \mu\text{m}$  at a reverse bias of  $-10 \text{ V}$ .  $I_R$  v.s.  $E_{\text{peak}}$  characteristic of the sidewall-activated diodes with  $R$  of (b)  $10 \mu\text{m}$  and (c)  $75 \mu\text{m}$  as well as the (d) fully- and (e) non-activated p-n diodes at temperatures of 20, 70, 120 and  $150^\circ\text{C}$ . (f)  $I_R$  v.s.  $1/E_{\text{peak}}$  plot and fitting for the sidewall-activated diodes. (g)  $\ln(I_R/E_{\text{peak}})$  v.s.  $\sqrt{E_{\text{peak}}}/T$  plot and fitting for the non-activated diodes. Note that the difference in the noise current density is due to the same noise floor of the curve tracer normalized to a different area/perimeter.

normalized to device area due to the uniform  $N_A$ , and  $E_{\text{peak}}$  represents the junction E-field that is calculated using the  $N_A$  extracted from C-V data. The  $I_R$ - $E_{\text{peak}}$ - $T$  characteristics of fully- and partially-activated diodes are similar, both showing little  $T$  dependence, while the  $I_R$ - $E_{\text{peak}}$  characteristics of non-activated diodes are quite different and show a strong  $T$  dependence. Both fully- and partially-activated diodes can sustain a  $E_{\text{peak}}$  of at least  $3 \text{ MV/cm}$  before the leakage current ramps up beyond the noise floor. Note that the critical E-field of GaN at a similar  $N_A$  and  $N_D$  levels (i.e.,  $10^{18}\sim 10^{19} \text{ cm}^{-3}$ ) is predicted to be  $\sim 5 \text{ MV/cm}$  [41]. In comparison, the non-activated diode can only sustain a  $E_{\text{peak}}$  of  $\sim 1.3 \text{ MV/cm}$  before the rise of leakage current.

The E-field and temperature dependence of  $I_R$  in fully- and partially-activated diodes were found to be consistent with the trap-assisted tunneling (TAT) across the barrier of the p-n junction [42], [43]. This TAT current is weakly dependent on  $T$  and can be modeled as [42], [43]

$$I_{\text{TAT}} \propto \exp\left(\frac{-8\pi\sqrt{2qm_n^*}}{3hE}\phi_t^{\frac{3}{2}}\right) \quad (10)$$

where  $m_n^*$  is the electron effective mass,  $h$  is the Planck's constant, and  $\phi_t$  is the trap energy level. Fig. 7(f) shows the good linearity between  $\ln(I_R)$  and  $1/E_{\text{peak}}$  for a typical sidewall-activated diode, confirming the TAT model. A  $\phi_t \sim 1.9 \text{ eV}$  below conduction band is extracted from the fitting, which may correlate to threading dislocations [44].

Finally, the leakage mechanism of non-activated diodes was found to agree with the Poole-Frenkel (PF) emission model, i.e., the E-field assisted trap ionization and carrier emission to the conduction band [16], [45]. The PF model features a linear relation between  $\ln(I_R/E)$  and  $\sqrt{E}/T$  [16], [45], which agrees with the experimental  $I_R$ - $E_{\text{peak}}$ - $T$  characteristics of the non-activated diodes (Fig. 7(g)). This PF mechanism, in conjunction with the lower sustainable  $E_{\text{peak}}$ , are consistent with the expectation from a high trap concentration in the non-activated p-GaN. At 70 and  $120^\circ\text{C}$ ,  $I_R$  shows a faster increase with  $E_{\text{peak}}$  than the prediction by the PF model, implying contributions from other leakage mechanism at elevated temperatures, which could be the variable-range-hopping along trap states [45], [46].

## VI. SUMMARY AND DISCUSSION

In summary, this work unveils the  $N_A$  activation efficiency profile, E-field distribution, and leakage mechanisms of a thick buried p-GaN activated through the etched sidewalls. Our model reveals the spatial  $N_A$  distribution and its evolution with the annealing time. The partially activated GaN p-n junction was found to be able to block a high E-field over  $3 \text{ MV/cm}$  with a leakage current mechanism similar to that in the fully activated counterpart. Whereas its breakdown field and leakage current are only determined by the edge area.

These results can provide two major implications for the buried p-GaN activated at different annealing conditions. First, our model contains two fitting parameters,  $D$  and  $A$ , which are processing-related. For example,  $D$  and  $A$  may be altered by the annealing temperature and ambient atmosphere, respectively. Second, as the edge area dominates the breakdown field and leakage current, the blocking characteristics of the sidewall activated p-n junction can be insensitive to the annealing condition, given a sufficient annealing time. This is because the  $\eta$  at the edge region can approach 100% for a sufficient annealing time, regardless of the activation temperature, ambient atmosphere and device size.

These results and implications provide key information for the future design and processing of large-area, advanced GaN devices comprising the buried p-GaN (e.g., GaN superjunction devices).

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