First Demonstration of Vertical Superjunction Diode in GaN

Ming Xiao[1ξ*], Yunwei Ma[1ξ*], Zhonghao Du[2], Yuan Qin[1], Kai Liu[3], Kai Cheng[3], Florin Udrea[4], Andy Xie[5], Edward Beam[5], Boyan Wang[1], Joseph Spencer[1,6], Marko Tadjer[6], Travis Anderson[6], Han Wang[2*], Yuhao Zhang[1*]
[1]Center for Power Electronics Systems (CPES), Virginia Polytechnic Institute and State University, Blacksburg, VA USA
[2]Ming Hsieh Department of Electrical and Computer Engineering, University of Southern California, Los Angeles, CA USA
[3]Enkris Semiconductor, Inc., Suzhou, Jiangsu China [4]Department of Engineering, University of Cambridge, Cambridge UK
[5]Qorvo, Inc., Richardson, TX USA [6]U.S. Naval Research Laboratory, Washington, DC USA
[ξ]The two authors contributed equally to this work. *Email: {mxiao, yunwei, yhzhang}@vt.edu, han.wang.4@usc.edu

***Abstract*—We report the first experimental demonstration of a vertical superjunction device in GaN. P-type nickel oxide (NiO) is sputtered conformally in 6 µm deep n-GaN trenches. Sputter recipe is tuned to enable 10^{17} cm^{-3} level acceptor concentration in NiO, easing its charge balance with the 9×10^{16} cm^{-3} doped n-GaN. Vertical GaN superjunction p-n diodes (SJ-PNDs) are fabricated on both native GaN and low-cost sapphire substrates. GaN SJ-PNDs on GaN and sapphire both show a breakdown voltage (BV) of 1100 V, being at least 900 V higher than their 1-D PND counterparts. The differential specific on-resistance ($R_{ON,SP}$) of the two SJ-PNDs are both 0.3 mΩ·cm^2, with the drift region resistance ($R_{DR,SP}$) extracted to be 0.15 mΩ·cm^2. The $R_{ON,SP}$~BV trade-off is among the best in GaN-on-GaN diodes and sets a new record for vertical GaN devices on foreign substrates. The $R_{DR,SP}$~BV trade-off exceeds the 1-D GaN limit, fulfilling the superjunction functionality in GaN.

I. Introduction

A 1-D, unipolar power device is theoretically limited by a trade-off that specific on-resistance ($R_{ON,SP}$) increases with the square of breakdown voltage (BV). A vertical superjunction can break this limit [1]. It comprises multiple, alternate n- and p-type pillars with relatively high doping and balanced charges. Its $R_{ON,SP}$ is much lower than 1-D devices and linearly increase with BV. Superjunction has achieved commercial success in Si [1] and been recently demonstrated in SiC [2], [3], enabling device performance beyond the 1-D Si and SiC unipolar limits.

The superjunction also promises breakthrough advances in GaN. Despite many simulation studies [4], [5], no vertical GaN superjunction device has been experimentally demonstrated. The superjunction concept was applied to polarization charges [6] in lateral GaN diodes [7], [8] and HEMTs [9]. However, lateral superjunction still holds a $R_{ON,SP} \propto BV^2$ limit [1], which is inferior to that of vertical superjunction ($R_{ON,SP} \propto BV$).

Superjunction is usually fabricated by the filling epitaxy in deep trenches or the multiple rounds of ion implantation and epitaxy [1]. The realization of superjunction in GaN is hindered by process challenges in each way, particularly on the selective, deep p-GaN doping [10] with precisely controlled acceptor concentration (N_A) to balance the donor (N_D) in n-GaN.

This work explores an alternative p-type semiconductor, nickel oxide (NiO), to form p-n junction with n-GaN pillars in deep trenches. NiO has a bandgap of 3.4~4 eV, a projected critical field (E_C) up to 5 MV/cm, and dielectric constant (11.9) larger than GaN [11], suggesting the NiO/GaN hetero-junction is not limited by NiO breakdown and can exploit the E_C of GaN. NiO can be conformally sputtered to form p-n junctions on non-planar GaN structures. The NiO-wrapped GaN trigate [12] and fin-anode [13] have enabled kilovolts lateral GaN devices.

To use NiO for superjunction, a new challenge appears for charge balance, as the sputtered NiO usually has a high N_A of 10^{18}~10^{20} cm^{-3} (it is used as p$^+$-region in prior power devices). The feasibility of NiO sputter in deep trenches is also unknown. This work presents new processes to address these challenges. NiO with N_A down to 10^{16}~10^{17} cm^{-3} is realized with conformal coverage in 6-µm deep trenches. This enables us to demonstrate vertical GaN superjunction devices for the first time on both sapphire and GaN substrates with a BV over 1 kV.

II. Epitaxy and Device Designs

Fig. 1 shows the epi structure and schematic of our vertical GaN superjunction p-n diode (SJ-PND). The GaN-on-GaN epi comprises 40 nm p^{++}-GaN ([Mg]: 10^{20} cm^{-3}), 300 nm p-GaN ([Mg]: 10^{19} cm^{-3}), 8 µm n-GaN ([Si]: 9×10^{16} cm^{-3}), 0.8 µm n$^+$-GaN ([Si]: 2×10^{18} cm^{-3}) grown on 2-inch GaN substrates by MOCVD. Our superjunction simulations reveal an optimal n-pillar width (w_n) of 2~2.5 µm for this n-GaN doping [5]. The GaN-on-sapphire wafer has the identical epi except for a thick (4 µm) n^{++}-GaN ([Si]: 10^{19} cm^{-3}) inserted on sapphire to reduce the current crowding in quasi-vertical devices [14].

Another key epi design is deploying a GaN p-n junction on the drift region to confine the peak E-field in the native junction. This minimizes the risk for surface premature breakdown and enables evaluation of the true blocking capability of GaN SJ.

In our SJ-PND, each GaN pillar is wrapped around by NiO with the superjuntion length (thickness) L_{SJ} = 6 µm. The target sidewall NiO width $w_p = w_n N_D/(2N_A)$ for charge balance. The pillar spacing (S) is no smaller than $2w_p$. The anode metals on top of each pillar form Ohmic contacts to both p-GaN and NiO. The latter contact is critical to supply/extract charges for NiO. At the device edge, the width of the outmost GaN pillar is $w_n/2$. Its outer mesa is covered by dielectrics, which mechanically support a side metal pad connected with all pillar metals. This side pad is for probe contact and obviates the need to remove the NiO on top of pillars, as NiO is very difficult to etch.

Fig. 2 and 3 show the simulated E-field contours in two SJ-PNDs, in which NiO has different N_A (and w_p), making GaN trenches fully filled in one and partially filled in the other. Both SJ-PNDs show uniform longitudinal E-field (E_y), suggesting the full trench filling is not required for SJ-PNDs.

III. Lowering Acceptor Concentraion in NiO

The NiO p-type conductivity was reported to decrease with the oxygen partial pressure in sputtering [15]. To explore if such correlation applies to N_A, we experiment three sputter recipes with various Ar:O_2 flow ratios in the mixture gas: (*A*) only Ar, *(B)* 20:1, *(C)* 2:1, with details listed in Table I. In addition to sputter conditions, the annealing's impact on N_A is also studied.

GaN Schottky diode and NiO/GaN p-n diode are fabricated for C-V tests (Fig. 4). N_D in n-GaN is first extracted to be 8×10^{16} cm^{-3} (Fig. 5(a)). The N_A of NiO is then extracted from $1/C^2$-V data of NiO/GaN diodes using the model shown in Fig. 5(b). The N_A for *recipe A* is 5.2×10^{16} cm^{-3} and shows no change after annealing (Fig. 5(c)). The N_A for *recipe B* is 4.8×10^{17} cm^{-3} and reduces to 4.3×10^{17} cm^{-3} after annealing (Fig. 5(d)). The N_A of *recipe C* is too high for C-V extraction; the Hall measurement reveals a $>10^{19}$ cm^{-3} hole density, suggesting an even higher N_A. Hence, *recipes A* and *B* are selected for SJ-PND fabrication, leading to a target w_p of ~1.73 and ~0.23 μm, respectively.

IV. Device Fabrication

Fig. 6 shows the main fabrication steps. P-GaN Ohmic is first formed in stripes, followed by thickening contact metals with thick Ni on the top (Mask I). After the mesa etch, 2-μm SiO_2 is deposited by PECVD, followed by a patterned SiO_2 etch to expose the Mask I. Then GaN trenches are etched with a ~6.4 μm depth. S ranges from 0.8 to 2 μm and w_n ranges from 1 to 3 μm. After a TMAH treatment, the anode pad is deposited, and the cathode is formed at the backside (GaN-on-GaN) or a mesa down to n^{++}-GaN (GaN-on-sapphire). Finally, NiO is sputtered using *recipes A* and *B* with their respective target w_p, followed by a 225 °C annealing. In this process, the Ni in Mask I serves as the hard mask for pillar etch and forms Ohmic to the top NiO.

Fig. 7(a) shows the SEM images before the NiO sputtering, revealing smooth sidewalls in high-aspect-ratio GaN trenches. Fig. 7(b) shows the cross-section SEM images of the fabricated SJ-PND using *recipe B*, revealing the NiO conformal coverage. Fig. 7(c) shows the SJ-PND fabricated using *recipe A*. Due to a large w_p, NiO coalesces laterally first at the trench opening region, shielding the vertical filling growth in the trench and thus leaving voids. **Hence, *recipe B* is deployed for SJ-PNDs**. Besides SJ-PNDs, 1-D PNDs are fabricated as control devices.

V. Device Characteristics

Fig. 8 shows the reverse I-V characteristics of GaN PNDs fabricated on GaN and sapphire, revealing a BV of 190 V and 110 V, respectively. The BV of GaN-on-GaN PNDs is limited by high N_D; the junction E-field reaches 2.5 MV/cm. The lower BV in GaN-on-sapphire PNDs is due to high leakage current.

Fig. 9 and 10 show the reverse I-V characteristics of GaN SJ-PNDs on GaN and sapphire with w_n of 1~3 μm. At various w_n, BV increases as the charge imbalance reduces (Fig. 11). At w_n=2.5 μm (charge balance), both SJ-PNDs show a BV over 1100 V with ~10^{-2} A/cm^2 leakage current. Interestingly, the leakage current of GaN-on-sapphire SJ-PNDs is comparable to GaN-on-GaN SJ-PNDs, suggesting the major leakage path is not through n-GaN but possibly the GaN/NiO interface or in NiO, which are not sensitive to the dislocation density in GaN.

From the experimental BV, we estimate the average E-field near the NiO/GaN junction in superjunction, which is useful to evaluate the potential of BV scaling. The transversal E-field (E_x) in GaN and NiO as well as the E_y in GaN can be solved by

$$E_{x(GaN)} = qN_D w_n/2\varepsilon_{GaN};\ E_{x(NiO)} = qN_A w_p/\varepsilon_{NiO} \quad (1)$$

$$BV = E_{y(GaN)}L_{SJ} + E^2_{y(GaN)}\varepsilon_{GaN}/(2qN_D) \quad (2)$$

The E_x and E_y in GaN is derived to be 2.03 and 1.69 MV/cm at 1100 V, revealing a peak E-field of 2.64 MV/cm in GaN. For NiO, (2) is modified to solve E_y; E_y is 1.8 MV/cm. Combining the E_x of 1.5 MV/cm solved by (1), the peak E-field in NiO is 2.34 MV/cm, which is lower than that in GaN.

Fig. 12 shows the forward I-V characteristics of GaN-on-GaN SJ-PNDs with w_n=2.5 μm and S=1 μm, revealing a 3.2 V turn-on voltage (V_{ON}) and a differential $R_{ON,SP}$ of 0.3 mΩ·cm^2. In the subthreshold region, current ramps early due to the n-GaN/NiO junction turn-on. This becomes a very minor current path after $V > V_{ON}$ due to the high resistivity of NiO. GaN-on-sapphire SJ-PNDs show nearly identical V_{ON} and $R_{ON,SP}$.

The $R_{ON,SP}$ components are analyzed for GaN SJ-PNDs and PNDs on both substrates as detailed in Fig. 13. The analyses are aided by TLM measurements to extract the contact resistance and Schottky diodes fabricated after p-GaN removal (similar to those shown in Fig. 4). The drift region resistance ($R_{DR,SP}$) of both GaN SJ-PNDs is extracted to be 0.15 mΩ·cm^2, which is below the 1-D GaN limit (i.e., ~0.2 mΩ·cm^2 for BV of 1100 V).

VI. Benchmark and Summary

Fig. 14(a) benchmarks the differential $R_{ON,SP}$ *vs.* BV of our SJ-PNDs with prior vertical GaN diodes. Our performance is among the best in GaN-on-GaN diodes and sets a new record in GaN diodes on foreign substrates. Moreover, as compared to prior 1-D diodes, our SJ-PNDs show a more efficient utilization of the epitaxy thickness to boost BV (Fig. 14(b)), showcasing the superjunction benefit. Table II compares our GaN SJ-PNDs with SiC and Si SJ devices [2], [16], revealing a much lower $R_{ON,SP}$ of GaN SJ despite the largest w_n. Tremendous $R_{ON,SP}$ reduction can be realized thorough the further w_n scaling [1].

In summary, we demonstrate the first functional vertical GaN superjunction device using NiO as the p-type material. Our GaN SJ-PNDs fulfill the key SJ merits, e.g., BV boost at charge balance and a $R_{DR,SP}$ below the 1-D limit. These results mark the arrival of superjunction to vertical GaN devices.

Acknowledgement

We acknowledge the support from ONR monitored by Lynn Petersen (Grant N00014-21-1-2183), NSF (Grants ECCS-2036740 and 2036915), and EPSRC (Grant EP/W007614/1).

References

[1] F. Udrea *et al.*, *IEEE Trans. Electron Devices*, vol. 64, pp. 720, 2017.
[2] X. Zhong *et al.*, in *2016 Int. Symp. Power Semicond. Devices ICs,* pp. 231.
[3] T. Masuda *et al.*, in *2018 IEEE Int. Electron Devices Meet.*, pp. 8.1.
[4] Z. Li *et al.*, *IEEE Trans. Electron Devices*, vol. 60, pp. 3230, 2013.
[5] M. Xiao *et al.*, *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 7, pp. 1475, 2019.
[6] A. Nakajima *et al.*, *Appl. Phys. Lett.*, vol. 89, pp. 193501, 2006.
[7] H. Ishida *et al.*, in *2008 IEEE Int. Electron Devices Meet.*, pp. 1-4.
[8] S.-W. Han *et al.*, *IEEE Trans. Electron Devices*, vol. 68, pp. 5736, 2021.
[9] A. Nakajima *et al*, *IEEE Electron Device Lett.*, vol. 32, pp. 542, 2011.
[10] T. Narita *et al.*, *J. Appl. Phys.*, vol. 128, pp. 090901, 2020.
[11] J. A. Spencer *et al.*, *Appl. Phys. Rev.*, vol. 9, pp. 011315, 2022.
[12] Y. Ma *et al.*, *Appl. Phys. Lett.*, vol. 117, pp. 143506, 2020.
[13] M. Xiao *et al.*, in *2020 IEEE Int. Electron Devices Meet.*, pp. 5.4.
[14] Y. Zhang *et al.*, *Appl. Phys. Lett.*, vol. 111, pp. 163506, 2017.
[15] S. Nandy *et al.*, *J. Mater. Sci.*, vol. 42, pp. 5766, 2007.
[16] J. Sakakibara *et al.*, in *2008 Int. Symp. Power Semicond. Devices ICs,* pp. 299.

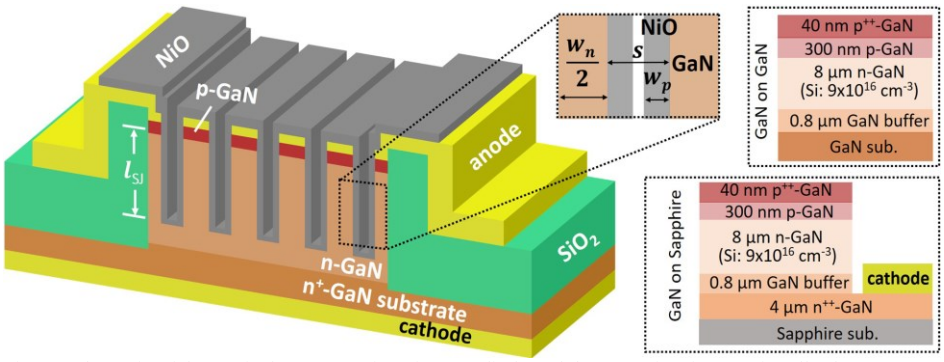


Fig. 1. Schematic of the vertical GaN superjunction p-n diode and the zoom-in of a SJ unit-cell. The contacts on each pillar are connected to the anode at the device periphery. The epi structures of GaN-on-GaN and GaN-on-sapphire wafers, as well as the cathode arrangement for quasi-vertical devices, are shown on the right.

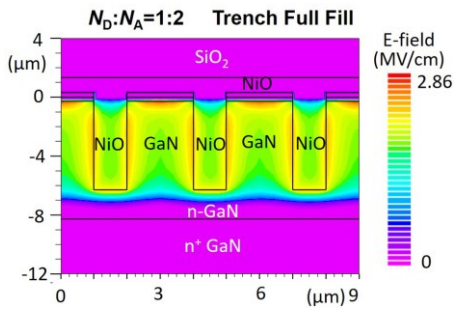


Fig. 2. Simulated E-field contours in a SJ-PND at 1200 V reverse bias, in which NiO fully fills n-GaN trenches. The peak E-field in the anode region is located at the GaN p-n junction and nearly identical to the peak E-field in SJ, minimizing the field crowding.

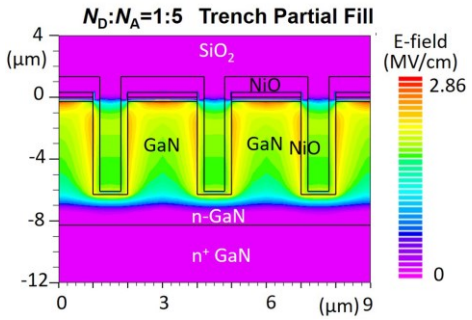


Fig. 3. Simulated E-field contours in a SJ-PND at 1200 V reverse bias, in which NiO covers the n-GaN pillar sidewall and partially fills n-GaN trenches. The peak E-field is identical to Fig. 2, validating this design.

TABLE I. NiO Sputtering Recipes.

Recipe	A	B	C
Ar flow (sccm)	61	59	40.6
O_2 flow (sccm)	0	2.9	20.3
Deposition rate @ large-area planar surface* (nm/min)	2.1	1.3	0.8
Deposition rate @ trench sidewall** (nm/min)	0.31	0.18	N/A
Common conditions	Pressure: 3 mTorr RF Power: 100 W Target material: NiO Temperature: 25 °C		

*rate on small-area surface is smaller
*estimated from cross-section SEM images

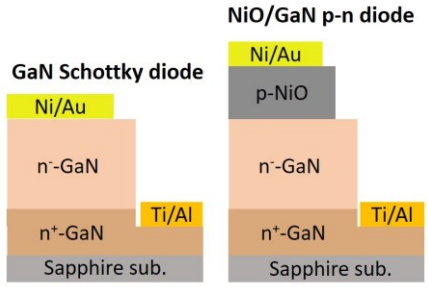


Fig. 4 Schematic of the fabricated GaN Schottky diode and NiO/GaN p-n diodes for C-V measurements. Ni forms Ohmic contact to p-NiO. The p-GaN layer is fully etched before the fabrication of these two diodes.

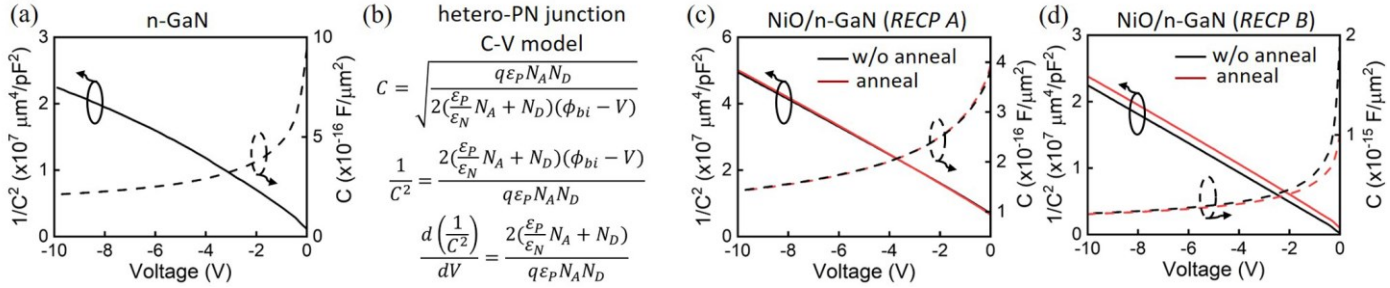


Fig. 5. (a) C-V and $1/C^2$-V characteristics of GaN Schottky diodes, with extracted $N_D = 8\times10^{16}$ cm^{-3} using $1/C^2$-V linear fit at -10~-4 V. (b) C-V model derived for a hetero-PN junction. C-V and $1/C^2$-V characteristics of NiO/GaN diodes with NiO sputtered using (c) recipe A and (d) recipe B, with and without a 225 °C annealing.

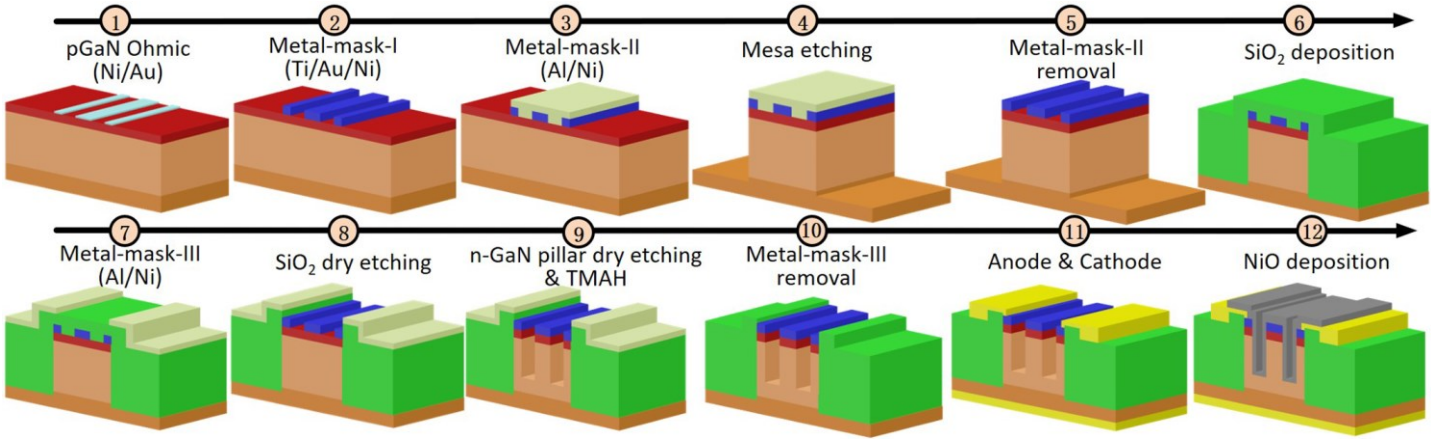


Fig. 6. Main steps in the fabrication process for GaN SJ-PNDs. In step 5 and 10, the Al/Ni metal hard mask can be removed by AZ developer without damaging other metals. The top Ni layer deposited in step 2 serves as the hard mask for GaN pillar etch in step 9 and forms the Ohmic contact to NiO deposited in step 12. For GaN-on-sapphire SJ-PNDs, the process is identical except for step 11, in which a window in SiO_2 is opened and the cathode is formed on the n^{++}-GaN layer. To show distinct metals, the contacts on top of each pillar are shown in blue (instead of yellow in Fig. 1). These pillar contacts are connected to the anode pad at the device periphery.

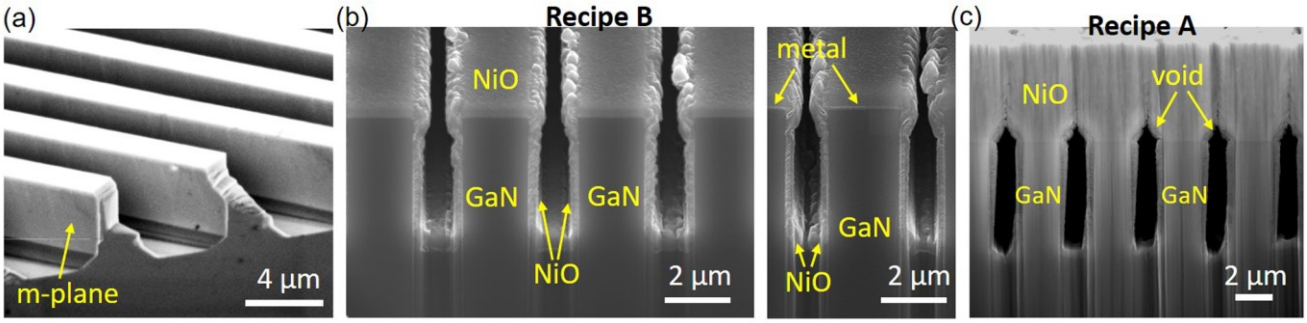


Fig. 7. (a) Side-view SEM images of the 6-μm deep GaN pillars. (b) Cross-section FIB-SEM images of the SJ region of the fabricated SJ-PNDs with (left) S=1.5 μm and (right) S=1 μm, using *recipe B* for NiO sputtering. (c) Cross-section SEMs of the SJ using *recipe A*, showing lateral NiO coalescence and the voids left in trenches.

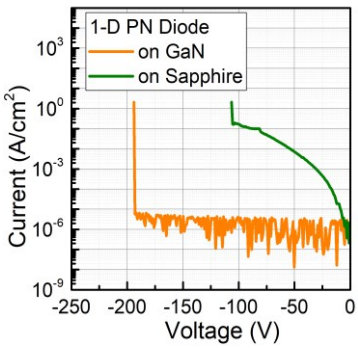


Fig. 8. Reverse I-V characteristics of 1-D PN diodes fabricated on GaN-on-GaN and GaN-on-sapphire.

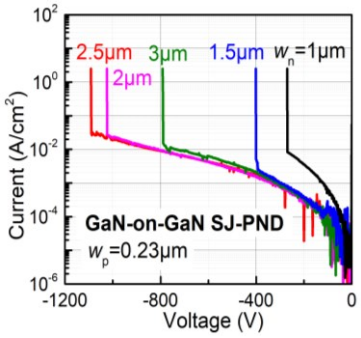


Fig. 9. Reverse I-V characteristics of the GaN-on-GaN SJ-PNDs with w_n of 1-3 μm. *Recipe B* is used for NiO with w_p=0.23 μm.

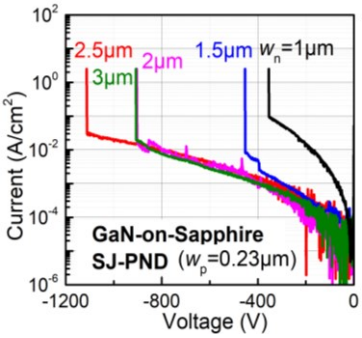


Fig. 10. Reverse I-V characteristics of GaN-on-sapphire SJ-PNDs with w_n of 1-3 μm. *Recipe B* is used for NiO with w_p=0.23 μm.

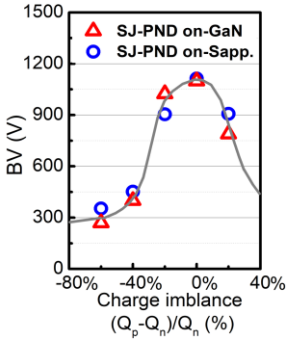


Fig. 11. The BV of SJ-PNDs as a function of charge imbalance in the SJ ($Q_n=w_nN_D/2$, $Q_p=w_pN_A$).

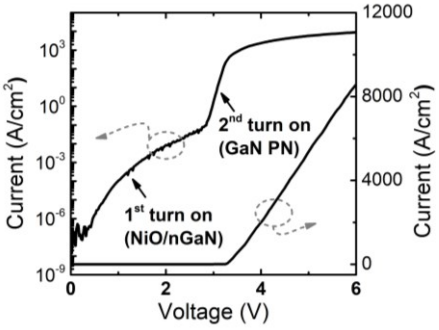
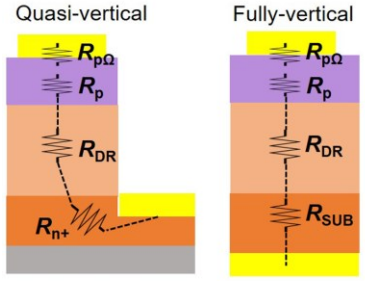


Fig. 12. Forward I-V characteristics of GaN SJ-PNDs plotted in semi-log and linear scales. The on/off ratio is over 10^{10}. The subthreshold region shows the first turn-on at NiO/GaN junction and the second at GaN p-n junction.



($m\Omega \cdot cm^2$)	R_{ON} component	GaN-on-GaN		GaN-on-sapphire	
		PND	SJ-PND*	PND	SJ-PND*
$R_{p\Omega}$	p-GaN Ohmic	0.05	0.08	0.05	0.08
R_p	p-GaN	0.025	0.03	0.025	0.03
R_{DR}	drift region	0.1	0.15	0.1	0.15
R_{SUB}	substrate	0.04	0.04	N/A	N/A
R_{n+}	spreading	N/A	N/A	0.04	0.04
R_{ON}	total, from IV	0.23	0.3	0.23	0.3

*SJ-PND: $w_n = 2.5\ \mu m; S = 1\ \mu m$

1) $R_{p\Omega}$, R_p and R_{DR} of SJ-PND larger than PND due to reduced conduction area
2) Small R_{SUB} due to the smaller device area (10^4~10^5X) than sample (cathode) size

Fig. 13. Schematic of the major R_{ON} components in quasi-vertical diodes and fully-vertical diodes, and the estimated R_{ON} component breakdown of GaN PNDs and SJ-PNDs on sapphire and GaN substrates. This analysis is aided by fabricating additional test structures (e.g., TLM, fully/quasi-vertical Schottky diodes).

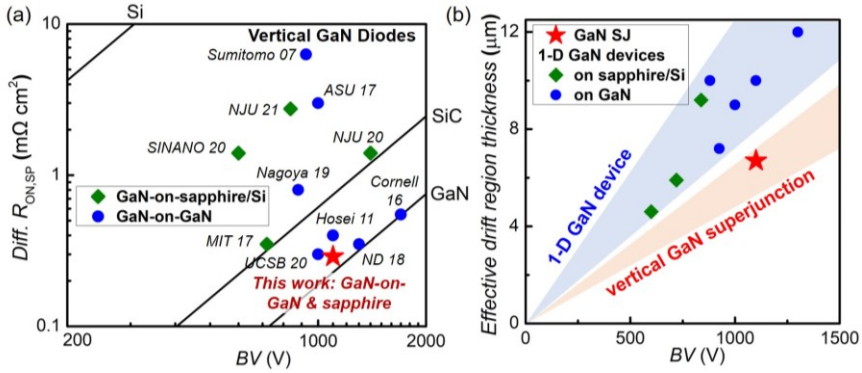


Fig. 14. (a) Differential $R_{ON,SP}$ *vs.* BV of our GaN SJ-PNDs and other 600-1700 V vertical GaN diodes on native and foreign substrates. (b) Effective drift region thickness *vs.* BV of the reported 1-D vertical GaN diodes (MOCVD/HVPE epi) and our SJ-PND, revealing the SJ's advantage in BV scaling on the thinner epi. Here the effective thickness is the thickness of the depleted drift region at BV. In our SJ-PND, this thickness is the SJ thickness plus the n-GaN depletion thickness below the SJ at 1100 V (totaling 6.8 μm).

TABLE II. Comparison between GaN SJ-PND and the state-of-the-art SiC SJ diode and Si SJ MOSFET, including BV, SJ length (L_{SJ}), n-type pillar width (w_n), $R_{ON,SP}$, and drift region resistance ($R_{DR,SP}$)

Device	BV (V)	L_{SJ} (μm)	w_n (μm)	$R_{ON,SP}$ ($m\Omega \cdot cm^2$)	$R_{DR,SP}$ ($m\Omega \cdot cm^2$)
GaN SJ-PND (this work)	**1100**	**6**	**2.5**	**0.3**	**0.15**
SiC SJ diode [2]	1350	6	2	0.92	0.32
Si SJ MOSFET [16]	685	37	1.7	7.8	N/A