# Dynamic Gate Breakdown of p-Gate GaN HEMTs in Inductive Power Switching

Bixuan Wang, *Student Member, IEEE*, Ruizhe Zhang, *Student Member, IEEE*, Hengyu Wang, Quanbo He, Qihao Song, *Student Member, IEEE*, Qiang Li, *Senior Member, IEEE*, Florin Udrea, *Member, IEEE*, and Yuhao Zhang, *Senior Member, IEEE*

***Abstract*—We employ a new circuit method to characterize the gate dynamic breakdown voltage ($BV_{dyn}$) of Schottky-type p-gate GaN HEMTs in power converters. Different from prior pulse I-V and DC stress tests, this method features a resonance-like gate ringing with the pulse width down to 20 ns and an inductive switching concurrently in the drain-source loop. At the increased pulse width, the gate $BV_{dyn}$ shows a decrease and then saturation at 21~22 V. Moreover, the gate $BV_{dyn}$ increases with temperature and is higher under the hard switching than that under the drain-source grounding condition. In the 400 V hard switching at 150 °C, the gate $BV_{dyn}$ reaches 27.5 V. Such impact of the drain switching locus and temperature on the gate $BV_{dyn}$ is not seen in Si and SiC power transistors tested in the same setup. These results are explained by a physics model that accounts for the electrostatics in the p-GaN gate stack in hard switching and at high temperatures. This work unveils new physics critical to the gate robustness of p-gate GaN HEMTs and manifest the necessity of the gate robustness evaluation in inductive switching conditions.[1]**

***Index Terms*— GaN, HEMT, power electronics, hard switching, gate, breakdown voltage, overvoltage, ruggedness, reliability.**

## I. Introduction

Gallium nitride (GaN) high-electron-mobility transistors (HEMTs) enable power electronics at very high frequency. Schottky-type p-gate GaN HEMTs (SP-HEMTs) are recently adopted by many device vendors and foundries as a common device platform [1]–[3]. A critical issue in their driver design is to suppress the gate-voltage ($V_G$) overshoot induced by the parasitic gate loop inductance or commutation crosstalk, as the margin between the typical drive voltage and the maximum allowable voltage of SP-HEMT can be as low as 1 V [4].

For SP-HEMT applications and protection circuit designs, in addition to the long-term gate lifetime, it is equally crucial to quantify the single-pulse gate overvoltage boundary, i.e., gate dynamic breakdown voltage ($BV_{dyn}$), in switching conditions that best resemble practical power converters. This information is important to evaluate the transient gate bias limit, which is being added to some SP-HEMT's datasheet, and the gate robustness against the single-event overvoltage stress. For example, resonant gate drivers comprise an inductor connected in series with the device gate [5], which could induce considerable surge energy and overvoltage to be withstood by the device gate under fault events.

Over the last several years, many groups used the DC tests with a constant-voltage stress or step-stress stress to study the gate breakdown of SP-HEMTs [6]–[13]. Recently, the square-wave pulse I-V test was used to study the gate breakdown and reliability [14]–[17]. The pulse I-V test identified the switching instead of DC phase to account for the gate overvoltage failure [14], [16], suggesting the need for switching tests.

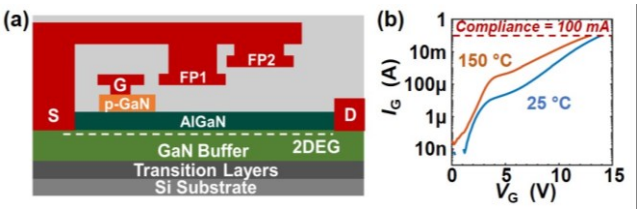


Fig. 1. (a) Schematic of the DUT. (b) Static $I_G$-$V_G$-$T$ characteristics measured with a 0.1 A compliance on Keysight B1505 Power Device Analyzer.

Despite the suitability for physics studies, DC and pulse I-V tests do not resemble the device operation in power converters: 1) the $V_G$ overshoot in converters is usually resonance-like with a waveform different from square-wave and a *dv/dt* higher than the pulse I-V test [18], [19]; 2) in inductive switching, e.g., hard switching (HSW), sharp changes in drain-source voltage ($V_{DS}$) and current ($I_{DS}$) occur concurrently with the $V_G$ overshoot, while most prior gate breakdown studies were performed under the drain-source grounding (DSG) condition. Recently, a pulse I-V test with the switching $V_{DS}$ produced by a resistive load was used for gate study [17]. This condition still differs from the usual converters with inductive loads.

While the drain $BV_{dyn}$ was recently revealed for GaN HEMTs [20], [21], the gate $BV_{dyn}$ under inductive switching has not been reported before. This work addresses this gap by developing a new circuit to mimic the $V_G$ overshoot in inductive converters, allowing for evaluating the gate $BV_{dyn}$ under the DSG and HSW conditions. The gate $BV_{dyn}$ of GaN SP-HEMTs is found to be higher under the HSW than that under the DSG and increase with temperature; these dependences are not observed in Si and SiC FETs tested under the same circuit.

## II. DUT and Circuit Design

The device under test (DUT) is a commercial 650V/30A GaN SP-HEMT [22] (Fig. 1(a)). Over 70 devices are tested, showing good statistical significance. Fig. 1(b) shows the static $I_G$-$V_G$ characteristics with 0.1 A compliance at 25 and 150 °C. DUT shows no failure or degradation after characterization.

Fig. 2 shows the design, working principles, and prototype of our circuit. The gate overvoltage study is performed in the DUT

[1]This work is supported in part by the Power Management Consortium of the Center for Power Electronics Systems at Virginia Tech and in part by the National Science Foundation under the Grants ECCS-2045001 and ECCS-2036740. B. Wang, R. Zhang, Q. Song, Q. Li, and Y. Zhang are with the Center of Power Electronics Systems, Virginia Polytechnic Institute and State University, Blacksburg, VA 24060 USA (e-mail: yhzhang@vt.edu).

H. Wang, Q. He, and F. Udrea are with the Department of Engineering, University of Cambridge, Cambridge, UK (email: fu10000@cam.ac.uk).

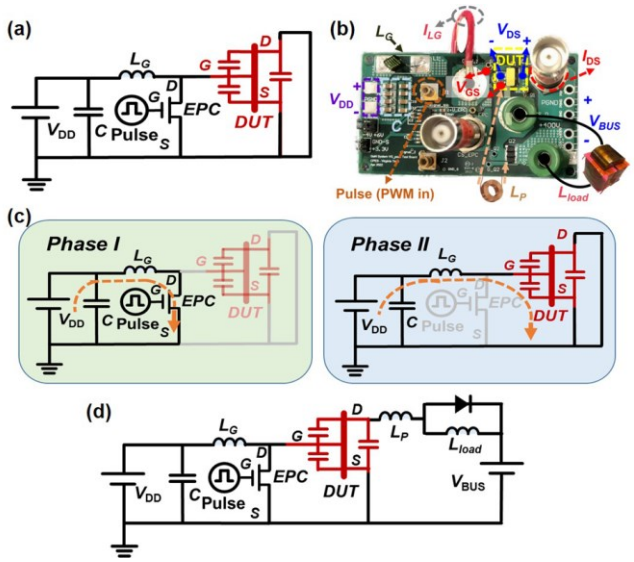


Fig. 2. (a) Schematic of gate overvoltage test circuit in the DSG condition. (b) Photo and (c) working principle of the test circuit. (d) Test schematic under hard-switching condition with the inductive load.

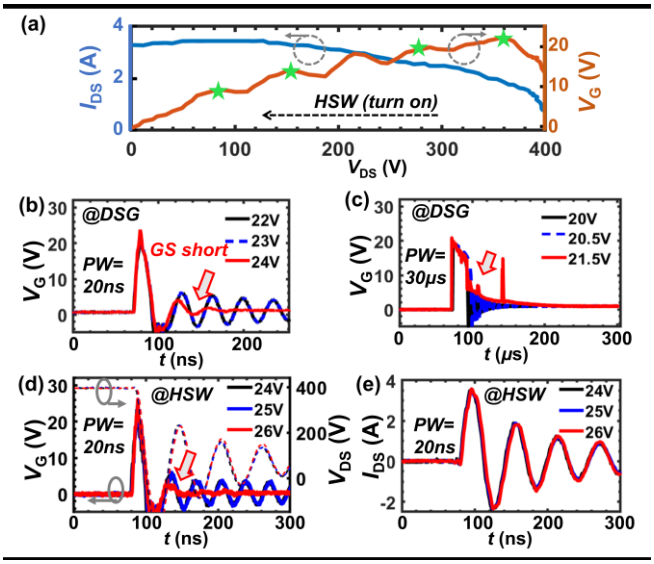


Fig. 3. (a) Switching locus in the gate overvoltage tests during hard turn on. The green symbols correspond to simulation conditions in Fig. 6. The failure and two survival $V_G$ waveforms under the DSG at pulse width (*PW*) of (b) 20 ns and (c) 30 µs. The failure and two survival waveforms of (d) $V_G$ (solid lines), $V_{DS}$ (dashed line), and (e) $I_{DS}$ under the HSW.

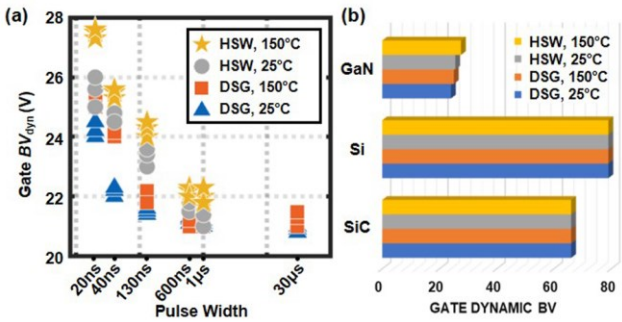


Fig. 4. (a) Gate $BV_{dyn}$ of GaN SP-HEMT as a function of pulse width under the DSG and HSW and at 25 and 150 °C. Three devices are tested for each condition. (b) Gate $BV_{dyn}$ of Si IGBT, SiC MOSFET and GaN SP-HEMT under the DSG and HSW and at 25 and 150 °C, all at a pulse width of 20 ns. Multiple Si and SiC devices are tested, showing nearly no variation.

turn-on process. The inductor $L_G$ mimics the gate loop parasitics. A low-voltage GaN HEMT (EPC2214 [23]) is used to create $V_G$ overshoot. In *phase I*, the EPC device is turned on, allowing $L_G$ to be charged by $V_{DD}$. In *phase II*, the EPC device is turned off, and the energy stored in $L_G$ creates an *RLC*-resonance-like $V_G$ overshoot at the DUT gate (*R* and *C* are the DUT's gate resistance and capacitance). This design is similar to the unclamped inductive switching used to create $V_{DS}$ overshoot and study the drain $BV_{dyn}$ [20], [21], [24].

The $V_{DD}$ (0.5 V) is lower than the DUT's threshold voltage to prevent the false turn-on. Several $L_G$ with inductances from 50 nH to 300 µH are used to tune the *dv/dt* and pulse width of the $V_G$ overshoot. For each $L_G$, the on-time of the EPC device is used to modulate the peak $V_G$ in the overshoot ($V_{G(PK)}$).

The circuit tests are first performed under the DSG condition for a direct comparison with the prior static/pulse I-V results (Fig. 2(a)). Then the gate $BV_{dyn}$ is measured under the HSW. As shown in Fig. 2(d), the loop comprises a load inductor (24 mH), a free-wheeling diode [25], a 400 V bus voltage, and a capacitor bank. Another inductor ($L_P$ = 1 µH) is added to mimic the main loop parasitics, suppress the peak $I_{DS}$, and avoid the thermal runaway. Fig. 3(a) shows the experimental $I_{DS}$-$V_{DS}$ and $V_G$-$V_{DS}$ switching locus, revealing a concurrence of high $V_G$, $V_{DS}$ and $I_{DS}$, thus verifying the HSW condition.

The DUT temperature is controlled by a power resistor attached to its case and calibrated by a thermal camera. Based on the switching loss and the datasheet's transient thermal impedance, the junction temperature is < 1 °C higher than the case temperature in the single-pulse switching test.

## III. Circuit Test Results

Gate $BV_{dyn}$ tests are performed with a 0.5 V step increase in $V_{G(PK)}$. Under the DSG, the failure and two survival waveforms of $V_G$ are shown in Fig. 3(b) and (c) for two pulse widths (20 ns and 30 µs). In the 20 ns pulse, the $V_G$ overshoot exhibits a *dv/dt* over 2 V/ns, which is slightly higher than the typical *dv/dt* (1~2 V/ns) in high-frequency GaN converters. In the failure waveform, the $V_G$ ringing damps fast after $V_{G(PK)}$, suggesting a gate-source (G-S) short. Post-test characterizations reveal a destructive failure with the G-S resistance ranging from 0 to 1 MΩ. Devices after all the tests with $V_{G(PK)} < BV_{dyn}$ show no noticeable degradation. The gate $BV_{dyn}$ is over 20 V and higher than those reported in DC and pulse I-V tests [14], suggesting a higher $V_G$ headroom in ns~µs switching.

Fig. 3(d) and (e) show the failure and survival waveforms of $V_G$, $V_{DS}$ and $I_{DS}$ under the HSW with 20 ns pulse width. The destructive failure shows a similar G-S short, while no shorting is present between source and drain. These failure signatures are confirmed by static I-V of the failed devices.

Fig. 4(a) shows the gate $BV_{dyn}$ of GaN SP-HEMTs as a function of pulse width (ns~µs range) under the DSG and HSW at 25 and 150 °C. At least 3 DUTs are measured in each condition, exhibiting a small $BV_{dyn}$ variation below 0.3 V.

Under the DSG at 25 °C, $BV_{dyn}$ decreases with the pulse width from 24 V to 21 V and then saturates; at 150 °C, $BV_{dyn}$ is 1~1.5 V higher than that at 25 °C in short pulses and also saturates to

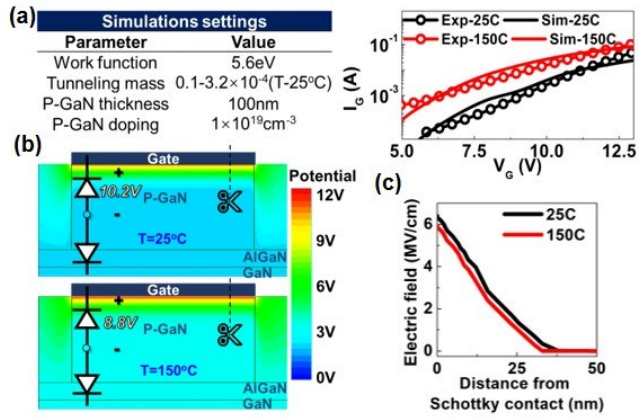


Fig. 5. (a) Key simulation parameters in the p-GaN gate simulation, and calibration of the simulated $I_G$-$V_G$ curve. (b) Simulated potential contours in the gate stack at $V_G$=12V at 25 and 150 °C. (c) Extracted electric field distribution along the cutline shown in (b).

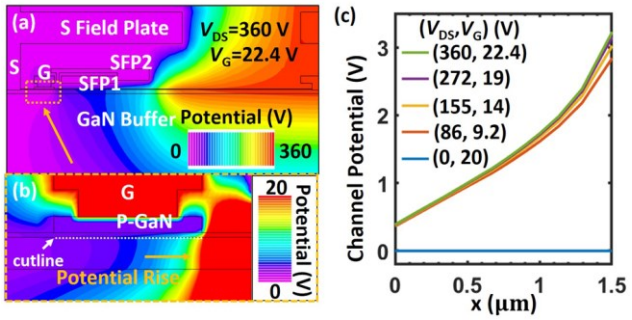


Fig. 6. Simulated potential contour in the (a) device and (b) gate region at the peak $V_G$ along the HSW locus. (c) Simulated potential in the channel below gate at four bias conditions along the HSW locus and under the DSG.

21 V. Under the HSW, the gate $BV_{dyn}$ is 2~2.5 V higher than that under the DSG. The highest $BV_{dyn}$ (27.5 V) is observed under the HSW with a 20 ns pulse at 150 °C.

The gate $BV_{dyn}$ of 650 V Si IGBT [26] and SiC MOSFET [27] are also measured using the same circuit setup, as shown in Fig. 4(b). The gate $BV_{dyn}$ of both devices show no dependence on temperature or the drain switching scheme, suggesting minimal impact of the drain stimuli on their MOS gate breakdown.

## IV. Physical Analysis and Simulation

The stronger impacts of temperature and switching locus on the gate $BV_{dyn}$ in GaN SP-HEMT originate from the non-insulating nature of the p-GaN gate as compared to the MOS gate. Its positive temperature coefficient ($\eta_T$) and saturation in long pulses cannot be explained by the thermal failure or the percolation-induced breakdown, which has a negative $\eta_T$ [7], [8]. We expand a model proposed in [14] to explain these dependences and give simulation validations. The simulation model is based on [28] with the DUT's structure on [24].

The SP-HEMT gate at high $V_G$ comprises a reverse-biased pGaN/gate Schottky junction in series with a forward-biased p-GaN/AlGaN/GaN pin junction. At high $V_G$, the pin junction injects electrons from the 2DEG into p-GaN, which then diffuse to the depleted p-GaN region, get accelerated by high electric field, and bombard the Schottky interface. This may degrade the local Schottky contact and turn it into Ohmic-like, leading to the crowded electric field and punch-through [14].

The gate $BV_{dyn}$'s saturation with the pulse width implies a threshold in the electric field or electron bombardment energy for the Schottky degradation. Such threshold is not reached at $V_G < 21$ V. Above this threshold, the local Schottky degradation may progressively accumulate until the destructive gate failure occurs. This progressive process can be accelerated by a higher electron bombardment energy, which explains the higher gate $BV_{dyn}$ under shorter pulses.

The temperature and switching locus impact the peak electric field at the p-GaN Schottky junction at a certain $V_G$, thus changing the gate $BV_{dyn}$. To explain the positive $\eta_T$, TCAD simulation with the models in [29] is calibrated with $I_G$-$V_G$ data (Fig. 5(a)). In the p-GaN gate, the reverse Schottky current ($I_R^{Sch}$) sets the forward pin current ($I_F^{pn}$). Simulation considers the $I_R^{Sch}$ at high $V_G$ to be induced by carrier tunneling across the Schottky barrier; the tunneling is thermally assisted [10] possibly due to dislocations. As shown in Fig. 5(b) and (c), at a certain $V_G$, as temperature rises, higher $I_R^{Sch}$ and $I_F^{pn}$ induce larger voltage drops in the non-depleted p-GaN and pin junction, decreasing the Schottky voltage drop and the junction electric field. The reduced field suppresses the electron bombardment, leading to a higher gate $BV_{dyn}$.

Some additional mechanisms can also contribute to the gate $BV_{dyn}$'s positive $\eta_T$, including the avalanche in the depleted p-GaN [14] and the hot electron transport in the non-depleted p-GaN. As the mean free path of hot electrons is small (~14 nm [30], [31]), only a portion of them can reach the depleted region. At higher temperatures, the mean free path reduces; a smaller number of hot electrons is accelerated in the depletion region and bombard the Schottky contact.

In the HSW, large $V_{DS}$ and $I_{DS}$ occur during the $V_G$ overshoot. The high $V_{DS}$ drives the DUT into saturation, expand the pinch-off region in the channel, and raise the potential along the channel. This is strengthened by channel voltage drop due to high $I_{DS}$. Fig. 6(a) and (b) show the simulated potential contour at $V_{DS}$ = 360 V and $V_G$ = 22.4 V, the peak $V_G$ condition on the switching locus [see Fig. 3(a)]. Fig. 6(c) shows the simulated channel potential at four bias conditions along the switching locus and under the DSG condition. The channel potential increase under the HSW condition reduces the actual voltage drop across the gate stack and makes the pin junction reverse-biased at the drain end of the gate, suppressing the electron injection into p-GaN and increasing the gate $BV_{dyn}$.

## V. Summary

This work characterizes the gate $BV_{dyn}$ of GaN SP-HEMTs using the converter-like $V_G$ overshoot. This new circuit method allows for the study of gate robustness in inductive switching that is not accessible via DC and pulse I-V tests. The gate $BV_{dyn}$ of GaN SP-HEMTs is found to be higher in hard switching and at higher temperatures. Such dependences are not observed in Si IGBTs and SiC MOSFETs. This distinction originates from the non-insulating gate stack in GaN SP-HEMTs, which leads to an interplay between the gate and channel electrostatics. These results provide direct references for GaN converter applications and reveal new physical insights for the evaluation and qualification of GaN HEMT gate ruggedness.

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