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Japanese Journal of Applied Physics **62**, SC0806 (2023) **PROGRESS REVIEW**

https://doi.org/**10.35848/1347-4065/acb365**

Power device breakdown mechanism and characterization: review and perspective

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Received November 14, 2022; revised January 11, 2023; accepted January 16, 2023; published online February 9, 2023

Breakdown voltage (BV) is arguably one of the most critical parameters for power devices. While avalanche breakdown is prevailing in silicon and silicon carbide devices, it is lacking in many wide bandgap (WBG) and ultra-wide bandgap (UWBG) devices, such as the gallium nitride high electron mobility transistor and existing UWBG devices, due to the deployment of junction-less device structures or the inherent material challenges of forming p-n junctions. This paper starts with a survey of avalanche and non-avalanche breakdown mechanisms in WBG and UWBG devices, followed by the distinction between the static and dynamic BV. Various BV characterization methods, including the static and pulse *I–V* sweep, unclamped and clamped inductive switching, as well as continuous overvoltage switching, are comparatively introduced. The device physics behind the time- and frequency-dependent BV as well as the enabling device structures for avalanche breakdown are also discussed. The paper concludes by identifying research gaps for understanding the breakdown of WBG and UWBG power devices.

1. Introduction

Power electronics is employed for electrical energy conversion in consumer electronics, electric vehicles, data centers, renewable energy systems, and electric grids, among many other applications. Central to a power electronics system is the power semiconductor device, which functions as a solid-state switch that blocks high voltage in the off-state, conducts high current in the on-state, and switches between the on- and off-states at high frequency.[1)] The global power semiconductor market has reached a value of about $40 billion in 2021 and is expected to exceed $50 billion by 2027.[2)]

Over the last several decades, a strong momentum for advances in power devices and power electronics is the adoption of wide-bandgap (WBG) semiconductors, such as gallium nitride (GaN) and silicon carbide (SiC). WBG devices such as the GaN high electron mobility transistors (HEMT) and SiC MOSFET have been commercialized, offering superior performance over silicon (Si) devices by advancing the efficiency, frequency, form factor, and power density of power electronics systems.[1,3–7)] On the horizon, power devices based on ultra-wide bandgap (UWBG) semiconductors such as gallium oxide (Ga_2O_3),[8–10)] aluminum nitride (AlN), aluminum gallium nitride (AlGaN),[11,12)] and diamond,[13)] are seeing fast progress. These devices promise theoretical limits superior to the WBG and Si counterparts.

Breakdown voltage (BV) is arguably one of the most important parameters for power devices. Si and WBG devices have demonstrated a very wide range of BV from a few volts[14)] to over 10 000 V.[15–18)] From the system requirement, some specific voltage ratings (e.g. 100 V, 600 V, 1200 V, 1700 V, 3300 V, 6500 V, 10 000 V) have been standardized for power devices. The BV should be designed to be higher than a specific voltage rating with a minimally sufficient overvoltage margin. This margin is required as the transient overvoltage is commonly seen in converters due to the unstable input voltage busbar, off-state voltage ringing,[19,20)] surge energy from the load,[21)] and the imbalanced voltage sharing in series device connection.[22)] On the other hand, the device specific on-resistance upscales with BV. Hence, an excessive BV margin compromises the device performance. To design the device BV and select the optimal margin, it is essential to understand the breakdown mechanism in power devices.

Avalanche is a desirable breakdown mechanism that has been realized in most of the commercially available Si and SiC power devices. The avalanche is an impact ionization (I. I.) and multiplication process that usually occurs at the p-n junction. This breakdown is non-destructive and allows the device to pass a relatively large current at BV. However, it is very challenging to realize the avalanche breakdown in many WBG and UWBG devices due to the limitations of either the device structure or the material property. For example, despite the good avalanche capability of GaN p-n junctions,[23)] the GaN HEMT has no p-n junction connected between the source and drain, leading to a minimal avalanche capability. In most UWBG materials, the formation of high-quality, native p-n junctions is hindered by the lack of efficient doping in either the n-type or the p-type[24,25)] For example, the p-type doping is nearly inviable in Ga_2O_3; the n-type doping is difficult in diamond; both donors and acceptors are deep in AlN. Despite the feasibility of polarization doping in AlGaN, the I. I. viability remains an open question. As a result, no avalanche breakdown has been reported in UWBG devices to date.

The breakdown in non-avalanche devices could have resulted from the premature breakdown in dielectrics and interfaces due to the non-optimal device designs. To study the intrinsic semiconductor breakdown in non-avalanche devices, devices with careful optimizations in the electric field (E-field) management are desirable. The recent availability of commercial GaN HEMTs with well-optimized field plates provides an excellent device platform. In addition, in the same GaN material system, the comparison between GaN HEMTs and other avalanche GaN devices makes it clear the enabling building block for avalanche breakdown. These

results have provided critical references for understanding the breakdown of the emerging UWBG devices. For example, breakdown behaviors similar to GaN HEMTs have been revealed in Ga_2O_3 devices.

Another field that recently generated new knowledge is the power device breakdown in switching transients, i.e. the dynamic breakdown. As power devices undergo switching in practical applications, the dynamic BV (BV_{DYN}) represents the device's true overvoltage margin in circuits. Particularly, for devices with considerable traps, as the carrier trapping/de-trapping is time-dependent, and the trapped carriers could impact the E-field profile, the device's BV_{DYN} can be time- and frequency-dependent. Recently, a few novel circuit methods have been developed to accurately measure the device's BV_{DYN} across various time scales down to the nanosecond scale or under continuous switching up to the megahertz frequency. These methods expanded the BV characterization tools beyond the conventional current–voltage (I–V) sweep.

This paper aims to overview the avalanche and non-avalanche breakdown mechanisms and the BV characterizations under static and dynamic conditions. Most mechanisms and characterizations focused on in this article are material agnostic and reflect the inherent properties of various power devices. This paper is organized as follows. Section 2 presents various breakdown mechanisms. Section 3 discusses the distinction between static and dynamic BV, followed by Sect. 4 surveying various BV characterization methods. Section 5 discusses the enabling device building block for avalanche breakdown. Section 6 discusses the immediate research needs and Sect. 7 concludes the whole paper. Note that this paper focuses on the device breakdown under the off-state drain-source (or anode-cathode) voltage; the gate breakdown[26] and the breakdown under the overcurrent conditions (e.g. surge current[23,27] short-circuit with high blocking voltage[28]) are also important failure mechanisms of power devices but will not be discussed in this paper.

2. Breakdown mechanisms

From the application standpoint, the breakdown mechanism of power devices can be divided into two categories, avalanche and non-avalanche breakdown. The avalanche breakdown is usually a non-destructive process and allows the device to pass a considerable current at BV. By contrast, the non-avalanche breakdown is often destructive and cannot accommodate much excessive current beyond the off-state leakage current. In this section, we discuss both breakdown mechanisms from the device physics perspective and exemplify them in various power transistors.

2.1. Avalanche breakdown

Avalanche breakdown relies on the I. I. and multiplication process that is initiated in the semiconductor region of the peak E-field in a power device. To maintain a sustained avalanche, the carriers produced in the I. I. and multiplication have to be effectively removed from the device structure. As an example, Fig. 1(a) illustrates the avalanche process in a power MOSFET. At a sufficiently high drain-to-source voltage (V_{DS}), the peak E-field is located at the p-n junction between the p-type base and n-type drift region, leading to the initiation of the I. I. there. The accelerated carriers collide with lattice atoms and generate an increasing number of electron-hole pairs. The generated holes are removed through the p-base and the source; the electrons are removed through the n-drift layer, substrate, and drain contact. The continued I. I. and multiplication as well as the effective carrier removal can support a considerable avalanche current (I_{AVA}).

Avalanche breakdown is desirable for power devices in two ways. From the device standpoint, avalanche breakdown is usually non-destructive, as the fast generation and effective removal of I. I. carriers prevent the further rise of the peak E-field and minimize the risk of electrical breakdown. In addition, the I. I. coefficient of either electron or hole in many materials including SiC[29,30] and GaN[31,32] has a negative temperature dependence, leading to a positive temperature coefficient of the avalanche BV (BV_{AVA}). As an example, Fig. 1(b) shows the temperature-dependent off-state I–V characteristics of a GaN p-n junction diode.[23] The BV_{AVA}'s positive temperature coefficient provides an additional overvoltage margin for power devices at elevated temperatures. From the system standpoint, the concurrence of high I_{AVA} and high V_{DS} in power devices produces a resistive heat dissipation, allowing for dissipating the system surge energy in power devices through avalanching. This dissipation prevents the continued circulation of surge energy in power converters, which may produce undesirable resonances among passive components and lead to destructive component failures.

The power device failure in avalanche breakdown is usually thermally limited. The critical parameter that represents the limit of avalanche breakdown is the energy instead of voltage. The critical avalanche energy (E_{AVA}) represents the maximum avalanche energy that a power device can endure without triggering the thermal runaway or reaching the intrinsic junction temperature limit. This E_{AVA} is included in the datasheet of many commercial devices. Comparable E_{AVA} has been revealed in GaN and SiC p-n junctions, with a density of E_{AVA} higher than Si.[23] In addition to thermal failure, in some power transistors such as MOSFET and insulated-gate bipolar transistor (IGBT), non-ideal avalanche failure mechanisms include the turn-on of the parasitic bipolar junction transistor (BJT)[33] and the parasitic thyristor,[34] respectively. As shown in Fig. 1(c), in a MOSFET, the parasitic BJT can be falsely turned on due to the high I_{AVA} flowing through the p-base and the decreased p-n junction built-in potential at high temperatures. This effect can induce direct thermal failure or a second avalanche breakdown at a much lower BV_{AVA}. While the failure induced by the parasitic BJT turn-on has been reported in SiC MOSFETs,[34,35] it is generally a less pressing issue in WBG and UWBG power transistors as compared to the Si counterpart due to the larger built-in potential of WBG and UWBG p-n junctions.

2.2. Non-avalanche breakdown

Avalanche breakdown is not a natural gift that comes with any power device; the non-avalanche breakdown is even more common. The mechanisms of non-avalanche breakdown are diverse, but they can be roughly grouped into two categories: (a) premature breakdown before the peak E-field in semiconductor is sufficient to initiate the I. I.; (b) after the I. I. initiates, the carrier removal is inefficient, leading to the local carrier accumulation and destructive E-field crowding. An obvious example of (a) is when the peak E-field in

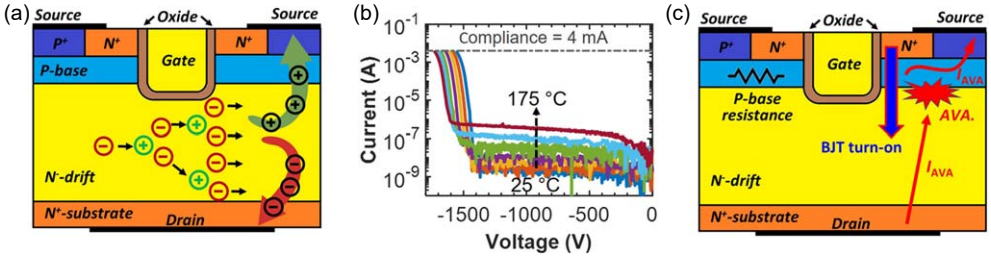

Fig. 1. (Color online) (a) Illustration of the avalanche breakdown in a power MOSFET. @ Copyright 2020 IEEE. Reprinted with permission from Ref. 21. (b) Off-state *I–V* characteristics of a GaN p-n diode at various temperatures. @ Copyright 2021 IEEE. Reprinted with permission from Ref. 23. (c) Illustration of the parasitic BJT turn-on in a power MOSFET induced by the avalanche current through the p-base and the resulted potential raise.

dielectrics and Schottky junctions reach the respective material breakdown field before that occurs in semiconductor. This leads to a destructive breakdown in dielectrics, surfaces, and interfaces without exploiting the full blocking capability of semiconductors. Some other mechanisms in (a) have been discussed for GaN HEMTs.[36] Here we focus on some less explicit non-avalanche breakdown mechanisms that occur in the semiconductor regions of power devices and expand the discussion into more diverse types of power devices.

Punch-through is a common premature breakdown mechanism. The high blocking voltage could weaken the critical potential/energy barrier in the main junction or channel, leading to the fast ramp-up of leakage current. Examples of the punch-through in power diodes include the full depletion of the p^+-type region in a p^+-n^- diode or the Schottky barrier lowering due to the image force. In power transistors, punch-through is commonly seen in junction-less field-effect transistors (FETs). An example is the fin-channel power MOSFET (Fin-MOSFET) [Fig. 2(a)], which realizes the enhancement-mode (E-mode) operation relying on the sidewall MOS gate stack to deplete the narrow fin channel.[25] This Fin-MOSFET has recently demonstrated excellent performance in GaN[37–41] and Ga_2O_3.[42,43] Its breakdown mechanism is found to be sensitive to the energy barrier in the fin channel, which is determined by the gate/drain biases, fin geometries, and interface charges.[44] At zero gate bias, a Fin-MOSFET with 450 nm fin width suffers from the punch-through [Fig. 2(b)] due to the drain-induced barrier lowering (DIBL) effect [Fig. 2(c)]. By shrinking the fin width, the channel barrier is raised to eliminate the DIBL and enable a much higher BV occurring at the edge termination [Fig. 2(d)].

A similar punch-through breakdown is also widely seen in the HEMT, another type of junction-less transistor, particularly at high temperatures and zero gate bias.[45,46] The punch-through usually places critical limitations on the gate length scaling, which is desirable to reduce the channel resistance, particularly for low-voltage power HEMTs. As a potential solution, a junction tri-gate gate stack has been recently proposed, which could strengthen the gate electrostatic control and eliminate the punch-through even at the scaled

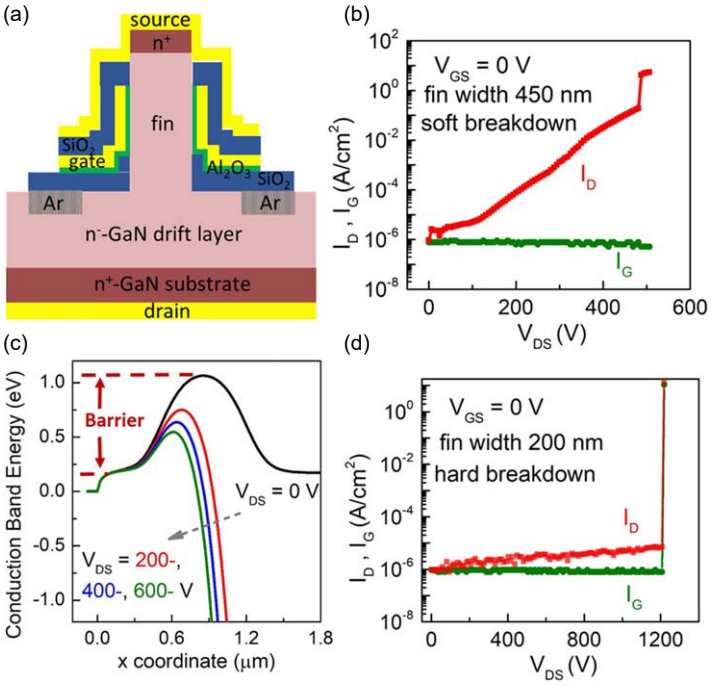

Fig. 2. (Color online) (a) Schematic of a vertical GaN Fin-MOSFET unit-cell. (b) Off-state *I–V* characteristics of a Fin-MOSFET with 450 nm fin width, showing a punch-through breakdown. (c) Conduction band diagram along the fin channel at different drain biases, showing the DIBL effect. (d) Off-state *I–V* characteristics of a Fin-MOSFET with 200 nm fin width, showing an E-field induced breakdown at the edge termination region. @ Copyright 2019 AIP. Reprinted with permission from Ref. 44.

gate length, at the same time maintain a kilovolt BV with good thermal stability.[45,47)]

Another premature breakdown mechanism is related to carrier trapping. Traps can capture free carriers, form fixed charges over a specific time span, and significantly impact the E-field distribution inside the device structure. Moreover, trapping can be strengthened by high blocking voltage and E-field, e.g. the Poole–Frenkel effect.[48)] A widely reported leakage current and breakdown mechanism associated with traps is the space-charge-limited current (SCLC).[49–55)] In the SCLC, free carriers in the leakage current are trapped, forming space charges that dominate the following carrier transport.[56,57)] The SCLC usually features a power-law I–V curve until a current hump occurs at the trap-filled-limited voltage (V_{TFL}), the voltage at which all local available traps are filled. The trap origins and locations can be very diverse, e.g. intrinsic dislocation and defects and those formed in device fabrication.

As an example, trap-assisted SCLC is widely reported in vertical GaN devices on foreign substrates, in which traps are in the epitaxial drift region originating from dislocations, defects, or background impurity doping (e.g. carbon).[58)] Figure 3(a) illustrates the leakage and breakdown in vertical GaN devices on foreign substrates, where the V_{TFL} is usually lower than the BV_{AVA} of the counterpart devices on native substrates. Another example involves the localized trap-filling in the edge termination region, which dominates the breakdown of a vertical GaN device.[55)] As shown in Fig. 3(b), at different temperatures, the sharp current humps

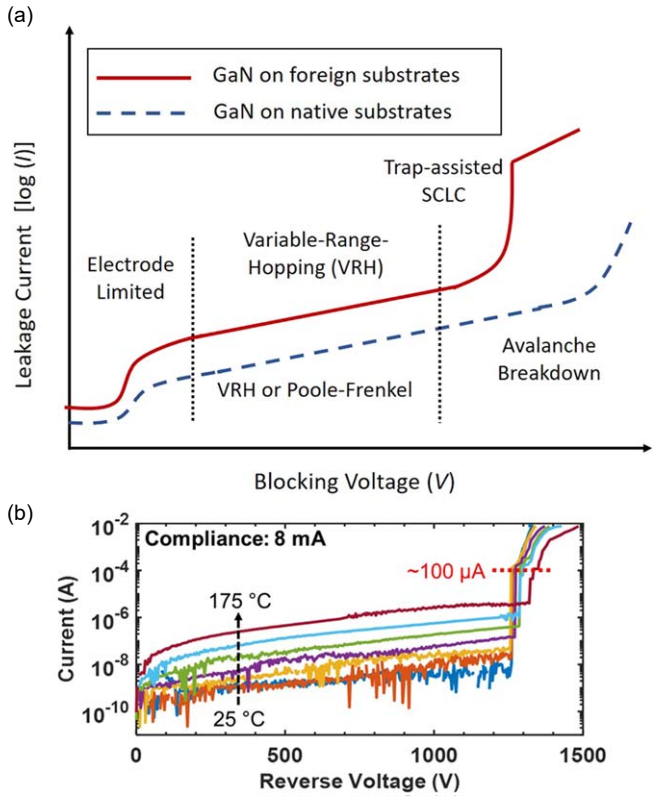

Fig. 3. (Color online) (a) Illustration of the off-state I–V characteristics of vertical GaN devices on foreign substrates (trap-assisted SCLC) and on native substrates (avalanche). (b) Reverse I–V characteristics of vertical GaN p-n diodes, showing the SCLC signature originated from the trap-filling in the edge termination region. Copyright @ 2020 IEEE. Reprinted with permission from Ref. 55.

ending at a similar current level indicate a trap-filling breakdown and its slightly positive temperature coefficient suggests that the V_{TFL} is very close to the avalanche regime. Finally, the trap-assisted SCLC could be a non-destructive breakdown, but it is difficult to accommodate a high current as in the avalanche and may suffer from poor repeatability due to the slow de-trapping of deep-level traps.

While the breakdown induced by punch-through and trap-filling is usually instantaneous, the material defects and the associated percolation process can also lead to a progressive breakdown. This percolation-induced breakdown is usually time-dependent and occurs at voltages much lower than the instantaneous BV. Broadly speaking, it can be viewed as a premature breakdown process on a longer time scale. This time-dependent breakdown has been reported in GaN-on-Si wafers between the drain contact and the Si substrate, which is ascribed primarily to a percolation process activated by the high E-field that leads to the generation of localized shunt paths.[59,60)] Other factors have also been reported to impact the percolation process and time-dependent BV, including the I. I. and Poole–Frenkel effects in the buffer layers[61,62)] as well as the substrate resistivity.[63)]

Through optimizations of the E-field management, material quality, and fabrication process, a power device could be devoid of premature breakdown in theory. However, this may not be sufficient to ensure an avalanche breakdown. The GaN HEMT is a good example.[64)] The peak E-field in commercial GaN HEMTs is usually located near the drain or in the gate-drain access region below the edge of the source field plates,[21)] as shown in Fig. 4(a). At high V_{DS} near the BV, I. I. initiates at these locations,[64–66)] producing excessive electrons and holes. While electrons are pulled out of the device from the drain, holes flow towards the buffer region, the substrate, and the p-GaN gate at which a negative bias is usually applied at the off-state. The hole removal is inefficient through either the gate stack or the substrate, due to the larger-bandgap AlGaN or AlN in the heterostructures or transition layers. Even in the gate injection transistor, which is known for the viability of hole injection from the p-GaN gate,[67)] the thin AlGaN barrier in the gate stack[68)] could still block the hole removal. This inefficient hole removal prevents the avalanche breakdown; the hole accumulation below the gate stack leads to the gate barrier lowering[64)] and E-field crowding, making the device suffer from a destructive breakdown.

Strong evidence for the I. I. and hole-limited breakdown in GaN HEMTs is recently revealed by repetitive switching tests.[69–72)] Commercial GaN HEMTs with various gate stacks are stressed to experience repetitive overvoltage switching near their BV. In each switching cycle, a voltage overshoot of up to 90% of BV is applied in the turn-off, and the device parametric shifts are monitored up to 1 million switching cycles. All these GaN HEMTs show the parametric shifts (e.g. threshold voltage, saturation current) as the consequence of the hole trapping in the gate stack and buffer region, and the device post-stress recovery is found to be dominated by the hole de-trapping and through-gate removal. Figs. 4(b)–4(d) show the simulated contours of the I. I. generation rate near the BV as well as the electron and hole current in the following off-state, respectively. These results suggest that hole removal is equally important as E-field

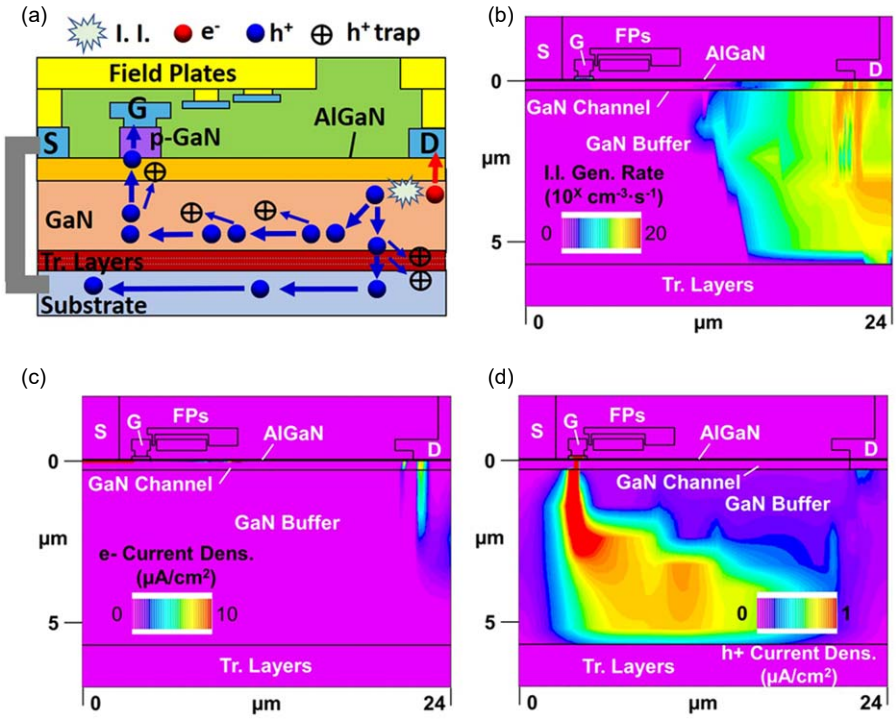

Fig. 4. (Color online) (a) Illustration of the carrier dynamics in the breakdown process of a GaN HEMT, including the impact ionization, electron removal, hole removal, and hole trapping. The simulated contours of (b) I. I. generation rate at V_{DS} near BV and the (c) electron current density and (d) hole current density in the following device off-state. "Tr." represents transitional, "FP" represents field plate; "S", "G" and "D" represent source, gate, and drain. (b)–(d): Copyright @ 2023 IEEE. Reprinted with permission from Ref. 69.

management for enabling the avalanche breakdown in power devices.

3. Static and dynamic BV

In power converters, BV quantifies the device overvoltage margin and provides a key reference for the control and protection circuitry. The device breakdown occurs in transient conditions with a usual slew rate (*dv/dt*) ranging from a few V ns^{-1} to over 100 V ns^{-1}. For example, in the turn-off process of WBG/UWBG devices, the circuit parasitic inductance could induce a resonant overvoltage on device with a *dv/dt* well above 100 V ns^{-1}.[21] This necessitates measuring the BV in the pulses down to the nanosecond (ns) scale. In some applications such as motor drives, under fault events, power device has to withstand the unclamped energy from the load. This energy also induces a resonant overvoltage, and its duration depends on the effective inductance of the load,[21] which can be much larger than the parasitic inductance. This necessitates measuring the transient BV over a wide spectrum of pulse durations. The BV measured in these transient processes is often referred to as the dynamic BV (BV_{DYN}), while the BV measured in a relatively long period (and very small slew rate) can be referred to as the static or quasi-static BV.

For avalanche devices, the BV measured in different time scales is usually identical and equal to the device's intrinsic BV_{AVA}. This applies to most unipolar power devices; some exceptions may exist in high-voltage bipolar devices due to the dynamic avalanche phenomenon.[73] Figure 5(a) illustrates the typical waveforms for the avalanche breakdown under various pulse widths. However, such a time independence may not hold for the non-avalanche BV, particularly for device structures with considerable traps. The non-avalanche

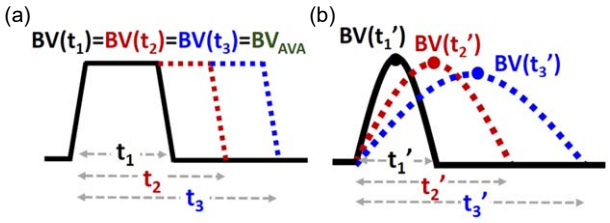

Fig. 5. (Color online) Illustration of the dynamic breakdown voltage of (a) avalanche devices and (b) non-avalanche devices in the overvoltage pulses with three different pulse widths.

BV is determined by the E-field profile and the peak E-field magnitude, both of which can be significantly impacted by the trapped charges. The carrier trapping and de-trapping are time-dependent and highly dependent on the electrical stress history. This suggests that the E-field profile and device BV can be also time-dependent, making the dynamic BV dependent on the pulse width (and frequency in continuous switching) and distinct from the static BV, as illustrated in Fig. 5(b). In the next session, we will introduce various methods to characterize the static and dynamic BV.

4. BV characterization methods

Overall, BV characterization can be grouped into two categories: the *I–V* sweep and the circuit-based test. In the *I–V* sweep, the device is constantly off with the leakage current measured as a function of the off-state bias until breakdown. In the circuit-based test, the device undergoes active switching with a controlled voltage overshoot to access its breakdown regime in dynamic conditions.

4.1. Static and pulse *I–V* sweep

The *I–V* sweep on a curve tracer is a routine BV measurement for bare-die and packaged power devices. There are

usually two voltage sweeping modes: the quasi-static *I–V* sweep, in which the voltage is applied in a staircase manner, and the pulse *I–V* sweep, in which each voltage is applied from a zero or constant quiescent bias condition. These two modes can give distinct results, such as the leakage current.[74] The advantages of the *I–V* sweep include the ease of test implementation and the accurate leakage current measurement. Using this method, the GaN HEMTs' static BV and BV_{DYN} with various pulse widths above 20 ms have been measured.[75]

A limitation of the *I–V* sweep is that the test condition deviates from the practical switching operation in inductive converters, as the device on-state and switching transients are missing. For example, the *I–V* sweep cannot measure the device BV_{DYN} in hard switching, in which high current and high voltage are applied concurrently. Besides, as compared to the converter operations,[76–78] the highest *dv/dt* provided by the pulse *I–V* measurement system is much lower. This gap may lead to a difference in BV_{DYN} measured in the pulse *I–V* sweep and practical converters, e.g. for various types of GaN HEMTs.[75] This comparison will be elaborated in Sect. 5.

4.2. Circuit-based measurement

A widely used circuit to characterize the breakdown for avalanche devices is the unclamped inductive switching (UIS) circuit,[55,79,80] as shown in Fig. 6(a). In a UIS test, the device is first turned on to charge the loop inductor (L_{loop}), then the device is turned off and the energy stored in L_{loop} triggers high voltage overshoot due to the resonance between L_{loop} and the device's output capacitor. Figure 6(b) illustrates the UIS test waveforms of an avalanche power device. The V_{DS} overshoot is clamped by the device's BV_{AVA}; the avalanche current (I_{AVA}) gradually reduces to zero, accompanied by the resistive dissipation of the energy originally stored in the L_{loop}. The E_{AVA} can be calculated through an integration of the product of voltage and current from the I_{DS}–V_{DS} waveform.

For non-avalanche devices, three circuits have been developed for BV_{DYN} characterization. Although the commercial GaN HEMTs are mainly studied, these methods are universal to all non-avalanche devices; some methods have already been deployed to characterize other emerging UWBG devices.

First, the UIS circuit is also suitable for non-avalanche devices. In the UIS waveform for non-avalanche devices, the resonance will not be clamped by BV_{AVA}; instead, the device fails when the peak resonant V_{DS} reaches BV_{DYN} [Fig. 6 (c)].[21,81] The amplitude and pulse period of this resonance can be tuned by the inductor charging time, value of the loop inductor, and an additional capacitor in parallel with the device,[75] covering a large range of *dv/dt* from hundreds of V s^{-1} to over 100 V ns^{-1}. The application of this method to GaN HEMTs unveils a strong dependence of BV_{DYN} on the pulse width.[75] Thanks to the simple circuit topology and setup, the UIS test has become very popular for BV_{DYN} characterization in various device technologies, e.g. UWBG Ga_2O_3 diodes,[82] various types of industrial GaN HEMTs,[83,84,85] emerging GaN diodes and HEMTs,[86,87] as well as for different applications, e.g. high and cryogenic temperature tests,[84,88] and on-wafer breakdown test.[89]

While the UIS resembles the device's soft-switched turn-off in converters, it cannot best mimic the hard-switched turn-off, as the input voltage (V_{in}) of the UIS test is usually very low and the device has minimal channel current during the voltage overshoot. To characterize the BV_{DYN} in hard switching, a clamped inductive switching (CIS) test can be employed.[21,70] Figure 7 shows the circuit schematic and typical waveforms of the CIS test. The circuit is similar to the double-pulse test with a freewheeling diode. The overvoltage is triggered by a small air-core inductor (L_{air}), mimicking the parasitic inductance of the PCB layout. In the CIS test, the V_{in} can be set as the typical busbar voltage in converters, i.e. 400 V for 600 V rated devices. The CIS tests applied to GaN HEMTs reveal an identical BV_{DYN} under the CIS and UIS

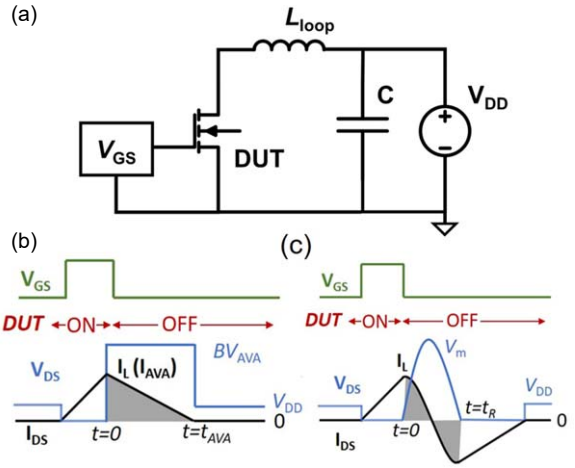

Fig. 6. (Color online) (a) Circuit schematic of the UIS test. Typical UIS waveforms of an (b) avalanche device and a (c) non-avalanche device. "DUT" represents the device under test.

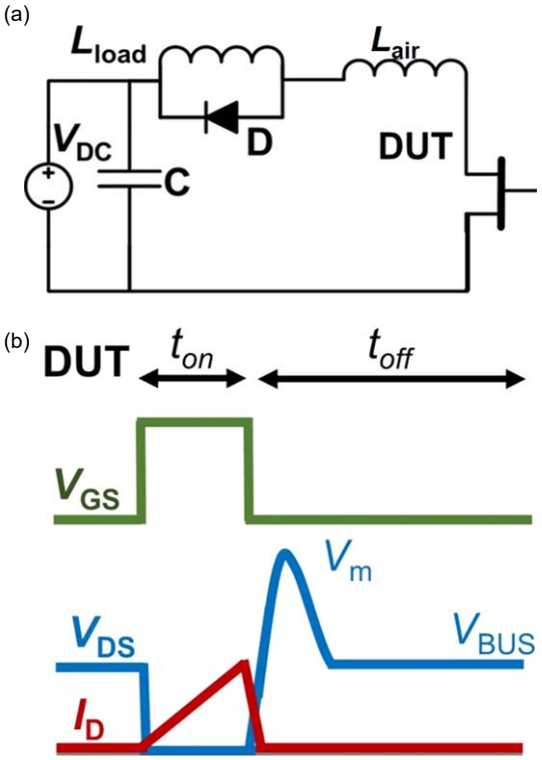

Fig. 7. (Color online) (a) Circuit schematic of the CIS test. (b) Illustration of the typical CIS waveforms. "D" represents the freewheeling diode. "L_{air}" represents an air-core inductor. "DUT" represents the device under test.

tests with a similar pulse period.[21,70,90] Repetitive CIS test has also been performed to study device degradation mechanisms in an overvoltage condition.[69,91,92]

A common limitation of the UIS and CIS tests is the difficulty of reaching a very high switching frequency (f_{sw}). In continuous switching, a stable peak overvoltage requires the inductive energy to fully dissipate in each switching cycle. For non-avalanche devices, as minimal energy can be dissipated in the resonance, the natural energy damping in the UIS or CIS tests is long. Therefore, the reported f_{sw} in repetitive UIS or CIS tests is usually only several kHz[86,91,93] up to a maximum of 100 kHz,[84,92] which is below the f_{sw} in many applications (hundreds of kHz).[76,77,94] To perform a high-frequency overvoltage test, an active clamping circuit (ACC) test is demonstrated.[95] The test circuit is illustrated in Fig. 8(a). It consists of a soft-switched buck converter with f_{sw} up to 1 MHz and peak overvoltage voltage above kilovolt. A L_{air} is to trigger a high V_{DS} overshoot in the device's hard turn-off transient, and an ACC is to dissipate the residual inductive energy in each switching cycle. Figure 8(b) shows the typical waveforms in the ACC test at 1 MHz f_{sw}. Each switching cycle contains one high V_{DS} overshoot with an average *dv/dt* around 100 V ns^{-1}. Recently, the ACC tests have been applied to multiple types of GaN HEMTs, unveiling their BV_{DYN} up to MHz, which will be discussed in the next section.

5. BV discrepancy in different testing conditions

In this section, two GaN devices, one with the avalanche capability and the other without, are used to showcase the discrepancy between the static and dynamic BV. Similar BV discrepancies reported in other material systems are also described.

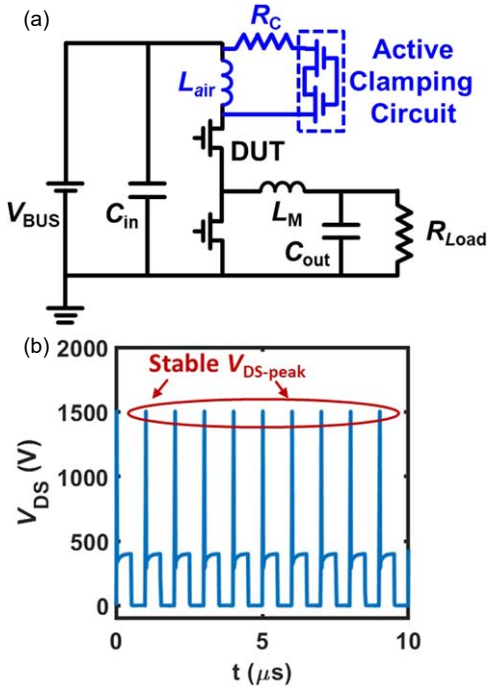

Fig. 8. (Color online) (a) Circuit schematic of the ACC test. (b) Testing waveforms obtained from ACC at 1 MHz. Copyright @ 2022 IEEE. Reprinted with permission from Ref. 95.

5.1. Avalanche BV discrepancy

In theory, BV_{AVA} is independent of the test conditions such as the pulse with or *dv/dt*. In some devices with trap-assisted premature breakdown, this argument may not hold. For example, a GaN p-n diode was recently reported to show a trap-assisted BV in the *I–V* sweep but an avalanche waveform in the UIS test; moreover, its static BV is ~400 V lower than the UIS BV_{AVA}.[55] The entire *I–V* data from the *I–V* sweep and the UIS tests with various load inductors is shown in Fig. 9 for the GaN p-n diode and a commercial SiC counterpart.

This interesting behavior is explained by a trap-mediated avalanche process. At 1300 V, I. I. occurs at the device edge termination region. The I. I. generated holes gradually fill the donor-like traps, leading to the trap-filling signature in the *I–V* sweep. This process reforms the charge distribution and reduces the peak E-filed. Then the voltage continues to ramp-up until the avalanche occurs in the device active region at 1700 V. In the UIS test, as the high I_{AVA} immediately fills the traps, the BV_{AVA} is present. A similar process has been reported in other materials[96] and devices[97] and may also be expected in future UWBG devices with deep trap-based edge termination.[98]

5.2. Non-avalanche BV discrepancy

Here we use the results of an E-mode p-gate GaN HEMT to showcase the BV measured by different approaches. This GaN HEMT shows a static BV of ~950 V in the quasi-static *I–V* sweep [Fig. 10(a)]. By using the pulse *I–V* sweep and UIS circuit test, the device's BV_{DYN} is found to increase with the decreased pulse width, reaching ~1450 V at a pulse width of 25 ns ($dv/dt > 100$ V ns^{-1}) [Fig. 10(b)].[75] The device's BV_{DYN} in the hard switching is also tested using the CIS circuit,[69,70,90] revealing a BV_{DYN} nearly identical to the UIS test result under a similar *dv/dt*. Finally, the BV_{DYN} is characterized by the ACC circuit up to 1 MHz continuous switching, and the device shows an electrothermal failure at a lower BV_{DYN} due to the significant on-resistance (and conduction loss) increase in the high-f_{SW} overvoltage switching.[99]

The above time- and frequency-dependent BV is explained by the dynamic trapping filling in the buffer region of the GaN HEMT structure, which is known to comprise acceptor-like trap states.[100] Under the high off-state bias, electrons are

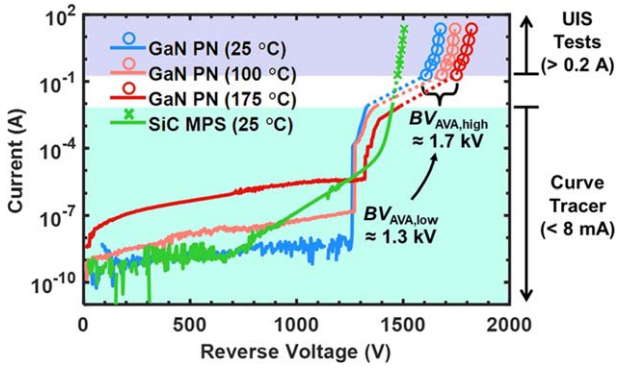

Fig. 9. (Color online) Combined *I–V* data of a GaN p-n diode from the quasi-static *I–V* sweep and UIS test, showing two breakdown processes due to the trap-filling and avalanche. "MPS" represents the merged-PN-Schottky diode, which is a reference device with near-ideal characteristics. Copyright @ 2020 IEEE. Reprinted with permission from Ref. 55.

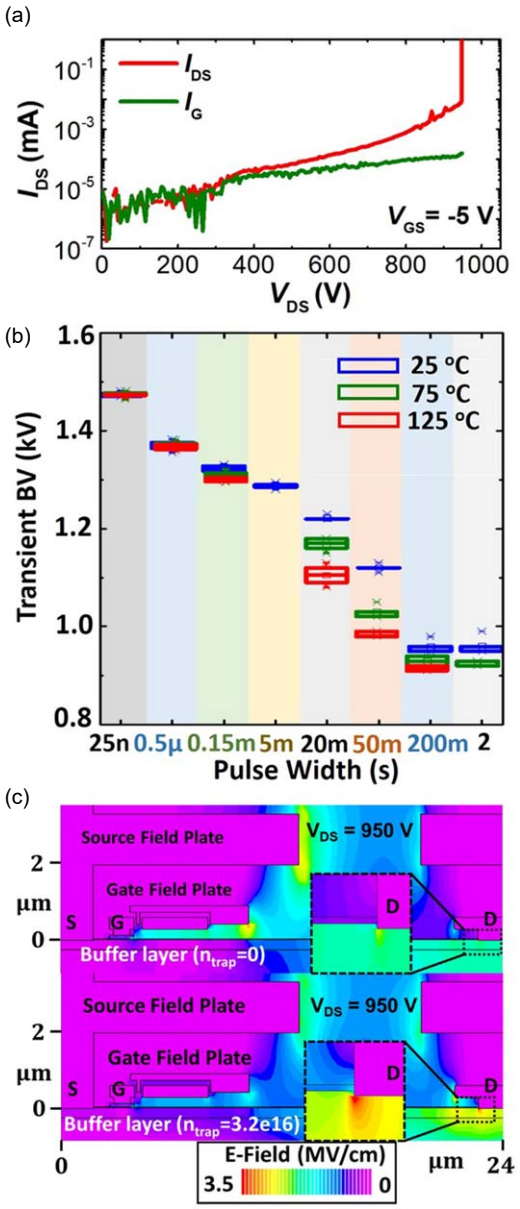

Fig. 10. (Color online) (a) Quasi-static *I–V* sweep, revealing a static BV of 950 V. (b) Dynamic BV measured as a function of pulse width and temperature. (c) Simulated E-field contour inside a GaN HEMT with minimal and full buffer trapping at 950 V, revealing an increased peak E-field near the drain with the increased buffer trapping. Copyright @ 2020 IEEE. Reprinted with permission from Ref. 75.

injected from the source or Si substrate, part of which are captured by the trapped states,[101] giving rise to net negative charges in the buffer layer, which increases the peak E-field magnitude near the drain side and lowers the device BV_{DYN} [Fig. 10(c)].[75] In quasi-static *I–V* sweep, the occupation of trap states in the buffer layer is enhanced, leading to a static BV lower than the BV_{DYN}. Similarly, in continued switching with very high f_{SW}, there is no sufficient time for de-trapping in each cycle, resulting in an accumulation of trapped charges and thus not only a lower BV_{DYN} but also an increased on-resistance.[99]

Note that the relative magnitude of the static and dynamic BV depends on the trapping under the dynamic condition and the impact of the trapped charges on the E-field distribution. In Cascode GaN HEMTs, the BV_{DYN} was found to be significantly lower than the static BV,[84] which is opposite to the case in p-gate GaN HEMTs. This phenomenon is explained by the internal Si MOSFET avalanching and the resultant hot electron injection into GaN HEMT under the dynamic switching condition.[84,85]

In addition to GaN HEMTs, a similar distinction between BV_{DYN} and static BV is also reported in devices based on various materials or architectures. In UWBG devices, a NiO/Ga_2O_3 p-n heterojunction diode with optimal edge termination exhibits a destructive BV of 1.95 kV in the static *I–V* sweep and a BV_{DYN} of 2.23 kV in the UIS test.[82] Similarly, an AlGaN/GaN Schottky diode with a resistive energy dissipation path exhibits a destructive BV of 790 V in the static *I–V* sweep and a BV_{DYN} of 1250 V in the UIS test.[87] These results show the inherent distinction of BV under static and dynamic conditions in power devices.

6. Key device design for avalanche breakdown

The learnings on many power devices such as p-n diodes, MOSFETs, IGBTs, etc. seem to consolidate that the p-n junction is the key enabling building block for the avalanche breakdown, and intuitively, the avalanche path is through the p-n junction. However, the recent study of a new GaN power transistor, the vertical GaN fin-channel JFET (Fin-JFET), suggests a need to revisit this statement. The GaN Fin-JFET consists of a plurality of submicron-meter wide, vertical n-GaN fin channels on top of an n-GaN drift region [Fig. 11(a)].[48,102] This Fin-JFET can realize the E-mode operation with a small channel resistance due to the high density of fin channels.[25] Moreover, vertical GaN FinFET shows text-book-like avalanche waveforms in the UIS tests, being the first avalanche-capable GaN power transistor.[48,102] The critical avalanche energy density is up to 10 J cm^{-2}, which is comparable to SiC devices and much higher than Si devices.[103]

The more interesting feature of the Fin-JFET breakdown is the capability of accommodating two distinct avalanche paths, which can be tuned by the gate driver. Undoubtedly, the natural avalanche path in GaN Fin-JFETs is through the gate p-n junction, producing an avalanche current flowing between the gate and drain.[48,102] However, if the gate driver is designed to turn-on the fin channel during the avalanche process, the avalanche path can be tuned to flow between the source, fin channel, and drain, due to the lower resistance of the fin channel as compared to the p-GaN gate.[103,104] This new avalanche scheme suggests that the avalanche path does not necessarily go through the p-n junction.

As compared to a conventional MOSFET driver, an *RC*-interface driver was found to lift the gate-to-source bias (V_{GS}) above the threshold voltage (V_{TH}) during the avalanche process [Fig. 11(b)].[104] As a result, the peak I. I. generation rate migrates to the foot of the n-GaN fin channel from the gate p-n junction [Fig. 11(c)].[104] The I. I. generated electrons are pushed towards the drain, while a large number of electrons are extracted from the source to recombine with the I. I. generated holes. The remaining holes are removed through the p-GaN gate. These carrier dynamics lead to an "avalanche-through-fin" process with a high electron current through the n-GaN fin channel and a small hole current through the p-GaN gate [Fig. 11(d)]. This interesting avalanche path not only obviates a large current flowing into the gate driver but also allows for spatial separation of

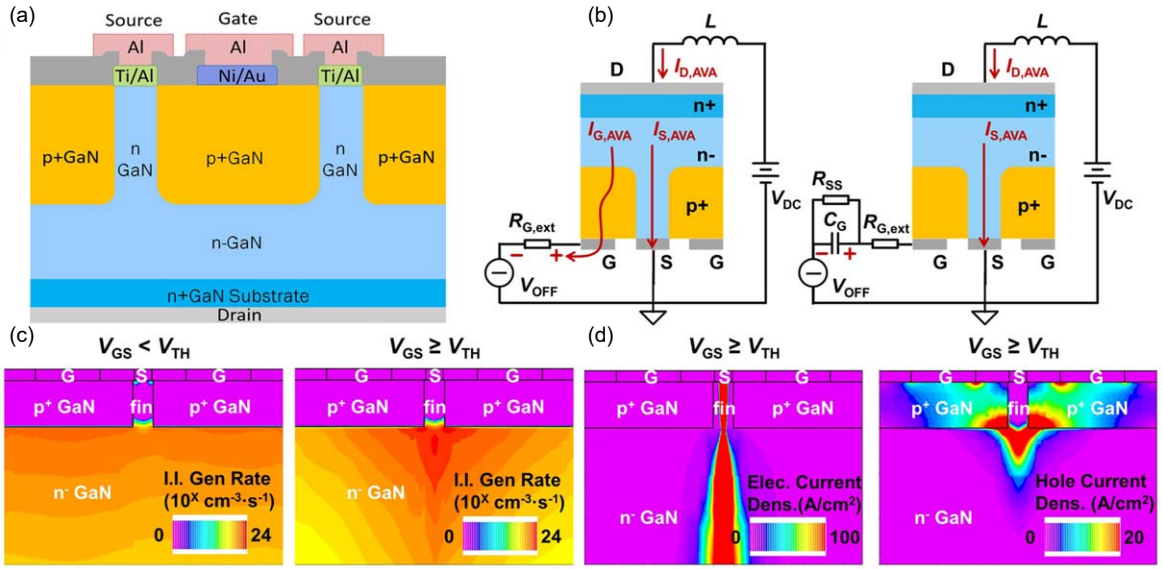

Fig. 11. (Color online) (a) Schematic of the vertical GaN Fin-JFET structure. (b) Illustration of the avalanche current path in a Fin-JFET unit-cell with a MOSFET gate driver (left) and an RC-interface driver (right). (c) The simulated contours of the I. I. generation rates under the through-gate avalanche (left) and through-fin avalanche (right). (d) The simulated contours of electron current density and hole current density under the through-fin avalanche. Copyright @ 2022 IEEE. Reprinted with permission from Ref. 104.

the locations with the peak current stress (fin channel) and the peak E-field (p-n junction), which further enables a desirable failure-to-open-circuit signature (i.e. BV_{AVA} retained after the failure in the UIS test).[103] The capability of accommodating a high channel current also produces a good short-circuit ruggedness of GaN Fin-JFETs at BV_{AVA}.[28,105,106]

The viability to accommodate two avalanche paths modulated by the gate driver is the inherent property of power JFETs and not a feature specific to GaN. By tuning the gate driver design (e.g. gate driver resistance), the avalanche path has been shown to migrate from the gate p-n junction to the source fin channel in a SiC JFET, after the gate bias exceeds the threshold voltage.[104] Even for a normally-ON SiC JFET, which has a wider channel, such transition has been demonstrated with the increased gate driver resistance.[104]

The learnings on power JFETs suggest the viability of engineering an avalanche path that detours the p-n junction and tuning the device breakdown behaviors by the gate driver design. Note that, to enable a sustained avalanche breakdown, the p-n junction may still be needed for hole removal even if the major avalanche path is elsewhere. These learnings bring new understandings on the power device breakdown and provide useful references for the "design-for-robustness" in future power devices.

7. Immediate research needs

New device structures and power semiconductors could bring new breakdown physics to power devices. With fast progress in WBG and UWBG power devices, numerous research opportunities lie in their breakdown physics and characterizations. This interdisciplinary field needs joint efforts from researchers in physics, material science, devices, circuits, and power electronics. Here we list several immediate research gaps to provoke exciting explorations in this field.

1. Recently, the non-destructive breakdown has been demonstrated in GaN HEMTs by guiding an avalanche to occur in the SiC or Si substrate[107,108] prior to the GaN HEMT breakdown. Pathways to enable the inherent avalanche in GaN HEMTs have also been proposed.[64] These works present pathways to realize the avalanche in inherently non-avalanche devices by using the device building block with lower avalanche BV. However, open questions persist on if the avalanche breakdown can be realized in non-avalanche devices like GaN HEMTs with the exploitation of their full blocking capability.
2. Heterogeneous p-n junctions have been recently applied to a few WBG/UWBG systems to address the challenges of forming native p-n junctions[10,109] or forming them in selective areas.[109–111] High-performance devices have been demonstrated on the p-NiO/n-GaN junction,[45,47,112,113] p-NiO/n-Ga_2O_3 junction,[114–118] p-GaN/n-Ga_2O_3 junction,[119,120] p-diamond/n-GaN junction,[121,122] and p-diamond/ n-Ga_2O_3 junction.[123] With various band alignments and carrier transport mechanisms, it is still unknown if heterogeneous p-n junctions can enable the avalanche capability. Addressing this gap is key to exploring pathways to make robust power devices based on semiconductors lacking intrinsic bipolar doping.
3. In addition to new materials, the viability of realizing avalanche breakdown in emerging device architectures remains a fundamental gap. Multidimensional device architectures such as superjunction and multi-channel are critical drivers for power device advancement.[1] Superjunction relies on alternative n- and p-type regions with balanced charges; it has achieved success in Si[124] and has been recently demonstrated in SiC[125] and GaN.[112] In an ideal superjuncion, the impact ionization

produced carriers will impair the charge balance, lower the BV, and induce destructive failure. By contrast, an avalanche-capable superjunction device can be realized by using unbalanced doping, which compromises device performance.[124] While avalanche is available in the Si superjunction, no avalanche breakdown has been reported in SiC and GaN superjunction, which requires future explorations.

4. In addition to non-avalanche BV, BV_{AVA} could also differ under static and dynamic conditions, i.e. the dynamic avalanche phenomenon.[73] This phenomenon is related to the internal plasma of free carriers with high concentration and thus only present in bipolar devices, such as bipolar diodes, thyristors, and IGBTs. This dynamic avalanche occurs at a voltage much lower than the static BV_{AVA} and could lead to the formation of high-current filaments, which could be destructive. The physics and prevention of dynamic avalanche have been extensively studied in high-voltage, bipolar Si devices.[73,126,127] Whereas, the dynamic avalanche has not been experimentally studied in WBG and UWBG devices. This is partly because WBG and UWBG devices have pushed the voltage boundary of unipolar devices to at least 10 kV.[16–18,128] With the advent of future WBG/UWBG bipolar devices, e.g. 15–27 kV SiC bipolar diodes,[129] dynamic avalanche is believed to be an important yet unexplored research topic.
5. The implanted, deep trap-based edge termination is recently deployed for device edge termination.[38,98,130–133] While the trap-filling process is known to govern the breakdown behaviors of these termination structures, their dynamic BV and the ruggedness under the repetitive overvoltage switching remain unknown. Intuitively, we envision two basic requirements of the trap-based edge termination for the device's stable operation in converters: (1) the trap ionization speed should be fast enough to ensure that the edge termination is functional in the fast-switching transient, which is a prerequisite for making BV_{DYN} not smaller than the static BV (otherwise, the device needs to be de-rated); (2) the device blocking voltage in converter applications should be much smaller than the one rendering the trap's full filling in the edge termination, as otherwise, high leakage current and BV instability would be expected. In addition to the viability of the edge termination's functionality under fast-switching transient, it is also unclear if these implanted structures can maintain the blocking capability after the repetitive trap-filling.
6. From the BV characterization standpoint, the on-wafer setup to directly characterize the BV_{DYN} for bare-die devices is highly desirable. Most of the current circuits for BV_{DYN} characterization have been applied to packaged devices. We do not see fundamental roadblocks to developing such setups for on-wafer characterization, which could bring much higher flexibility and enable a fast cycle to directly probe the BV_{DYN}'s relation with specific device designs and processing steps. In addition, the on-wafer test platform could allow for the study of BV_{DYN} of devices with various breakdown mechanisms, such as punch-through, percolation, etc., which are largely unexplored in the literature.

8. Summary

This paper reviews recent understandings of the avalanche and non-avalanche breakdown mechanisms and emphasizes the distinction between static and dynamic BV. Various BV characterization methods, including the static and pulse *I–V* sweep as well as the circuit methods are comparatively introduced. The device physics behind the time- and frequency-dependent BV as well as the enabling device structures for avalanche breakdown are also discussed. Most of these learnings are material agnostic and applicable to power devices based on various WBG and UWBG semiconductors. The key takeaways include:

1. The realization of avalanche breakdown hinges on not only the I. I. and multiplication but also the effective removal of the generated carriers from the device structure.
2. The BV_{DYN} of non-avalanche devices can be quite different from the static BV, and BV_{DYN} could be dependent on pulse width and frequency in power switching.
3. The UIS, CIS, and ACC circuits are useful tools to characterize the BV_{DYN} in soft and hard switching and identify the device's true overvoltage margin in applications.
4. In the sweep, the device's avalanche capability could be blinded by the premature trap-filling process; the UIS circuit can test the device's true avalanche capability.
5. Distinct device avalanche paths can be tuned by the gate driver. The avalanche can detour the p-n junction, while the p-n junction may still be essential for hole removal.

Acknowledgments

The authors acknowledge the funding support from the National Science Foundation Grants ECCS-2036740, ECCS-2202620, ECCS-2100504, and ECCS-2045001 as well as the CPES Industry Consortium at Virginia Tech. We greatly appreciate the continued collaboration with Prof. Florin Udrea, Prof. Wataru Saito, and Prof. Qiang Li as well as NexGen Power Systems.

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