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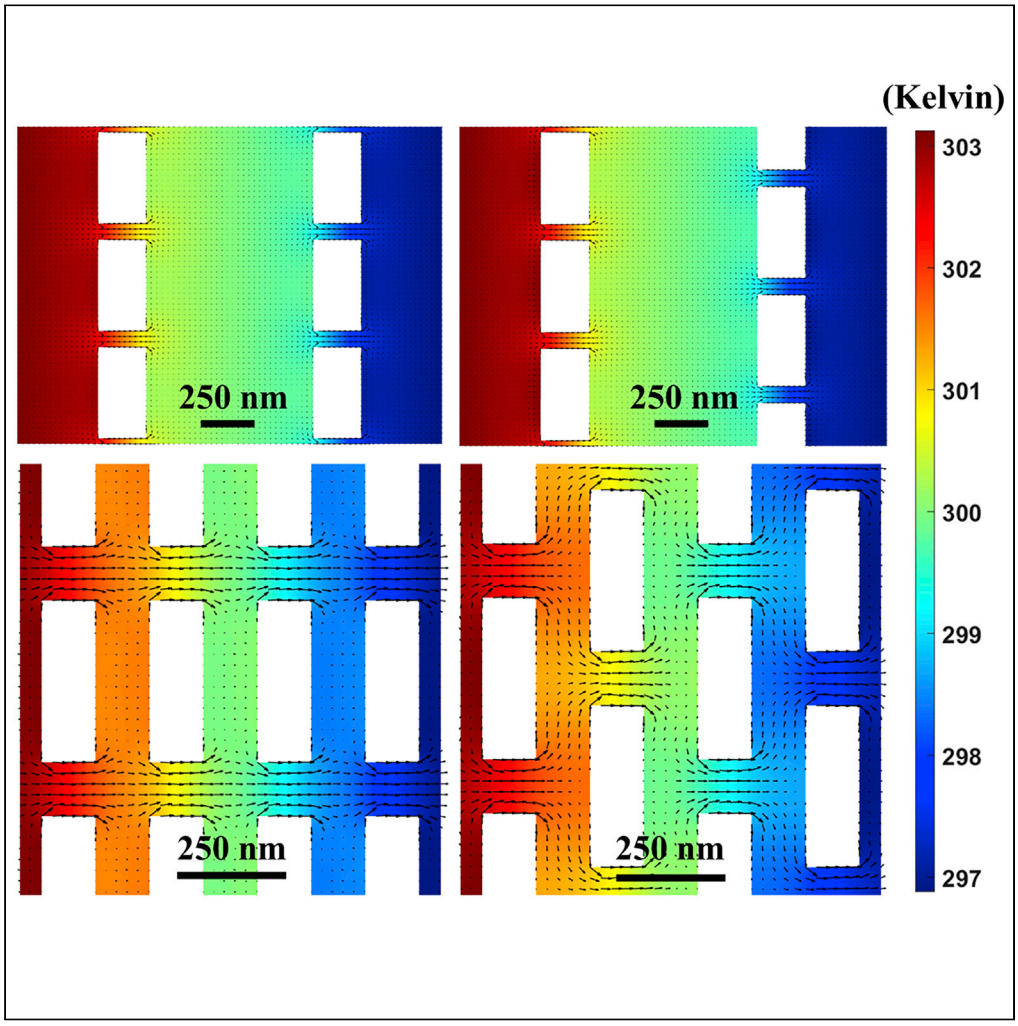

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Highlights

Offset nanoslot patterns to minimize the in-plane thermal conductivity of thin films

Ion implantation to further reduce the thermal conductivity

Redistributed heat fluxes revealed by phonon Monte Carlo simulations

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Engineering thermal transport within Si thin films: The impact of nanoslot alignment and ion implantation

Sien Wang,[1] Yue Xiao,[1] Qiyu Chen,[1] and Qing Hao[1,2,*]

SUMMARY

In recent years, nanoporous Si films have been intensively studied for their potential applications in thermoelectrics and the thermal management of devices. To minimize the thermal conductivity, ultrafine nanoporous patterns are required but the smallest structure size is largely limited by the spatial resolution of the employed nanofabrication techniques. Along this line, an effectively smaller characteristic length of a nanoporous film can be achieved with offset nanoslot patterns. Compared with periodic circular pores, the nanoslot pattern can achieve an even lower thermal conductivity, where a much smaller porosity is required using ultra-narrow nanoslots. The obtained low thermal conductivity can be understood from the thermally dead volume revealed by phonon Monte Carlo simulations. To further minimize the contribution from short-wavelength phonons, an additional 25% thermal conductivity reduction can be achieved with Ga ions implanted using a focused ion beam.

INTRODUCTION

Better understanding and then "taming" the thermal transport inside various materials and devices are critical to many applications, including thermoelectric (TE) energy conversion (Shi et al., 2020), cooling of power electronic devices (Hao et al., 2018c; Won et al., 2013), and heat guide (Anufriev et al., 2017; Xiao et al., 2021). Among these, TE materials have a great potential in various energy harvesting and refrigeration applications (Shi et al., 2020). Currently, TE power generators have been developed to produce electricity from the waste heat in the car exhaust gas (Yang and Stabler, 2009) or from solar-radiation heat as a cheap alternative to solar cells (Kraemer et al., 2011). The effectiveness of a TE material is indicated by its dimensionless TE figure of merit, defined as $ZT = S^2\sigma T/k$, where S is the Seebeck coefficient, σ is the electrical conductivity, k is the thermal conductivity, and T is the absolute temperature. Here the thermal conductivity k can be split into the lattice (phonon) contribution k_L and the electronic contribution k_E. In practice, it has been a challenge to achieve both a low k and a high $S^2\sigma$ within the same material (Slack, 1995). After decades of research, there are still very limited choices for high-performance and abundant TE materials. This material restriction can now be opened up by decoupling the electron and phonon transport using multi-length scale structures (Biswas et al., 2012; Bux et al., 2009; Lan et al., 2009; Poudel et al., 2008). The structures introduced into the materials include point defects such as alloy atoms (Wood, 1988), embedded nanostructures, and nano- to micro-grain boundaries (Hao and Garg, 2021; Vineis et al., 2010; Wan et al., 2010). These structures can minimize the k_L across the whole phonon spectrum, while maintaining bulk-like electrical properties. Following this, a high ZT can be potentially achieved in a variety of unconventional materials with a large power factor $S^2\sigma$, particularly those made of low-cost, abundant, and nontoxic elements. One notable example can be nanostructured bulk silicon (Si) as cost-effective TE materials (Bux et al., 2009; Hao et al., 2010; Kashiwagi et al., 2019).

Considering the difficulty in exactly controlling the nanostructures within a synthesized bulk material, fabricated nanoporous thin films (Hao and Xiao, 2020; Hao et al., 2018a; Lee et al., 2017; Lim et al., 2016; Marconnet et al., 2012; Tang et al., 2010; Yu et al., 2010) and graphene (Gunst et al., 2011; Oh et al., 2017; Xu et al., 2019) have been intensively studied to demonstrate the ZT improvement with the nanostructuring approach. Tremendous attention has been paid to nanoporous Si thin films that can be directly used for the thermal management of semiconductor devices. In such films, diffuse nanopore-edge scattering of phonons is usually dominant and k_L can be reduced by classical phonon size effects, whereas wave effects

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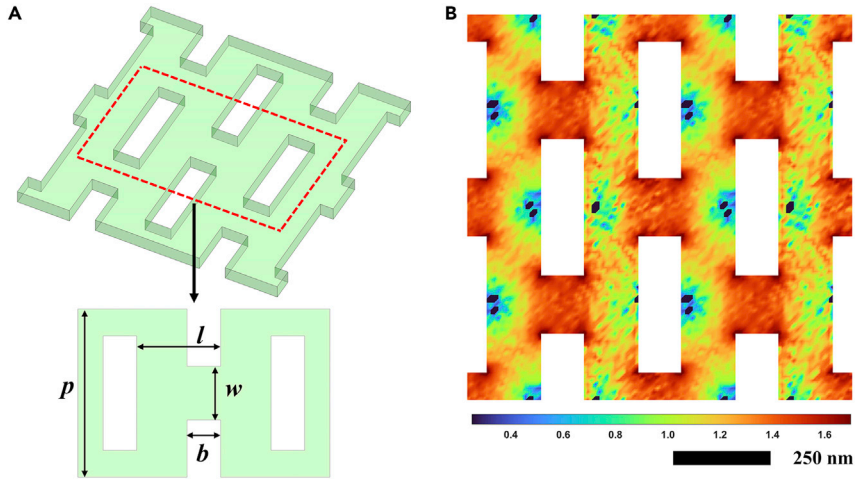

Figure 1. Demonstration of a nanoporous thin film with offset nanoslots

(A) Offset nanoslots patterned across a thin film. The geometry parameters are defined in the inset.

(B) Heat flux intensity map of a typical offset pattern, with overall heat flowing from the left end to the right end. The magnitude of the heat flux is taken as common logarithm in the plot.

may become important at ~10 K or below (Graczykowski et al., 2017; Lee et al., 2017; Maire et al., 2017; Nomura et al., 2022; Wagner et al., 2016; Xiao et al., 2019). Following the Matthiessen's rule, nanopores can modify the phonon mean free paths (MFPs) with a characteristic length (L_C) (Hao et al., 2016a; Xiao et al., 2019). To maximize the ZT, this L_C should be longer than majority electron MFPs but shorter than majority phonon MFPs (Hao et al., 2016b). In a similar case for nanocrystalline materials, L_C becomes the grain size and the recommended L_C value is 20 nm for Si at a carrier concentration of 1×10^{19} cm^{-3} (Qiu et al., 2015). In practice, challenges exist in achieving such a small L_C in bulk materials due to significant grain growth during the hot press (Lan et al., 2009). For thin films, the effective L_C can be estimated with the radiative mean beam length (MBL) for optically thin samples, defined as $MBL = 4V_{solid}/A_{pore}$ (Hao et al., 2016a, 2017a). Here, V_{solid} is the solid region volume and A_{pore} is the pore surface area. For aligned circular through-film pores, the recommended L_C = 20 nm requires a pore diameter of 6.77 nm with a typical 25% porosity. In nanofabrication, such sub-10 nm patterns can be defined with electron beam lithography (EBL) but the actual pore diameter d is often restricted by the film thickness t and aspect ratio of dry etching, i.e., $d > t/3$ (Marconnet et al., 2013). Further reducing the nanopore size and spacing may also lead to the degradation of the mechanical strength (Winter et al., 2017). Keeping this in mind, the nanoporous patterns should be optimized to minimize the effective L_C (Romano and Grossman, 2014). Among various patterns, long and narrow rectangular nanopores (i.e., nanoslots) exhibit great potentials in thermal designs, i.e., a smaller neck width w between adjacent nanoslots to yield a smaller L_C (Hao and Xiao, 2020; Hao et al., 2019). This L_C can be further reduced by offsetting adjacent rows of nanoslots (Figure 1A), which also adjusts the in-plane thermal anisotropy of a thin film (Xiao and Hao, 2021). Perpendicular to the overall heat flow direction, the pitch p is fixed at 500 nm for all devices. The dimensions for a device can be uniquely described with (l, b, w) in Figure 1A. In general, nanoslot offsets can vary from zero (i.e., aligned nanoslots) to half of the pitch p (i.e., staggered nanoslots). In this work, the focus is on staggered nanoslots to minimize the in-plane thermal conductivity perpendicular to nanoslot rows. For circular, square, and rectangular nanopores, comparisons between aligned and staggered patterns can be found (Huang et al., 2017; Romano and Kolpak, 2017; Song and Chen, 2004; Tang et al., 2013; Verdier et al., 2017). The use of nanoslots also introduces a "thermally dead volume" with little contribution to heat transfer, as found in similar structures such as nanoladders (Park et al., 2018) and fishbone-like structures (Maire et al., 2018; Yang et al., 2019b). Such a thermally dead volume can also be revealed by the simulated heat flux distribution within the structure, which can be obtained by solving the phonon Boltzmann transport equation (BTE). With a similar thermally dead volume, zigzag Si nanowires exhibited a k_L reduction compared with the straight Si nanowire (Anufriev et al., 2019; Heron et al., 2010; Yang et al., 2019a; Zhao et al., 2019). The reduction ranges from ~5% to 25% at the room temperature and is up to 50% at 25 K (Yang et al., 2019a; Zhao et al., 2019). In a separate study, no k_L suppression was observed above 150 K due to the relatively large structure size compared with the phonon MPFs (Anufriev et al., 2019). Following this, heat transfer is mainly

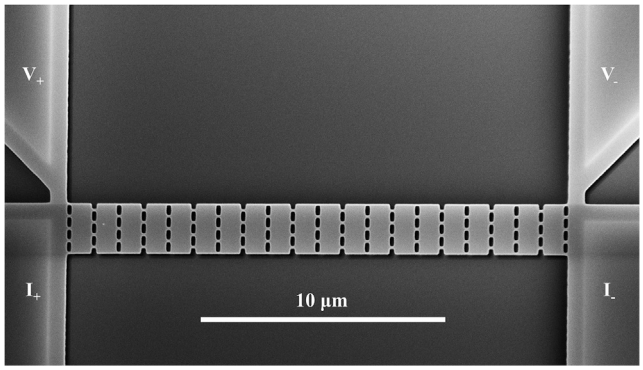

Figure 2. SEM image of a Si thin film with offset nanoslot (sample 1o)
Terminals for the 4-probe measurement are labeled.

along a zigzag path across offset nanoslots (Figure 1B) to achieve a similar k_L reduction. Compared with individual zigzag nanowires, a nanoporous film can transport significantly more heat and electrical currents, along with advantages in the device fabrication.

In addition to the nanoporous pattern variation, ion implantation by a focused ion beam (FIB) may also be used as an effective method to locally decrease the k_L. Such ion implantation can introduce point defects such as silicon vacancies and interstitials (Lim et al., 2016). For ion irradiation with sufficient energy and/or beyond a threshold dose, amorphization can also be observed to lower the k_L (Scott et al., 2020; Tamura et al., 1986; Xiao et al., 2020; Zhao et al., 2017). For the doping purpose, an one order of magnitude reduction in the k was reported for 100-nm diameter ZnO nanowires with implanted gallium ions (Ga^+), with a simultaneous one order of magnitude increase in the σ (Xia et al., 2014). The local k value along a single Si nanowire was tuned with selective helium ion irradiation (Zhao et al., 2017). For a single-crystal Si substrate, doses of 10^{12} to 10^{18} Ga^+/cm^2 led to amorphization within the top surface layer with a typically <70 nm thickness. The lowest out-of-plane k was about 1 W/m•K at a dose of roughly 10^{16} Ga^+/cm^2 for the irradiated Si volume (Alaie et al., 2018). In practice, ion implantation was used to dope nanoporous Si films, and further k reduction was found (Lim et al., 2016).

In this work, the in-plane k of Si thin films with varied nanoslot patterns was systematically studied. Figure 2 shows a typical device used for 3ω measurements. The typical data analysis to extract the k value is presented in Figure 3. The detailed dimensions for all fabricated samples are summarized in Table 1.

The aligned nanoslot patterns can be cut into fishbone nanowires or nanoladders as a strip along the heat conduction direction (Hao and Xiao, 2020). More controls of the in-plane k are achieved by changing the nanoslot alignment. An up to 33.7% k reduction from aligned to offset nanoslot patterns was found at 125 K, which was comparable to the 34% k reduction from straight to zigzag nanowires at 75 K (Yang et al., 2019a). The experimental result was consistent with phonon Monte Carlo (MC) simulations. When Ga^+ ions were implanted with an FIB, the k was further decreased by 25% for one heavily doped sample. By minimizing the energy for ion irradiation, no amorphization was found in transmission electron microscopy (TEM) studies on ion-implanted thin films. These implanted ions simply function as point defects to dramatically scatter short-wavelength phonons. The finding here shows the potential of combining nanofabrication and ion implantation to locally tune the in-plane thermal conductivity of a thin film or atomic-thick material.

RESULTS AND DISCUSSION

Phonon MFP distributions and heat flux maps

Phonon MC simulations were used to compute the k_L of nanoporous thin films, along with the temperature and heat flux profiles under an applied temperature difference. Figure 4 presents the accumulated in-plane k_L as a function of the in-plane phonon MFP (Λ_{in}) (Hao et al., 2019, 2020) for a 70-nm-thick solid film at 300 K, where 67% of the k_L is contributed by phonons with Λ_{in} less than 100 nm. This Λ_{in} is modified from the bulk phonon MFP (Λ_{Bulk}) using the Fuchs-Sondheimer model (Chen, 2005) to incorporate the influence of possibly diffusive phonon scattering at the top/bottom film surfaces, given as

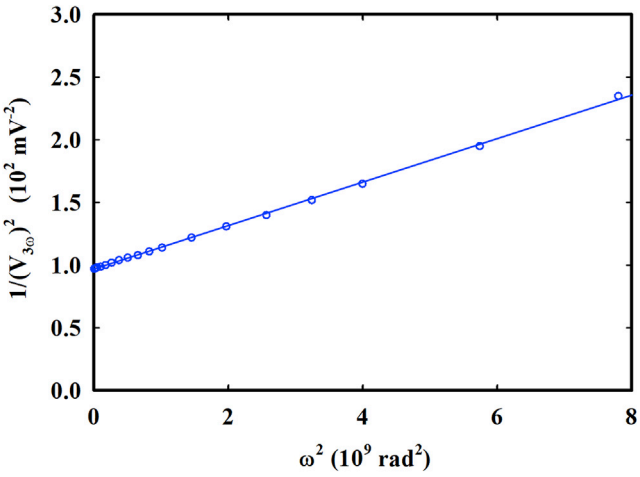

Figure 3. 3 ω voltage of Sample 1a at 300 K

Circles are experimental data, and the solid curve is the fitting of the experimental data with Equation 3.

$$\frac{\Lambda_{in}}{\Lambda_{Bulk}} = 1 - \frac{3[1 - P(\lambda)]\Lambda_{Bulk}}{2h}\int_0^1 (x - x^3)\frac{1 - \exp\left(-\frac{h}{\Lambda_{Bulk}x}\right)}{1 - P(\lambda)\exp\left(-\frac{h}{\Lambda_{Bulk}x}\right)}dx \qquad \text{(Equation 1)}$$

where λ is the phonon wavelength, and $P(\lambda)$ is the specularity of film-surface phonon reflection for a film with its thickness h. For our measured temperature range, completely diffusive film-surface phonon scattering can be assumed, i.e., $P(\lambda) \approx 0$. The computed Λ_{in} distribution can be used to compute the in-plane thermal conductivity of thin-film-based nanostructures, such as etched nanowires and nanoporous thin films (Hao et al., 2020). For the 70 nm film thickness, our calculated Λ_{in} distribution is similar to the Λ_{in} distribution computed based on first-principles (first P) Λ_{Bulk} given by Esfarjani et al. (2011) but the temperature-dependent phonon MFPs are not available for first P calculations. In our previous study, a good agreement was found between temperature-dependent measurements on nanoporous Si thin films and phonon MC simulations using fitted phonon MFPs by Wang et al. (2011). The phonon MFPs for a 100-nm-thick Si film were also predicted by Malhotra and Maldovan using a Boltzmann-transport-based reduced MFP model (Malhotra and Maldovan, 2016). In comparison, the Λ_{Bulk} distribution given in a separate study (Jain et al., 2013) was converted into the Λ_{in} distribution for a 70-nm-thick thin film. For a 145 nm film thickness, Anufriev et al. reconstructed the phonon MFPs from the measured in-plane k of Si films with nanoslits of various aperture sizes (Anufriev et al., 2020).

In practice, the phonon MFP distribution can be used to guide the thermal designs of nanoslot patterns. When the $(l - b)$ value in Figure 1A is much longer than majority phonon Λ_{in} values, little k_L difference

Table 1. Critical dimensions for four groups of nanoslot-patterned Si thin films

Sample index	l (nm)	p (nm)	b (nm)	w (nm)
1a	1000	500	200	80
1o				
2a	500	500	200	80
2o				
3a	250	500	100	160
3o				
4o	1000	500	120	160
4o+				
4o++				

The definition of geometry parameters (pitches l and p, depth b, and neck width w) is given in Figure 1. The subscript "a" stands for aligned nanoslots and "o" stands for offset nanoslots. Samples 4o+ and 4o++ are further implanted with Ga^+ ions with a nominal dose of 2.1×10^{15} cm^{-2} and 2.1×10^{16} cm^{-2}, respectively.

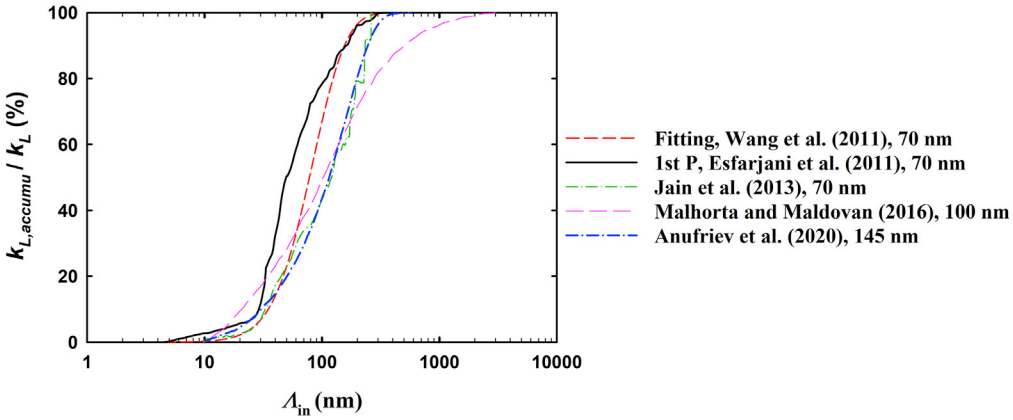

Figure 4. Room temperature phonon MFP distributions for the in-plane heat conduction along a 70-nm-thick Si thin film

The red dashed line is computed with the fitted bulk phonon MFPs by Wang et al. (Wang et al., 2011), and the black solid line is based on first P calculations by Esfarjani et al. (Esfarjani et al., 2011). The compared room temperature MFP distributions are predicted for 100-nm-thick Si thin films (Malhotra and Maldovan, 2016), predicted for a 70-nm-thick Si thin film using bulk-Si phonon MFPs given by Jain et al. (Jain et al., 2013), and measured for 145-nm-thick Si films (Anufriev et al., 2019).

can be found between aligned [Figure 5A for Sample 1a (1000,200,80)] and offset [Figure 5B for Sample 1o (1000,200,80)] nanoslot patterns. In this situation, phonons coming out of the neck region can spread out in the middle of the solid region and then converge at the entrance of the following neck. The thermal resistance of the entire structure can be largely attributed to the ballistic thermal resistance for phonons passing through the mostly "isolated" narrow necks between adjacent nanoslots (Hao et al., 2019; Prasher, 2005). The nanoslot alignment has limited influence here. In contrast, clearly defined heat transfer "channels" can be found when the $(l - b)$ value is comparable to or smaller than majority phonon Λ_{in} values (Figures 5C and 5D). For Sample 3a (250,100,160) (Figure 5C), heat flow is mostly along straight channels similar to parallel nanowires, as suggested in one previous study on nanoporous Si films (Yu et al., 2010). The interconnecting parts between channels are thermally inactive for most of their volume. When the nanoslots are offset [Figure 5D for Sample 3o (250,100,160)], phonons are enforced to flow along a zigzag path with larger thermal resistance than that for straight channels in Figure 5C.

Temperature-dependent k_L measured for varied nanoslot patterns

The device layer of an SOI wafer has a low electrical conductivity σ = 5–100 S/m so that $k \approx k_L$ can be approximated. The measured in-plane k_L with different nanoslot arrangements at different temperatures are plotted as symbols in Figure 6. The maximum temperature rise in the self-heating 3ω measurements is generally controlled within 5 K to avoid the uncertainty in the sample temperature.

Consistent with simulation results in Figure 5, the measured k_L values show small difference between Sample 1a (1000,200,80) and Sample 1o (1000,200,80) (red symbols in Figure 6) with l-$b \approx$ 800 nm. For samples in Group 2 (500,200,80) (green symbols), a reduced $l - b \approx$ 300 nm yields a ~7.3% reduction in k_L at room temperature and a 11.7% reduction at 83 K by offsetting the nanoslots. In Group 3 (250,100,160) with l–$b \approx$ 150 nm (blue symbols), a 30.2% k_L reduction at room temperature and 33.7% at 125 K is observed for the offset nanoslot pattern. In this situation, phonons are enforced to travel along interconnected nanowires and experience more phonon boundary scattering at nanoslot edges.

The suppression factor, defined as $\mathcal{R} = 1 - (k_{L,O}/k_{L,A})$, is used to quantify the impact of the nanoslot offset (Figure 7). Due to the increased Λ_{in} at decreased temperatures, the suppression effect becomes stronger for Groups 2 (500,200,80) and 3 (250,100,160) at cryogenic temperatures.

Figure 8 shows the correlation between l and $\mathcal{R}$, with a fixed p = 500 nm. Based on phonon MC simulations (solid curves), $\mathcal{R}$ increases rapidly when l is decreased below 300 nm. An over 90% suppression is found for l–b = 20 nm, which can largely benefit thermoelectric applications. The $\mathcal{R}$ for square nanopores (Tang et al.,

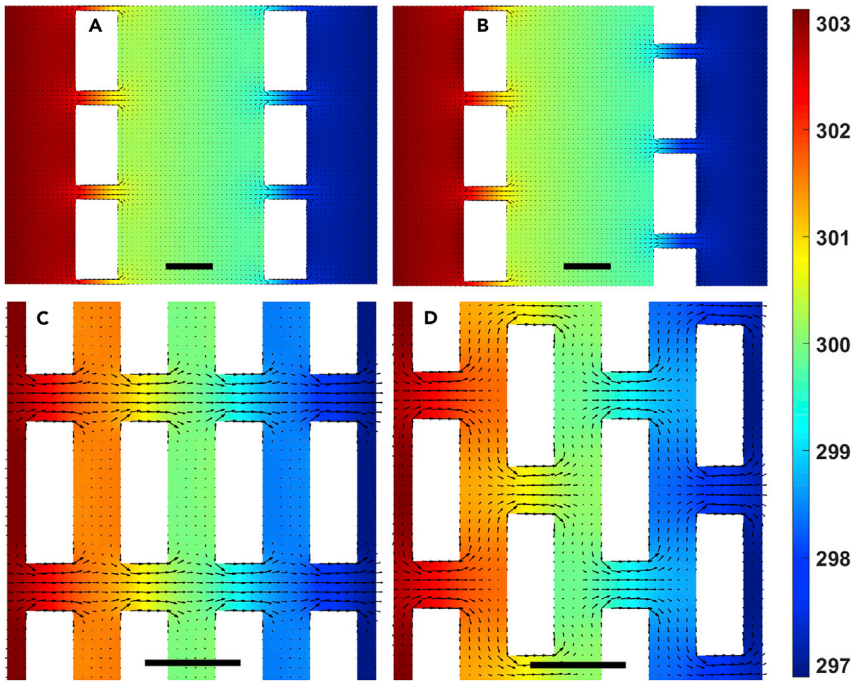

Figure 5. Simulated temperature profiles (in Kelvin)
The arrows are the local heat flux. Scale bars are 250 nm.
(A) Temperature profile for Sample 1a (1000,200,80).
(B) Temperature profile for Sample 1o (1000,200,80).
(C) Temperature profile for Sample 3a (250,100,160).
(D) Temperature profile for Sample 3o (250,100,160).

2013), circular nanopores (Verdier et al., 2017), and segmented silicon nanowires (NWs) (Anufriev et al., 2019) are also added in comparison. In addition, Gluchko et al. also studied the packman-shaped nanopores (Gluchko et al., 2019). The staggered pattern led to a $\mathcal{R}$ of 17% at 4 K.

Impact of crystal defects induced by ion implantation

Temperature-dependent k_L for ion-implanted samples was also measured as Group 4 (1000,120,160) (Figure 6). Compared with Sample 4o without ion implantation, the room temperature k_L is reduced by 10.8% and 20.0% for Sample 4o+ and Sample 4o++, respectively. The reduction factors further increase to 13.9%

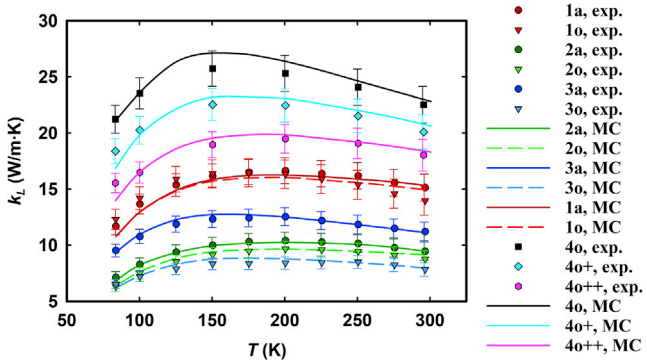

Figure 6. Temperature-dependent k_L for different nanoslot-patterned Si thin films
The geometry for each sample is listed in Table 1. Symbols are experiment (exp.) data from the 3ω measurements and curves are predictions from the phonon MC simulation. Error bars are estimated for the 95% confidence interval.

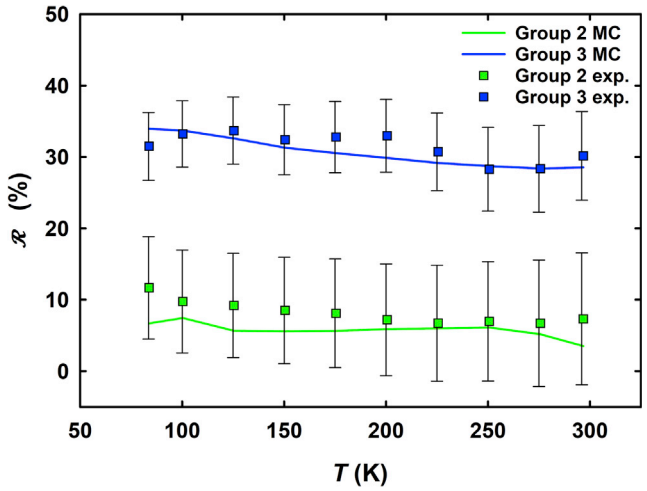

Figure 7. Temperature-dependent suppression factors for two groups of nanoslot patterns. Error bars are estimated for the 95% confidence interval.

and 30.0% at 100 K. In phonon MC simulations, the scattering coefficient A_1 for point-defect scattering is increased to match the experimental data. Here $A_1 = 1.69\times10^{-45}$ s^3 for the undoped Si was increased to 8.00×10^{-45} s^3 and 1.80×10^{-44} s^3 for Samples 4o+ and 4o++, respectively.

For ion implantation studies, solid Si thin films were released from the SOI and transferred onto TEM grids. The detailed wet transfer process was similar to those used in the film-wafer bonding (Wang et al., 2020). The ion implantation condition followed that for measured nanoporous samples. As shown by the electron backscatter diffraction (EBSD) patterns and TEM images (Figures 10A and 10B), the 70-nm-thick Si film maintained a high crystal quality under the nominal dose of 2.1×10^{15} cm^{-2} and 2.1×10^{16} cm^{-2}. The minimized structure damage is mostly attributed to the employed low ion implantation voltage and is critical to doping applications (Xia et al., 2014). The Ga concentration is further measured with energy-dispersive X-ray spectroscopy (EDS). Figure 9C shows a typical EDS spectrum taken from a region with a 2.1×10^{16} cm^{-2} nominal dose. In addition to Si and Ga atoms, O with an atomic percentage (at%) of 1.9–4.7 at% was found but no C contamination was detected. Detailed Ga concentration for each implantation dose is listed in Table 2. Due to the low acceleration voltage, 45%–50% of the irradiated Ga^+ were captured by the thin film instead of penetrating the film. A similarly high Ga at% was observed by Roediger et al. (2011). For ion implantation, it should be noted that more Ga atoms should be found on the top part of

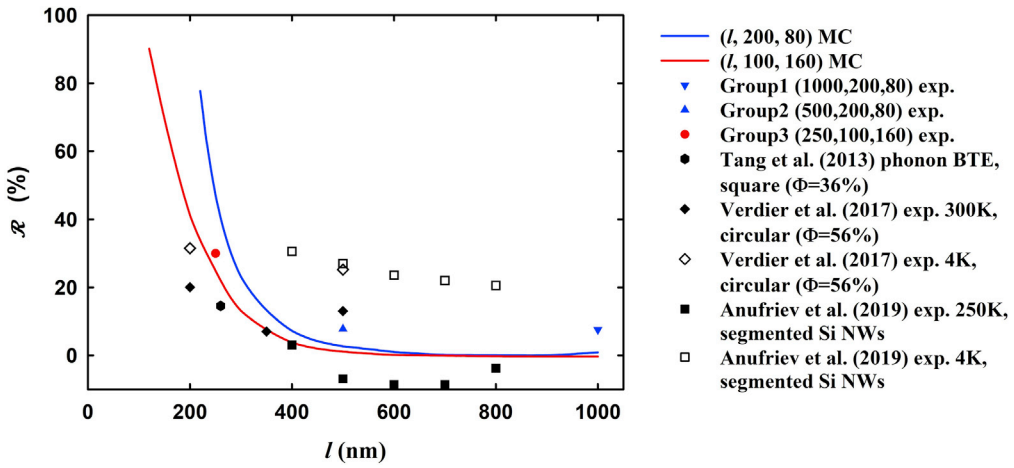

Figure 8. Suppression factors for nanoporous Si thin films with various pore designs
The (*l*, *b*, *w*) values are indicated in the legend.

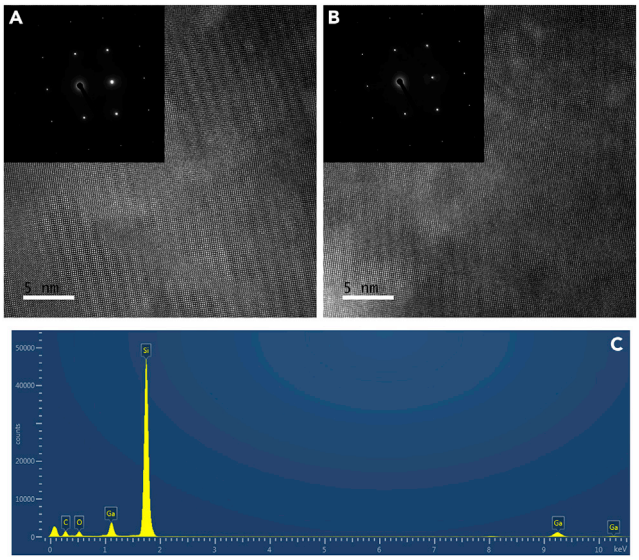

Figure 9. Electron microscopy results for ion-implanted samples

(A) TEM images of the Si thin film with a nominal Ga^+ dose of 2.1×10^{15} cm^{-2}. Inset is the SAED taken from the region. The scale bar is 5 nm for the TEM image.

(B) TEM images of the Si thin film with a nominal Ga^+ dose of 2.1×10^{16} cm^{-2}. Inset is the SAED taken from the region. The scale bar is 5 nm.

(C) EDS spectrum from the Si thin film with a nominal implanted Ga dose of 2.1×10^{16} cm^{-2}.

a thin film. As a simple way to match the experimental data, the phonon MC simulations are thus focused on an effective A_1 value across the whole film thickness.

With a high Ga^+ dose of 2.1×10^{17} cm^{-2}, Ga precipitation was observed (Figure 10). Polycrystalline Ga clusters were found across the Si thin film. When the same dose was applied to a suspended nanoporous Si thin

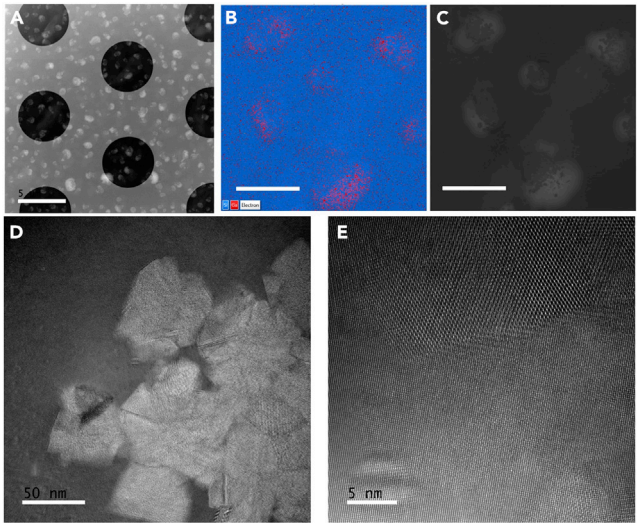

Figure 10. Electron microscopy results for the sample with a Ga^+ dose of 2.1×10^{17} cm^{-2}

(A) STEM image of Ga precipitation on the 70-nm-thick Si film (2.1×10^{17} cm^{-2} dose) supported by a holey TEM grid. The scale bar is 5 μm. The dark circular regions are the suspended part of the 70-nm-thick Si film on the TEM grid.

(B) EDS mapping of Ga clusters across the Si thin film. The scale bar is 1 μm.

(C) Corresponding secondary electron image for the EDS mapping in (b). The scale bar is 1 μm.

(D) TEM image of one polycrystalline Ga cluster. The scale bar is 50 nm.

(E) TEM image of the interface between crystalline Si and crystalline Ga. The scale bar is 5 nm.

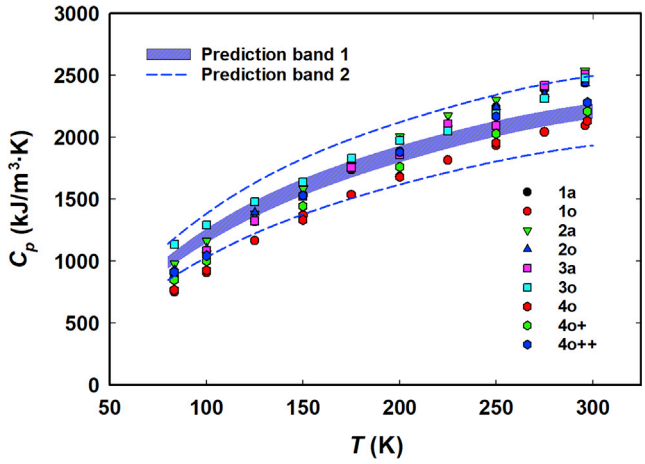

Figure 11. Measured solid C_p for nanoporous thin films

The predicted range is based on the bulk material properties of the metal-coated film. Prediction band 1 considers the uncertainty of the film thickness (± 5 nm for Si, ± 2 nm for Cr, and ± 4 nm for Pt). Prediction band 2 further considers the uncertainty of porosity measurements (± 10%) in addition to the thickness uncertainty.

film, the suspended part warped due to the significant heating effect from bombarded ions. The k_L of the nanoporous thin film cannot be measured for this dose.

Temperature-dependent C_p

Within periodic nanoporous films, the phonon wave effect (Maldovan, 2015) may play an important role in the k_L reduction. There are several experimental methods to justify the importance of the wave effect, such as comparing the k_L of periodic and aperiodic nanoporous thin films (Lee et al., 2017; Maire et al., 2017; Wagner et al., 2016), comparing the C_p of nanoporous thin films with the bulk value (Hao et al., 2018b), and measuring the thermal resistance of nanoporous thin films with added periodic nanopores (Xiao et al., 2020). To compare C_p values, all measured C_p values are divided by $(1-\Phi)$ to yield the solid C_p. The porosity Φ is estimated based on the sample geometry but errors may occur due to tapered sidewalls for dry-etched nanopores (Hao et al., 2018a). Considering the thickness variation for each material layer and 10% error in estimated Φ, all solid C_p values are within the range for the predictions using bulk specific heat values (Figure 11). This result suggests negligible influence of the wave effect for the measured temperature range. It should also be noted that the ion implantation did not significantly affect the C_p value. In practice, doping heavy atoms to the material (i.e., increased mean atomic mass) has been widely used to reduce the k by decreasing the phonon group velocity (Kargar et al., 2018; Pei et al., 2012; Winter and Clarke, 2007). Based on measured C_p values, the phonon dispersion modification cannot be remarkable with implanted Ga^+ ions here.

Conclusions

In this work, nanoslot alignment and ion implantation are explored for their potential applications in reducing the k_L of Si thin films. Without changing the feature size and porosity, a 33.7% k_L reduction at 125 K can be achieved simply by offsetting nanoslots. This nanoporous structure can be easily implemented in thin films and atomic-thick materials to tune the thermal transport. For aligned periodic nanoslots, the characteristic length can be approximated as $L_c \approx 3wl/4H_w(p-w)$, where H_w is the correction factor to

Table 2. Parameters and results for ion implantation studies. The Ga at% is measured with EDS

Sample index	Nominal dose (cm^{-2})	Ga at%	$k_L/k_{L,undoped}$ at 300 K
4o (1000,120,160)	0	0.0	100%
4o+	2.1×10^{15}	0.3	89.2%
4o++	2.1×10^{16}	2.7	80.0%

account for the reduced thermal conductance due to decreased cross-section for heat conduction inside a porous structure (Hao and Xiao, 2020). For thermoelectrics, the recommended $L_c \approx 20$ nm for heavily doped Si (Qiu et al., 2015) can be achieved by patterning aligned nanoslots with $l = 60$ nm, $b = 10$ nm, $w = 13$ nm, and $p = 120$ nm. The dimensions here are much larger than the aforementioned pore diameter of 6.77 nm for periodic circular pores with a 25% porosity. Following this, offset nanoslots can provide a comparable L_c value with even larger feature sizes and thus minimize the challenges in nanofabrication. The alignment modification can also be applied to three-dimensional nanoporous structures (Ma et al., 2016; Yang et al., 2014) when classical phonon size effects are dominant. Along another line, the low-energy ion implantation introduced with an FIB did not damage the overall lattice structure but created local defects to suppress the phonon transport, which can be combined with nanoporous patterns to minimize the k_L but still maintain bulk-like electrical properties. Attention should also be paid to charge carriers trapped by pore-edge defects. The charge carrier depletion near pore edges may largely reduce the carrier concentration (Tang et al., 2010). A potential field can build up to further scatter electrons and holes within the pore-edge depletion region (Hao and Xiao, 2019; Hao et al., 2017b), which also affects the electrical properties.

Limitations of the study

This study focuses on suppressing the phonon transport inside Si thin films. In principle, the method (i.e., well-designed nanoporous patterns and ion implantation) could be extended to other thin films and atomic-thick materials to locally tune the thermal properties. For thermoelectric applications, the electrical properties of the material should be experimentally measured for ion implantation. More complicated staggered patterns should also be investigated.

STAR★METHODS

Detailed methods are provided in the online version of this paper and include the following:

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SUPPLEMENTAL INFORMATION

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AUTHOR CONTRIBUTIONS

Qing Hao supervised the work. Sien Wang performed the experiments. Yue Xiao and Sien Wang performed the simulations. Sien Wang, Yue Xiao, and Qiyu Chen performed the data analysis. Sien Wang, Yue Xiao, and Qing Hao wrote the article.

DECLARATION OF INTERESTS

The authors declare no competing interests.

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STAR★METHODS

KEY RESOURCES TABLE

REAGENT or RESOURCE	SOURCE	IDENTIFIER
Software and algorithms		
Fortran	Intel Corporation	https://www.fortran90.org/
MATLAB	MathWorks, Inc.	https://www.mathworks.com/
SigmaPlot	SPSS Inc.	https://systatsoftware.com/sigmaplot/

RESOURCE AVAILABILITY

Lead contact

Further information and requests for resources including data and code should be directed to and will be fulfilled by the lead contact, Dr. Qing Hao (qinghao@arizona.edu).

Materials availability

This study did not generate new unique materials.

Data and code availability

Any additional information required to re-analyze the data reported in this paper is available from the lead contact upon request.

The phonon Monte Carlo simulation code is unavailable for now.

METHOD DETAILS

Device fabrication

All devices were fabricated from the 70-nm-thick device layer of a silicon-on-insulator (SOI) wafer. Nanoslots of various sizes and pitches were defined with EBL (Elionix ELS-7000). Reactive ion etching (RIE) with an SF_6/Ar recipe was used to remove the Si layer and thus produce the nanoslot-patterned Si beam. The sample was then wet etched in the diluted hydrofluoric acid (DHF) solution to remove the underlying 2-μm-thick buried oxide (BOX) layer and fully suspend the nanoporous Si thin film. All thermal measurements were based on the AC self-heating of a suspended device, i.e., the 3ω method (Hao et al., 2018b, 2020, 2018b; Xiao et al., 2019). As the heater and electrical resistance thermometer, an electrically conductive layer consisting of 10 nm Cr and then 40 nm Pt was deposited onto the Si device via electron beam evaporation. Before thermal measurements, each sample was carefully examined under a scanning electron microscope (SEM) to ensure the quality of the suspended bridge and measure the exact dimension of nanoslot patterns. The suspended region is 20 × 2 μm in the top view (Figure 2). SEM images for different device configurations can be found in the supplemental information (Figure S1). It is acknowledged that pore-edge defects (e.g., roughness, oxidation, amorphization) introduced during the nanofabrication process could affect the phonon transport inside the nanoporous structure (Hao et al., 2018a), which can effectively expand the pore size (Ravichandran and Minnich, 2014). For the feature sizes of our fabricated nanoslot patterns, the ~2 nm surface layer introduced by dry etching (Tang et al., 2010) can be neglected for its impact and the comparison between aligned and offset patterns is unaffected when both patterns are fabricated under the same etching condition.

Ion implantation with an FIB

To locally introduce defects on a nanoslot-patterned Si thin film, ion implantation was performed within a Ga FIB (FEI Helios NanoLab 660) before the metal deposition. The dose was calculated by multiplying the beam current, exposure area and exposure time. Since the ion beam was bombarded onto a small area, rapid ion implantation with high doses can be achieved. During the exposure, the acceleration voltage

for the Ga^+ ions was set to 500 eV to minimize the milling effect. The sputter yield, which is the ratio between the number of removed atoms and irradiated ions, is around 0.7 for Si under 500 eV ion bombardment (Rossnagel, 2001). Based on this value, the thickness of the Si removed during the exposure is estimated to be 0.14 nm for the largest dose, which is negligible compared with the 70 nm film thickness.

Thermal characterization

The in-plane thermal conductivity measurement was carried out in a high vacuum (<1 × 10^{-4} Torr) with the 3ω method (Cahill, 1990; Lu et al., 2001). The measurement temperature range was from 83 to 300 K for all samples. An AC source (Keithley 6221) was used to generate a heating current at an angular frequency ω. Using differential circuits to eliminate the 1ω signal, the third-harmonic root-mean-square (RMS) voltage ($V_{3\omega}$) of the sample and the corresponding phase lag were recorded by a lock-in amplifier (Stanford Research SR830).

In the data analysis, the effective in-plane thermal conductivity k and specific heat of the metal-coated film can be extracted by fitting $V_{3\omega}$ as a function of the angular frequency, given as (Lu et al., 2001)

$$V_{3\omega} \approx 4I^3 LRR' \Big/ \left(\pi^4 kS\sqrt{1+(2\omega\gamma)^2}\right) \qquad \text{(Equation 2)}$$

In Equation 2, I is the RMS heating current, R is the electrical resistance, $R' = dR/dT$, T is the absolute temperature, L is the length and S is the cross-sectional area of the suspended film. The volumetric specific heat (C_p) can be further calculated from the thermal time constant $\gamma = C_p L^2/\pi^2 k$ for the metal-coated film. The linear regression is performed by transforming Equation 2 into the following form:

$$\frac{1}{V_{3\omega}^2} = \left[\frac{2\pi^4 Sk\gamma}{4I^3 LR(dR/dT)}\right]^2 \omega^2 + \left[\frac{\pi^4 Sk}{4I^3 LR(dR/dT)}\right]^2 \qquad \text{(Equation 3)}$$

Figure 3 shows the analysis result of Sample 1a at 300 K, with $R^2 > 0.9995$ for the linear fitting.

To obtain the in-plane thermal conductivity of the Si film itself, the k contribution from the metal layer should be subtracted. The thermal conductivity of the metal layer can be estimated from its electrical conductivity σ using the Wiedemann-Franz law, $k_E = L\sigma T$. The employed temperature-dependent Lorenz number L has been calibrated in an earlier study on an identical metal layer (Hao et al., 2018b). For the specific heat of the metal layer, bulk values for each material are used in the calculation.

Phonon MC simulation

In phonon MC simulations, the movement and scattering of individual phonons are tracked to yield a statistical description of the transport process, as an alternative way to solve the phonon BTE. By employing the periodic heat flux boundary condition (Hao et al., 2009; Hao and Xiao, 2020), a single period can be selected as the computational domain to minimize the computational load. The computational efficiency can be further improved using a variance-reduced MC technique developed by Péraud and Hadjiconstantinou, where the tracked "useful" phonons are related to the distribution function distortion from an equilibrium distribution function, i.e., the Bose-Einstein distribution at a reference temperature (Péraud and Hadjiconstantinou, 2011). These tracked phonons are directly associated with the net heat flow across a structure. Phonon boundary scattering and internal scattering are two scattering events in the simulation. The former includes scattering with the nanoslot edge and top/bottom film surfaces, which are both treated as diffusive. Considering impurity scattering and Umklapp (U) scattering, the internal phonon scattering rate is expressed as $1/\tau(\omega) = A_1\omega^4 + B_1\omega^2 T exp(-B_2/T)$. In the expression, $\tau(\omega)$ is the phonon relaxation time depending on the phonon angular frequency ω, A_1 is the parameter for the impurity scattering, B_1 and B_2 are the parameters for the U processes. The employed parameters were obtained by fitting the temperature-dependent k_L of bulk Si (Hao, 2014; Wang et al., 2011). Following these works, $A_1 = 1.69 \times 10^{-45}\ s^3$, $B_1 = 1.53 \times 10^{-19}\ s/K$ and $B_2 = 140\ K$ were used in the simulation of undoped samples. For samples with point defects introduced by the ion implantation, the A_1 value should be further increased to account for stronger point-defect phonon scattering (Hao et al., 2010).