Derivation and Validation of a Common-Mode Model for a Neutral Point Clamped Dual Active Bridge

Ryan Olson
Dept. of Electrical Engineering
University of Wisconsin-Milwaukee
Milwaukee, WI 53212 USA
olson299@uwm.edu

Ahmad El Shafei
Dept. of Electrical Engineering
University of Wisconsin-Milwaukee
Milwaukee, WI 53212 USA
aie@uwm.edu

Tianchen Li
Dept. of Electrical Engineering
University of Wisconsin-Milwaukee
Milwaukee, WI 53212 USA
tianchen@uwm.edu

Robert Cuzner
Dept. of Electrical Engineering
University of Wisconsin-Milwaukee
Milwaukee, WI 53212 USA
cuzner@uwm.edu

Adel Nasiri
Dept. of Electrical Engineering
University of South Carolina
Columbia, SC 29208 USA
nasiri@sc.edu

Yue Zhao
Dept. of Electrical Engineering
University of Arkansas
Fayetteville, AR 72701 USA
yuezhao@uark.edu

Zhuxuan Ma
Dept. of Electrical Engineering
University of Arkansas
Fayetteville, AR 72701 USA
zm009@uark.edu

2022 IEEE Energy Conversion Congress and Exposition (ECCE) | 978-1-7281-9387-8/22/$31.00 ©2022 IEEE | DOI: 10.1109/ECCE50734.2022.9947783

***Abstract*—This paper applies a common-mode modeling approach for a Silicon Carbide (SiC) based medium voltage neutral point clamped (NPC) dual active bridge (DAB) with a 2 level Full-Bridge (2L-FB) stage utilizing an electromagnetic interference (EMI) characterization testbed. A common-mode equivalent circuit model (CEM) for the system is derived, which accurately captures the effect of cross-mode coupling behavior between differential-mode and common-mode caused by circuit asymmetries, such as baseplate capacitance of multi-chip power modules or windings in the transformer. This cross-mode coupling effect is required to accurately model EMI at the higher frequencies of the conducted emissions standards. The derived CEM shows close agreement when compared to the mixed-mode simulation, verifying the model's efficacy. Additionally, baseplate current was shown to be minimized by tying the neutral point of the converter to the heatsink, where this result can be explained through the CEM. The CEM of the NPC DAB will be validated through empirical measurements on an EMI characterization testbed. The testbed features a copper ground plane and custom-built LISNs that can handle the unfiltered harmonic and EMI content of power electronic converters.**

***Index Terms*—EMI, Common-mode, ANPC, DAB**

I. Introduction

Continued efforts in developing wide-bandgap (WBG) semiconductors have provided more efficient devices that lead to more power-dense power electronic converters. However, the higher voltages, faster edge rates, and increased switching frequency produce a problematic level of conducted emissions in the form of common-mode (CM) current [1]. The CM noise introduced can be a detriment not only to the converter itself but also to the surrounding systems. This CM noise can find its way through unexpected ground paths within the power distribution network and cause potential radiated emissions issues.

The transformer is a key asset of any electrical distribution system and has two main jobs: (1.) voltage transformation and (2.) provision of galvanic isolation between the ground potentials. Galvanic isolation can be extremely effective for providing human safety and improving noise immunity between circuits. However, frequency content in the high-frequency spectral range is introduced to the system as a byproduct of simultaneous higher voltage blocking capability and higher switching frequency (consequently reducing transformer size) that can be realized with WBG-based systems. Reducing the size of the transformer brings with it increased parasitic capacitance between primary to secondary sides of the transformer which, combined with the increased spectral content due to high $\mathrm{d}v/\mathrm{d}t$, lower loss switching of SiC MOSFETs results in high frequency circulating currents between primary and secondary circuits.

Electromagnetic (EMI) characterization methodologies have been emphasized in recent years as a means of gaining insight into root causes of self and system compatibility issues and as a means to EMI filter over-design. EMI characterization

This material is based upon work supported by the National Science Foundation under Grant No. 1650470. Any opinions, findings, and conclusions or recommendations expressed in this material are those of the author(s) and do not necessarily reflect the views of the National Science Foundation.

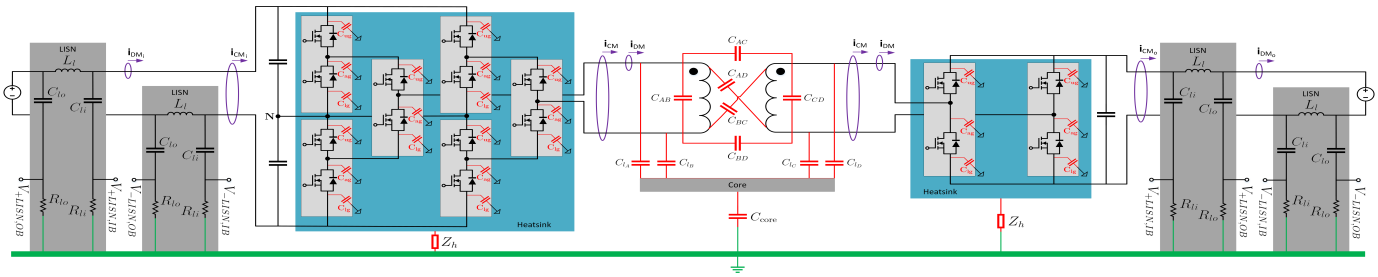

Fig. 1. EMI Characterization Platform, Dual Active Bridge MM Circuit with LISNs

provides quantified insights into the EMC design challenge. Proper characterization is necessary to determine the correct amount of attenuation required to meet standards. If a method quantifies the EMI behavior with minimal computational burden, the iteration process is manageable to allow the implementation of automated EMI filter optimization algorithms. Various EMI characterization methodologies have been explored by many researchers and generally fall under categories of direct circuit [2], FEA assisted [3], or empirically driven models [4]. These approaches can be categorized as either black-box methodologies [4], which lack high-frequency accuracy, or white-box methodologies [2], [3], which can be computationally burdensome and time consuming. To balance the analysis accuracy and simulation efficiency, a gray-box approach [5]–[8] is applied in this work for EMI characterization. This modeling approach establishes a mathematical foundation by breaking up a mixed-mode (MM) circuit into its corresponding differential-mode (DM) and common-mode (CM) equivalent models (DEMs/CEMs), and captures the CM/DM cross-mode coupling caused by asymmetries. The approach enables accurate reproduction of waveforms up to 30 MHz [9].

To this end, this paper applies the methodology demonstrated in [7] to the SiC-based NPC dual active bridge (DAB). This work derives the CEM and associated DM cross-coupling for an Active Neutral Point Clamped (ANPC-FB), 2L-FB, and medium frequency (MF) transformer. These CEMs are then combined to form the full NPC DAB CEM. The CEMs are derived in Section II, validated through simulation in Section III, and the beginning stages of validation through hardware in Section IV. To the best of the author's knowledge, such derivation and validation for an NPC DAB have not been done in the literature.

II. Common-Mode Derivation

The NPC DAB converter is a candidate topology for applications in power distribution systems due to its high power density, low device stresses, galvanic isolation, and bidirectional operation. With its high demand in power electronics, this paper has been directed towards an accurate EMI characterization and reduction methodology to support the design of the DAB as a sub-module for much larger system applications. The NPC DAB topology and its corresponding test platform can be seen in Fig. 1. On the primary side of the transformer, there is a type-1 NPC full-bridge converter and can either be active (i.e. controlled as an ANPC converter) or commutated through the diode depending on controls or voltage balance techniques. On the secondary side of the transformer, there is a 2L-FB.

The CM modeling methodology establishes a mathematical equivalent circuit modeling technique where the dominant parasitic paths are parameterized and combined with CM voltage sources representing the impact of power electronic switching for an accurate prediction of conducted emissions. A systematic CM modeling approach is used where the objective is to define the CM voltage with respect to an arbitrary reference point, which is distinct from the ground. This floating reference makes it possible for the transformation of MM system components into CM equivalent components, which can then be systematically assembled to form CM equivalent circuits. These equivalent circuits accurately model the effects of mutual coupling between CM and DM voltages and currents due to circuit asymmetry. With this, there is a simple connection of these CM equivalent circuits that can be used to form the CM models for an entire system. The Line Impedance Stabilization Networks (LISNs) connected to the lines on the inputs and outputs of the converter provide known CM impedances for the source and load side CM current paths and points to ground current measurement through each LISN resistor in order to provide hardware validation points for assumptions regarding internal parasitic capacitance paths to ground. The model validation approach is described in [9].

The full CM equivalent model will be comprised of three CM subsystems: the CM circuit of the Active Neutral Point Clamp full-bridge (ANPC-FB), the CM circuit of the MF transformer, and the CM circuit of the 2L-FB.

A. Converter CM Modeling

The first step in the proposed modeling methodology is to generate a CM equivalent circuit for each component of the power system. A detailed derivation of CM models for many types of converters has been covered in previous work [10].

The general procedure for producing such an equivalent circuit from the component's DM model is broken into a few steps. First, parasitic couplings that provide paths for CM currents are identified and added to the DM model to form a MM model, shown in Fig. 1. The MM model is broken into its converter subsystems, and every interconnection point, or

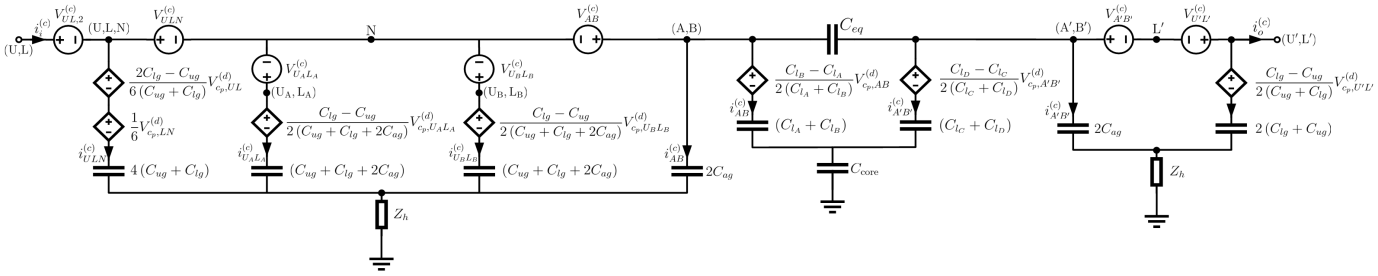

Fig. 2. Dual Active Bridge CEM

node, within the converter itself is labeled. When looking at these nodes, calculate the total paralleled capacitance to the heatsink for each node. Next, gather two or more nodes into "super-nodes", which need to be in proximity and make sense. Typically the super-nodes will be input nodes, output nodes, or symmetrical interconnection nodes. Once the super-nodes are assigned, construct a parasitic capacitance model. When following this procedure, two-line and three-line parasitic capacitance models are typically encountered (Fig. 3).

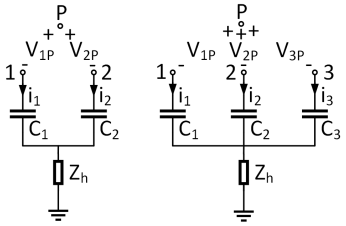

Fig. 3. Two-line (left) and three-line (right) capacitor models

By using KVL, line voltages for the model are determined with respect to an arbitrary reference point, P. The KVL for the two-line model in matrix form is,

$$\begin{bmatrix} V_{Pg} \\ V_{Pg} \end{bmatrix} = \begin{bmatrix} V_{1P} \\ V_{2P} \end{bmatrix} + \frac{1}{\hat{p}} \begin{bmatrix} \frac{1}{C_1} & 0 \\ 0 & \frac{1}{C_2} \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \end{bmatrix} + \begin{bmatrix} R_h & R_h \\ R_h & R_h \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \end{bmatrix}$$

where $\hat{p}$ is the Heaviside operator. Using the CM and DM definitions for currents and voltages

$$\begin{aligned} V^{cm} = (V_1 + V_2)/2 \ , \quad V^{dm} = V_1 - V_2 \\ i^{cm} = i_1 + i_2 \quad , \quad i^{dm} = (i_1 - i_2)/2 \end{aligned}$$

and applying these definitions to transformation matrices

$$T_2^v = \begin{bmatrix} 1 & -1 \\ 1/2 & 1/2 \end{bmatrix}, \quad T_2^i = \begin{bmatrix} 1/2 & -1/2 \\ 1 & 1 \end{bmatrix}$$

such that,

$$\begin{bmatrix} V^{dm} \\ V^{cm} \end{bmatrix} = T_2^v \begin{bmatrix} V_1 \\ V_2 \end{bmatrix}, \quad \begin{bmatrix} i^{dm} \\ i^{cm} \end{bmatrix} = T_2^i \begin{bmatrix} i_1 \\ i_2 \end{bmatrix}$$

Applying these transformation matrices to the KVL equation decomposes the MM equation into its corresponding DM and CM equations. Then extracting the CM expression for a general two-line parasitic capacitor model results in

$$V_{Pg} = -V^{cm} + \frac{C_2 - C_1}{2\,(C_1 + C_2)} V^{dm}_{c_p,12} + \frac{i^{cm}}{\hat{p}\,(C_1 + C_2)} + Z_h i^{cm} \tag{1}$$

This expression is then extended to a single line circuit, which takes the form shown in Fig. 4. The total voltage from arbitrary point P to ground includes; the CM voltage source from P to the super-node, the DM coupling into the CM circuit (dependent voltage source), the total CM parasitic capacitance, and the heatsink impedance. When modeling a grounded system the heatsink impedance is simply a resistive connection to ground, and when a floated system is modeled there is a small capacitance in series with the resistive connection to ground.

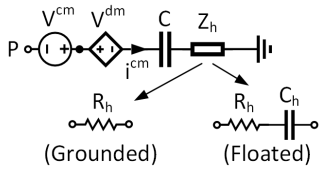

Fig. 4. CEM section example

Using this same procedure, the CEM for a three-line capacitor model can be derived with the CM expression shown in Eq. 2.

$$\begin{aligned} V_{Pg} = -V^{cm} + \frac{i^{cm}}{\hat{p}\,(C_1 + C_2 + C_3)} + Z_h i^{cm} \ \cdots \\ + \frac{C_2 + C_3 - 2C_1}{3\,(C_1 + C_2 + C_3)} V^{dm}_{c_p,12} + \frac{2C_3 - C_1 - C_2}{3\,(C_1 + C_2 + C_3)} V^{dm}_{c_p,23} \end{aligned} \tag{2}$$

With (1) and (2), it is possible to construct the full system CEM. From inspection, as you increase the number of nodes in the super-node the more information it contains in each branch. By sticking with two- and three-line super-node models, it greatly reduces the complexity and the amount of DM coupling terms in each branch. Once this is applied to each component of the power system, the connection of each system is pieced together to form a CM equivalent circuit for the entire system. When piecing together each CM branch, the arbitrary reference point needs to be chosen. There is freedom in what is

chosen for the arbitrary reference, but it makes sense to choose a point that is common within each converter separately (i.e. ANPC-FB, 2L-FB). For the CEMs produced in the paper, the arbitrary reference point for the ANPC-FB is chosen to be the neutral point (N), and for the 2L-FB it is chosen to be the lower dc bus connection (L). From there, it is a simple connection of similar reference points and super-nodes together to form the full system CEM.

B. Transformer Modeling

The CM modeling of the MF transformer has been derived from a simplified transformer parasitic model, Fig. 5. These lumped parasitic capacitance's seen are used to model conduction paths for the high-frequency currents. The inter- and intra-winding parasitics, labeled in blue, have originated from the basic six capacitor model for winding parasitics. Each winding has a leakage capacitance due to the core and is labeled in red. The voltage stresses and winding capacitance are increased when grounding the core, for this reason, the core has been floated and this can be seen as some standoff capacitance, labeled in green.

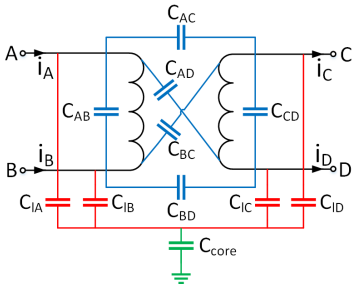

Fig. 5. Simplified transformer model

Since the transformer provides isolation, it makes sense to group up the input and output nodes separately. With the input and output super-nodes chosen, three main CM paths can be seen. First, a CM path from nodes (A,B) to ground through leakage paths containing C_{lA} and C_{lB}. This creates a two-line parasitic capacitor model, therefore plugging the capacitance values into (3) provides a CM expression that can be constructed into a single line CM branch. Similarly, on the secondary side a CM path flows from nodes (C,D) to ground through leakage paths containing C_{lC} and C_{lD}. Resulting in another two-line parasitic capacitor model, where (3) is used again to construct another single line CM branch. The final CM path is the parasitic coupling path through the windings. Due to the nature of the modeling approach, the input nodes and output nodes are shorted, leaving an equivalent capacitance which consists of a parallel combination of the inter-winding capacitance. The intra-winding capacitance vanishes from the CM model, which makes sense as it primarily contributes to DM operation. The fully constructed CEM for the MF transformer is shown in Fig. 6. With transformer isolation there isn't a common reference point, therefore, the arbitrary reference points are influenced by its neighboring converter. So the primary reference point P_1 is shared with the ANPC-FB converter (N), and the secondary reference point P_2 is shared with the 2L-FB (L).

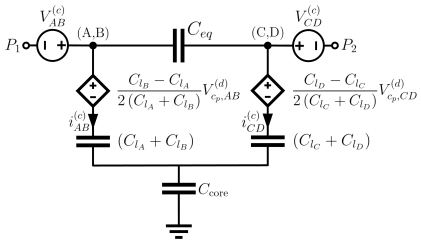

Fig. 6. Transformer CEM

C. Transformer Parasitic Calculation

The cross-sectional view of the current design of the MF transformer can be seen in Fig. 7. Our objective is to correlate the capacitance obtained from analytical calculations and Finite Element Analysis (FEA) simulations incorporated into the simplified six-capacitor transformer parasitic model.

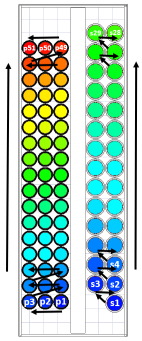

Fig. 7. Transformer cross-sectional view

Due to long computation time for FEA simulations, an analytical method of obtaining parasitic elements of the MF transformer needs to be established [11]. This analytical method provides ways of determining winding parasitics which correlate to the equivalent six capacitor model for multi-layer windings. This approach is used for windings consisting of solid or litz wire, but the calculations are carried out using solid wire approximations. For litz wires, the nominal radius can be calculated by subtracting the thickness of the litz wires outer insulation and the thickness of the insulation of a single strand from the total radius of the complete litz wire. The outer diameter of the litz wire can be taken from the data sheet of the wire.

All calculations carried out for the equivalent winding capacitance are based on the static layer-to-layer capacitance. With this capacitance, the electrical energy which is stored between two successive winding layers is calculated and then used for calculating the equivalent capacitance for the whole winding arrangement. The winding capacitance of a transformer primarily depends on the winding arrangement, in which the windings can either be wrapped orthogonal or

orthocyclic to each successive layer. In orthogonal windings the turns of successive layers are orthogonally on top of each other, whereas in orthocyclic windings the turns of the successive layers are in the gaps between the turns of the preceding layer.

The current transformer design follows an orthogonal winding arrangement, in this arrangement the layer-to-layer capacitance is calculated by assuming the layers of the winding are equipotential surfaces that are used to approximate the electric flux lines as straight lines. With the considered path of the flux lines, a certain permittivity of the wire insulation and the insulation between the gaped layers with distance h, and the given layer-to-layer voltage, the electric field strength in different sections of the approximated flux line can be calculated. The electric field strength is used for calculating the electric energy which is stored between the two wires lying on top of each other. This energy is equated to the electric energy which is stored in the equivalent capacitor, and then multiplying this capacitance by the number of turns per layer, z, results in the static capacitance of the two layers.

$$C_{s,ortho} = \frac{\epsilon_o \cdot z \cdot l_{w,m}}{\alpha} \cdot \left[V + \frac{1}{8 \cdot \epsilon_D} \cdot \left(\frac{2 \cdot \delta}{r_o} \right)^2 \cdot \frac{Z}{\alpha} \right] \quad (3)$$

with,

$$\alpha = 1 - \frac{\delta}{\epsilon_D \cdot r_o}; \quad \beta = \frac{1}{\alpha} \left(1 + \frac{h}{2 \cdot \epsilon_F \cdot r_o} \right)$$

$$V = \frac{\beta}{\sqrt{\beta^2 - 1}} \cdot \arctan \left(\sqrt{\frac{\beta + 1}{\beta - 1}} \right) - \frac{\pi}{4}$$

$$Z = \frac{\beta \left(\beta^2 - 2 \right)}{\left(\beta^2 - 1 \right)^{3/2}} \cdot \arctan \left(\sqrt{\frac{\beta + 1}{\beta - 1}} \right) - \frac{\beta}{2 \left(\beta^2 - 1 \right)} - \frac{\pi}{4}$$

where, $l_{w,m}$ is the mean turn length of the two considered layers, ϵ_o is vacuum permittivity, ϵ_D is the dielectric constant of the wire insulation, and ϵ_F is the dielectric constant of the insulation between the layers.

The static layer-to-layer capacitance does not take into account the voltage distribution between the layers, which is dependent on the winding method. There are two winding methods discussed in this paper; standard and flyback winding methods, shown in Fig. 8.

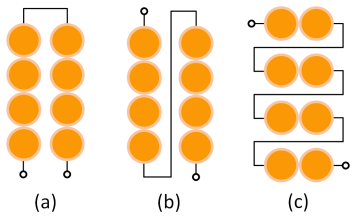

Fig. 8. (a) Standard winding; (b),(c) flyback winding

For the standard winding method, one side of the two layers is shortened and the voltage between the two layers at the unconnected end is doubled, which leads to a relatively high electric field strength and dielectric losses. With the flyback winding method all layers are wound in the same direction and the voltage between the two layers is consistently equal to one another. Therefore, the electric field strength and dielectric stress are uniformly distributed and thus lower compared to the standard winding method. Equating the stored electrical energy to the energy which is stored in the equivalent layer capacitor results in

$$C_{layer,flyback} = C_{s,ortho}/4 \quad (4)$$

The disadvantage of the flyback winding method is that at the end of one layer the wire of the winding has to cross all turns of this and its next layer, resulting in a larger overall winding length with more complexity for manufacturing.

With the calculation of the equivalent layer capacitance for two layers defined, the equations can now be extended for multilayer windings. The equivalent capacitor for the complete winding is calculated by equating the energy stored in this capacitor to the energy which is stored in all the layer capacitors. If all layer capacitors are equal, the equation for the equivalent winding capacitor is greatly simplified to

$$C_{winding} = 4 \cdot \frac{N_{layer} - 1}{N_{layer}^2} \cdot C_{layer} \quad (5)$$

Let us consider a multilayer winding where all layers except the last layer has z turns and the last layer has k turns, where $k < z$. The equivalent winding capacitor is calculated by transforming all interlayer capacitors to the connection of the winding by the impedance transformation rule of transformers. If it is assumed that all interlayer capacitances are the same the equivalent winding capacitor is simply

$$C_{winding} = \frac{4 \cdot C_{layer} \cdot (N_{layer} - 1) \cdot \left(z^2 + k^2 \right)}{\left((N_{layer} - 1) \cdot z + k \right)^2} \quad (6)$$

Previously, an equivalent capacitance for two or more layers of the same winding has been calculated. This same technique can be used for calculating the equivalent capacitance for two layers from different windings (i.e. primary and secondary windings). The electrostatic behavior for two layers of different windings can be modeled by six independent capacitors. The values of the six capacitors are calculated using the energy approach, similar to the previous calculations. The six capacitors can be expressed in terms of the static winding capacitance C_s, where it is assumed that $C_{AB} = C_{CD}$, $C_{AC} = C_{BD}$, and $C_{AD} = C_{BC}$.

$$C_{AB} = -\frac{C_s}{6}, \; C_{AC} = \frac{C_s}{3}, \; C_{AD} = \frac{C_s}{6} \quad (7)$$

With all of this information, the calculation of the winding parasitic capacitance for the current transformer design can be done. The transformer employs the flyback winding method, similar to Fig. 8(c), with an orthogonal winding arrangement. The primary side has 17 layers, 3 turns per layer, and no distance between between consecutive layers. The secondary side has 15 layers, 2 turns per layer, an incomplete layer containing a single turn, and no distance between layers. The wire

constants are obtained from data sheets, and the mean turn length is determined by assuming a tight winding construction. The primary and secondary winding capacitance is calculated using (5) or (6), respectfully. For the equivalent capacitance between the primary and secondary layers, only the static layer-to-layer capacitance (3) needs to be calculated, where the values used is the average between the primary and secondary winding values, and the insulation thickness between windings is accounted for. With this static capacitance, the equivalent capacitance is extended to the six-capacitor model following the assumptions made in (7). Finally, the primary winding capacitance which is in parallel with C_{AB} can be summed together, and likewise with the secondary winding capacitance and C_{CD}. This results in a calculated equivalent parasitic model for the windings of the MF transformer, shown in Fig. 9.

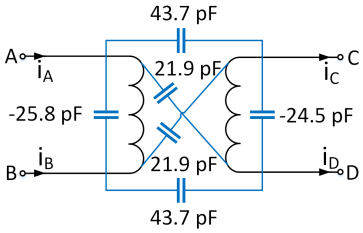

Fig. 9. Calculated Winding Parasitics

An FEA simulation will be used to calculate the leakage capacitance for the rest of the CEM model, and will also be used to verify the analytic results. Once the transformer is finalized and built, the parasitic capacitance will be measured experimentally and will be compared with both the FEA and analytical methods.

III. Simulation Validation

To validate the CM analysis, a time-domain simulation was performed for the detailed MM model of the power system. A PLECS blockset integrated into MATLAB Simulink is used, where the controls are created in Simulink and the electrical circuits are modeled in PLECS. A single-phase shift modulation scheme has been developed, where the switching frequency and duty cycles are predetermined, and then closed-loop controls are applied to determine the phase shift needed to achieve the desired power level. All of the CM voltage inputs to the model were determined analytically from the steady-state DM operating point of the system. This steady-state DM operating point can be seen at the transformer interface, where the voltages and currents are shown in Fig. 10.

The CEM for the ANPC-FB and 2L-FB of the DAB have been validated, showing very accurate results of the displacement current through the heatsink for both the CM and MM models. The validation of the CEM is done for a system where every heataink is grounded (Fig. 11) and floated (Fig. 12).

In these figures, both the CEM and MM measurements line up exactly with no error between the two. From inspection,

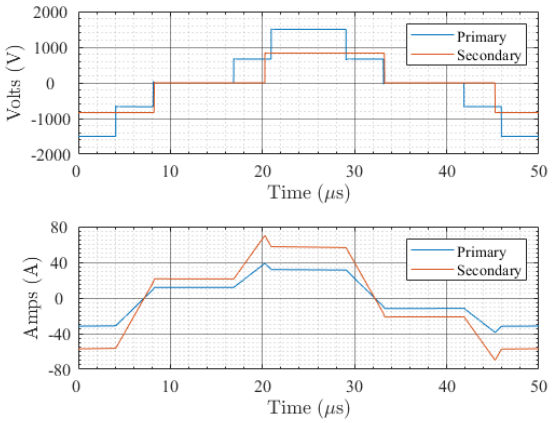

Fig. 10. Steady-state voltages (top), currents (bottom)

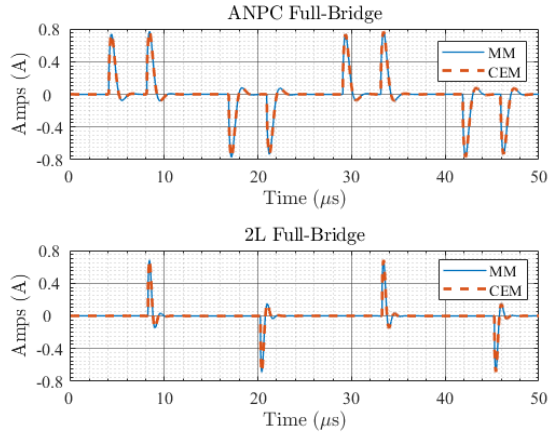

Fig. 11. CM validation, grounded heatsink

a grounded system produces the greatest amount of CM current with peak values at 0.8 Amps. CM current through the transistor baseplate can degrade power semiconductor module insulation, and by floating the heatsink we can limit the insulation stress on the devices. The CEM validation/measurements have verified this by reducing the peak currents and shortening the amount of time that the currents are flowing.

While keeping the heatsink floated, a few CM mitigation efforts have been investigated for the ANPC-FB converter. The most significant method of decreasing the amount of CM displacement current through the heatsink into the ground potential was discovered by tying the neutral point of the ANPC-FB converter to the heatsink. This technique reduced the CM displacement current from amps down to a tens of micro amps, which resulted in a reduction with a few orders of magnitude. A plot of displacement current implementing this technique can be seen in Fig. 13. This method essentially shorts all parasitic capacitors seen by the neutral point of the ANPC, which makes up for about 25 percent of the total parasitic paths. Mathematically, this reduces the DM coupling into the CM circuit and reduces the total parasitic capacitance.

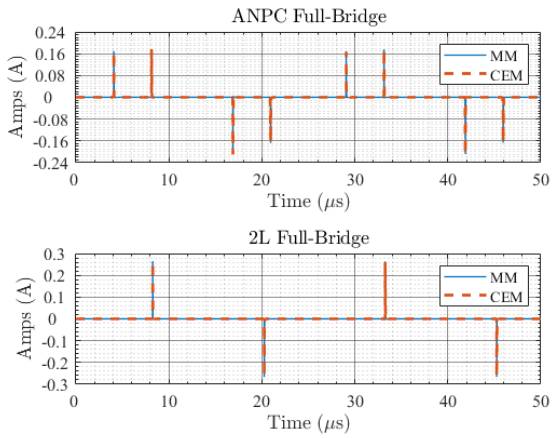

Fig. 12. CM validation, floated heatsink

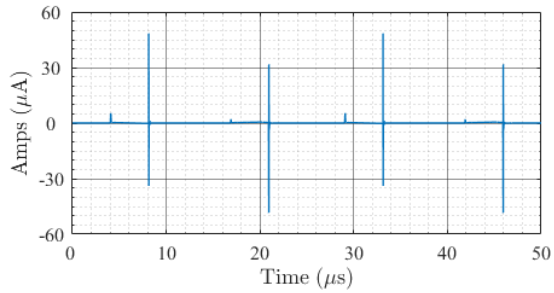

Fig. 13. ANPC CM current, neutral clamped heatsink

To the author's knowledge and the tools provided, it is difficult to float the transformer and provide parasitic paths for CM validation in simulation. This necessitates the need for validation of the transformer using hardware.

IV. Hardware Validation/EMI Characterization

The HF characterization, transformer CEM, and impacts of heatsink grounding on CM currents will be validated and verified using all SiC MOSFET power modules. The 2L-FB and ANPC half-bridge (ANPC-HB) building blocks are used to construct the full system consisting of 1.7 kV SiC MOSFET power modules (HT-3234-R-VB) from CREE [12]. Both double pulse tests (DPT) and pump-back tests have been performed to validate the effectiveness of the ANPC converter. DPT was performed at 2.4 kV dc bus and 400 A load current. In the DPT, the module under test withstood 1.2 kV dc.

To successfully characterize the conducted emissions, a multi-step process needs to be followed. First, the parasitic capacitance of the switching module is extracted, this is required to accurately model the conducted emissions. Secondly, the full system is broken into multiple stages, with each stage having a controlled CM path through LISNs. Finally, multiple tests are performed to measure the conducted emissions and validate the CEMs.

The custom-designed EMI characterization platform uses an unconventional configuration of LISNs on both the input and output of the system. This configuration allows observation of the conducted emissions generated, and by taking the difference of the input and output CM currents, the displacement current into the ground can be determined.

The stages of testing are performed in this order: 2L-FB, ANPC-HB, ANPC-FB, some intermediate step using both full-bridges, and the DAB. Each stage will allow for the converter to be placed on the ground plane of the test platform with the LISNs connected to the input and output. The impacts of grounding and floating the heatsink on conducted emissions are studied. For the ANPC converters the impact of a floating neutral clamped heatsink on conducted emissions will be characterized in future work. Once both the 2L-FB and ANPC-FB have been characterized separately, the penultimate stage utilizes both full-bridges as calibrated parts of the EMI test and characterization platform, without introducing any additional CM paths. The final stage, also to be performed in future work, will allow validation of all assumptions regarding the transformer CEM, including the model developed in this paper. Once this final step is completed, the future aim is to integrate a validated MF transformer CEM into full system design processes that provide insight into the impacts of conducted emissions compliance and assurance of robust self-compatibility. Fig. 1 shows the final EMI test and characterization environment.

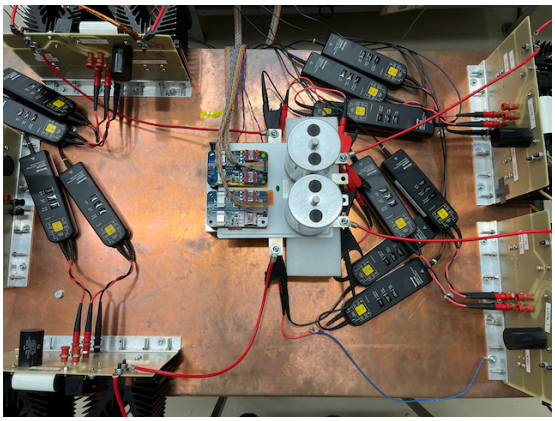

Fig. 14. Two-level full-bridge converter on EMI characterization platform

A. Two-Level Full-Bridge Converter Characterization

The EMI conducted emission of the 2L-FB is characterized by a methodology demonstrated in [8]. As shown in Fig. 14, the un-filtered full-bridge is configured as a 500 V inverter, where the MOSFETs legs are switching at 20 kHz, 50 % duty-cycle, with a bipolar scheme. It is terminated with a set of custom-made MIL-STD line impedance stabilization networks (LISNs) from the dc-side, and a set of artificial networks from the ac-side. Both the LISNs and the artificial networks have calibrated common-mode paths, therefore, ensuring an accurate common-mode measurement in frequency up to 30 MHz. The in-situ voltage measurements on LISN measurement ports provide the waveforms necessary for EMI characterization of

the full-bridge under test. Fig. 15 and Fig. 16 present the EMI characterization results of the un-filtered full-bridge in time-domain and in frequency-domain. The results show that the common-mode EMI component is dominating the lower frequency between 10 kHz to 1 MHz and the differential-mode component is dominating the higher frequency. In this configuration, no obvious cross-mode coupling can be observed from the EMI spectrum. The estimated parasitics of the MOSFET modules shows close-to-symmetric pole-to-chassis parasitic capacitances, which explains the absence of the cross-mode coupling effects.

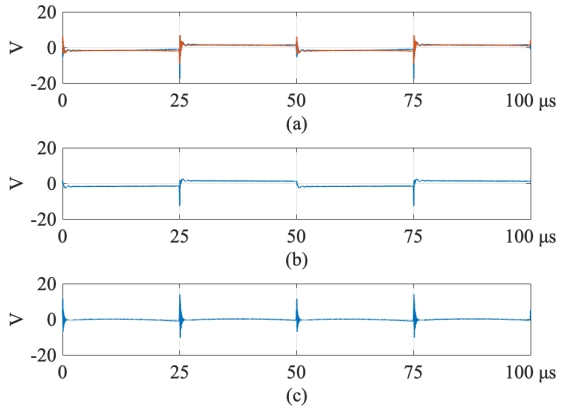

Fig. 15. Two-level full-bridge converter EMI characterization in time-domain. (a) mixed-mode (DC+ and DC-), (b) common-mode, (c) differential-mode.

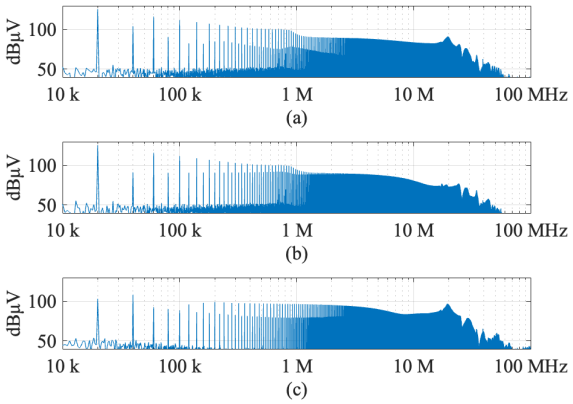

Fig. 16. Two-level full-bridge converter EMI characterization in frequency-domain. (a) mixed-mode, (b) common-mode, (c) differential-mode.

V. Conclusion

This paper describes the full process for CM modeling, or derivation of a CEM, for an NPC DAB comprised of ANPC-FB and 2L-FB converters on each side of a MF transformer. The CEM captures the effect of DM cross-coupling into the CM circuit, which enables accurate reproduction of waveforms measured at LISNs, up to 30 MHz, based upon the custom EMI characterization testbed. The CEM is validated alongside a detailed MM time-domain simulation of the entire system, and baseplate current is shown to be minimized by tying the neutral point of the NPC converter to the floated heatsink. The beginning stages of hardware validation using the EMI characterization testbed are demonstrated, starting with the 2L-FB converter. The full process, which will include ANPC-FB characterization and validation, testbed-system calibration and validation of the CEM for the MF transformer derived in this paper, will be executed in follow-on work. All stages of the characterization are described. Future work will also includes comparing the analytical calculation of parasitic parameters of the MF transformer with FEA and empirical data. The ultimate goal is validate the MF transformer CEM and provide insight into conducted emissions for solid state transformers and enable system-level design optimizations that capture conducted EMI impacts out to the HF range.

References

[1] N. Oswald, B. H. Stark, D. Holliday, C. Hargis, and B. Drury, "Analysis of shaped pulse transitions in power electronic switching waveforms for reduced emi generation," *IEEE Transactions on Industry Applications*, vol. 47, no. 5, pp. 2154–2165, 2011.

[2] H. Chen and D. Divan, "High speed switching issues of high power rated silicon-carbide devices and the mitigation methods," in *2015 IEEE Energy Conversion Congress and Exposition (ECCE)*. IEEE, 2015, pp. 2254–2260.

[3] A. Dutta and S. S. Ang, "Electromagnetic interference simulations of power electronic modules," in *2015 IEEE International Workshop on Integrated Power Packaging (IWIPP)*. IEEE, 2015, pp. 83–86.

[4] B. Sun, R. Burgos, and D. Boroyevich, "Common-mode emi unterminated behavioral model of wide-bandgap-based power converters operating at high switching frequency," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 7, no. 4, pp. 2561–2570, 2018.

[5] H. Bishnoi, A. C. Baisden, P. Mattavelli, and D. Boroyevich, "Analysis of emi terminal modeling of switched power converters," *IEEE Transactions on Power Electronics*, vol. 27, no. 9, pp. 3924–3933, 2012.

[6] A. D. Brovont, J. Zhao, and A. N. Lemmon, "Modeling and validation of conducted emissions trends in medium-voltage power electronic systems," in *2020 IEEE Applied Power Electronics Conference and Exposition (APEC)*. IEEE, 2020, pp. 1438–1444.

[7] A. D. Brovont, "Generalized differential-common-mode decomposition for modeling conducted emissions in asymmetric power electronic systems," *IEEE Transactions on Power Electronics*, vol. 33, no. 8, pp. 6461–6466, 2018.

[8] T. Li, J. Gudex, J. Lentz, M. Vygoder, R. M. Cuzner, and J. Katcha, "Reduction of Intra-system Common-mode Electromagnetic Interference in Enclosed Wide-bandgap Four-pole Boost Converter," in *2021 IEEE Fourth International Conference on DC Microgrids (ICDCM)*. Arlington, VA, USA: IEEE, Jul. 2021, pp. 1–8.

[9] A. N. Lemmon, R. Cuzner, J. Gafford, R. Hosseini, A. D. Brovont, and M. S. Mazzola, "Methodology for characterization of common-mode conducted electromagnetic emissions in wide-bandgap converters for ungrounded shipboard applications," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 6, no. 1, pp. 300–314, 2017.

[10] R. Olson, "Common-mode modeling of neutral point clamped converter based dual active bridge," MS Thesis, The University of Wisconsin-Milwaukee, 2021.

[11] J. Biela and J. W. Kolar, "Using transformer parasitics for resonant converters-a review of the calculation of the stray capacitance of transformers," in *Fourtieth IAS Annual Meeting. Conference Record of the 2005 Industry Applications Conference, 2005.*, vol. 3. IEEE, 2005, pp. 1868–1875.

[12] Y. Wu, M. H. Mahmud, S. Christian, R. A. Fantino, R. A. Gomez, Y. Zhao, and J. C. Balda, "A 150-kw 99% efficient all silicon carbide triple-active-bridge converter for solar-plus-storage systems," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, 2020.