SAT-ATPG Generated Multi-Pattern Scan Tests for Cell Internal Defects: Coverage Analysis for Resistive Opens and Shorts

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***Abstract*—Recent advances in process technology have resulted in novel defect mechanisms making the test generation process very challenging. In addition to complete opens and shorts that can be represented via extreme defect resistance magnitudes, partial resistive opens and shorts are also of concern in deeply scaled CMOS technologies. For open defects with intermediate defect magnitude values, it has been shown that multi-pattern tests are necessary for defect exposure. We extend this approach to short defects with intermediate defect magnitude values to obtain a suite of multi-pattern tests for standard cell instances that cover complete as well as partial intra-cell open and short defects. A hierarchical scan-compatible SAT-based test generation approach for full scan sequential circuits is then proposed that allows such multi-pattern tests to be applied to the circuit via the scan infrastructure. A key innovation is the combined use of shift and capture operations along with launch-on-capture and launch-on-shift scan based test application for increased defect coverage. Resulting defect coverage improvements over conventional two-pattern tests are demonstrated on ISCAS89 benchmark circuits.**

***Index Terms*—Delay testing, SAT-ATPG, Multi-pattern test generation, Fault model, Cell-Aware Test**

I. Introduction

One of the major challenges with advanced integrated circuits is the high percentage of defects that escape traditional testing methods. The more commonly used test methods rely on fault models such as stuck-at and transition fault delay and produce test sets for deployment using Automatic Test Equipment (ATE). This approach reduces the need for functional testing of the manufactured IC at the system level and the accompanying test costs. It has been observed that structural testing using traditional fault models tends to be inefficient for screening defects. More complex fault models have been investigated in the past [1], [2], [3]. However, most methods require extensive circuit simulation for generating test pattern sets and are computationally expensive.

Imperfections in interconnect metal lines, missing contacts, imperfect vias and breaks in poly lines, etc., lead to open defects. Further, open and short defects can occur because of manufacturing imperfections within cells or across cells in a physical layout of the design. The traditional fault model for open defects considers opens at the Gate, Drain and Source terminals of transistors [4]. The commonly used fault model for short defects used in the past, considers shorts between the Gate-Drain, Gate-Source and Drain-Source terminals of a transistor [5]. The Gate Oxide fault model, used for short defects, considers an electrical connection between the gate of the transistor through the dielectric to the silicon surface of the CMOS [6]. In [7], analysis of the impact of body-biasing, supply voltage and temperature on the detection of short defects in FDSOI technology is presented.

It has been observed that certain values of partial open and short circuit defects can affect the propagation delay of standard cells [8]. The effect of a resistive short and resistive open in a CMOS standard cell is seen to be pattern dependent. Other techniques such as IDDQ testing have been very efficient in the detection of short defects [9] [10]. Very low voltage testing and higher than nominal voltage testing for shorts have been observed to improve the defect coverage for domino circuits as shown in [11] and [12]. The "Cell Aware" Test (CAT) methodology involves circuit simulation of open and short defects injected into the parasitic extracted netlists of standard cells to produce test pattern sets [13] [14]. The key contributions of this paper in relation to prior work are discussed next.

II. Key Contributions

The core contribution lies in a hierarchical testing approach in which: (a) multi-bit change and multi-pattern tests for embedded cells in a design targeting complete as well partial open and short defects are generated via cell-level simulation experiments and (b) the generated multi-pattern test are applied to embedded standard cells in design partitions using standard scan based DFT infrastructure. The core innovations in each of (a) and (b), above are described below.

(a) Synthesis of multi-bit change, multi-pattern test stimulus: The need for multi-bit change and multi-pattern tests to detect open defects of different sizes within standard cell instances in a design partition has been studied in [15]. The current work extends this approach to short defects within standard cells. Circuit simulations are used to demonstrate that certain

partial and complete short circuit defects within standard cells can go undetected with existing test methods. There are certain short defects which require more than 2-time frame or multi-bit switching test patterns or both for their detection. Standard cells from a 45nm library [16] were used for these experiments. Using these simulations and analysis, a suite of *multi-bit change and multi-time frame test patterns* with comprehensive coverage of complete and partial short defects within standard cells is identified.

(b) Generation of scan test vectors using combinations of launch-on-capture and launch-on-shift: The current work also proposes an ATPG method to generate scan test vectors for a full-scan sequential design containing standard cell instances, such that those scan test vectors provide the above-mentioned multi-bit change and multi-time frame test stimuli to the inputs of standard cell instances in that design to target open and short defects within those standard cell instances. A SAT-based ATPG formulation of the test generation problem is proposed. This approach enables generation of scan tests applicable through different combinations of capture followed by launch-on-capture (C_LOC), capture followed by launch-on-shift (C_LOS), shift followed by launch-on-shift (S_LOS) and shift followed by launch-on-capture (S_LOC) test application methods. The overall test generation flow is shown in Figure 1. To the best of our knowledge, this is the first time combinations of capture (C), shift (S), launch-on-capture (LOC) and launch-on-shift (LOS) methods have been explored in the literature. This scan test generation methodology is used to target both open and short circuit defects within standard cell instances. For this reason, we include the results on cell input stimuli identified for open defects from [15] as reference.

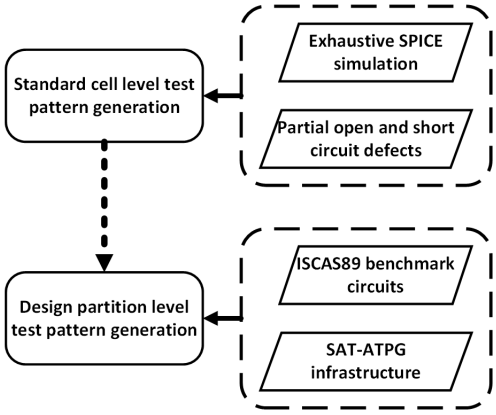

Fig. 1: Test Generation Flow

The rest of this paper is organized as follows, Section III presents the motivation along with preliminary results. Simulation driven cell level test generation is described in Section IV. Experimental setups and simulation studies are also discussed in this section. The design partition level test generation methodology is presented in Section V with the experimental setup and the proposed SAT-ATPG based approach. In Section VI experimental results are presented followed by conclusions.

III. Motivation

We first discuss our motivation for synthesizing multi-bit change and multi-pattern tests for high coverage of complete as well a partial opens and shorts in standard cell designs. First, likely defect locations for various open and short defects within a cell are identified using the extracted parasitic netlists and the prior silicon insight. After the identification of the defect locations, resistors which emulate open and short circuit defects are simulated, one at a time. Each injected resistor with its corresponding resistance value is termed as open or short circuit $defect$. Using exhaustive analog circuit simulations, each cell input stimuli that detect at least one defect (cause a cell-internal defect to be observed as an erroneous value at the cell's output) is identified. Subsequently, the identified cell input stimuli and it's accompanying erroneous cell-output value are then used as excitation and propagation conditions, respectively, to generate scan test vectors for designs containing instances of those cells.

For cell level identification of test conditions for defect detection at the cell output, the input stimuli can be either DC, 2-time frames or multi-time frames. For identifying the test conditions for various defects in an n-input cell, the cell is first characterized with 2^n combinations of DC input patterns. The defects that escape the DC tests are subjected to 2-time frame input stimuli for detection. The number of exhaustive 2-time frame input stimuli for an n-input cell is $2^{2n} - 2^n$ (without repetitions). However, the current methods in practice, because of the high simulation overhead, use only a subset of such combinations with only one-bit change in the second time frame, which results in $n \times 2^n$ ($<< 2^{2n} - 2^n$ for large n) patterns. Also, current methods in practice consider only extreme values of resistance for open and short circuit defects and not the partial defect sizes to reduce the simulation overhead (though the capability of simulating various defect sizes is available in the tools).

For resistive open and short defects, the behaviour of partial defect sizes is not fully captured in the analysis of extreme opens and shorts. The current traditional test methods are therefore not sufficient for detection of partially open and short defects. In this research, we classify 2-time frame test pattern vectors in four categories for cell delay characterization in the format $\{V_0,V_1,V_2\}$ where V_0 is the initialization vector which is applied before the application of the 2-time frame vectors V_1 and V_2. V_0 can have all possible (exhaustive) combinations. V_1 and V_2 are the first and second time frame vectors, respectively. For example, for a 2 input standard cell with inputs A and B, the 2-time frame vector will be $\{A_0B_0,A_1B_1,A_2B_2\}$. The different categories of 2-time frame test patterns used in this work are described as follows:

(a) *Single Bit Same Initialization* (SBSI): These patterns have single bit change from V_1 to V_2 with V_0=V_1, e.g. $\{V_0,V_1,V_2\}$=$\{00,00,01\}$. These tests are referred to as SBSI, which is prevalent with existing CAT practice.

(b) *Single Bit Different Initialization* (SBDI): These patterns have single bit change from V_1 to V_2 with $V_0 \neq V_1$, e.g.

$\{V_0,V_1,V_2\}=\{01,00,01\}$. These tests are referred to as SBDI. (c) *Multi Bit Same Initialization* (MBSI): These patterns have multi-bit change from V_1 to V_2 with $V_0=V_1$, e.g. $\{V_0,V_1,V_2\}=\{11,11,00\}$. These tests are referred to as MBSI. (d) *Multi Bit Different Initialization* (MBDI): These patterns have multi-bit change from V_1 to V_2 with $V_0 \neq V_1$, e.g. $\{V_0,V_1,V_2\}=\{10,00,11\}$. These tests are referred to as MBDI.

We expand our analysis to multi-time frame patterns (MTF) where patterns are of type: $\{V_0,V_1,V_2,V_3\}$ where V_0, V_1 and V_2 are the same as vectors in 2-time frame test and V_3 is the third time frame vector. For example, $\{00,01,00,11\}$. It should be noted that for the design partition level analysis and from a ATPG scan perspective the category of input stimuli with $\{V_0,V_1,V_2\}$ (2-time frame pattern with initialization vector) is a 3-time frame test pattern and $\{V_0,V_1,V_2,V_3\}$ (3-time frame with initialization vector) is a 4-time frame test pattern. Also, the patterns with same initialization (SBSI and MBSI) can be applied using both 2-time frame and a 3-time frame ATPG scheme.

The pie chart in Figure 2 shows combined defect coverage of open and short defects in gate AND3_X2 over different defect sizes and locations within the standard cell. The AND3_X2 cell has ten MOSFETs, with the defect universe consisting of 390 (210 open & 180 short) defects. This includes 48 (18 open & 30 short) defects detected by DC analysis, 219 (162 open & 57 short) defects detected by SBSI patterns, 39 (14 open & 25 short) defects detected by SBDI patterns, 13 (9 open & 4 short) defects detected by MBSI patterns, 23 (2 open & 21 short) defects detected by MBDI patterns and 6 (1 open & 5 short) defects detected by MTF patterns as shown in the Figure 2.

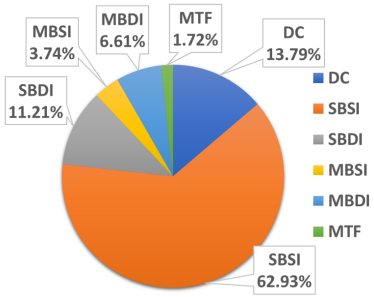

Fig. 2: AND3_X2 Defect Coverage

Resistive open circuit faults in the gate terminals of transistors are not detected by DC input stimuli. The 2-time frame and 3-time frame input stimuli are applied with exhaustive initialization conditions for exposing open and short circuit defects. It is seen that many defects require multi-time frame and multi-bit change test patterns over traditional 2-time frame single bit change test patterns for defect exposure.

The input stimuli identified for each cell are then used to generate scan test vectors for a design containing instances of these cells using the SAT-ATPG infrastructure discussed in Section V. Based on the pattern coverage obtained using SAT-ATPG and the pattern versus defect detection coverage

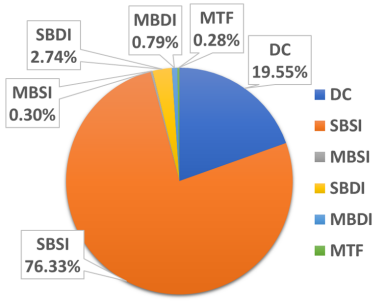

Fig. 3: Defect Coverage for s9234 benchmark circuit

obtained at the cell level, overall defect coverage for different types of multi-pattern tests is calculated and shown for the benchmark circuit s9234 in Figure 3. The total number of defects considered is the sum of the number of open and short defects *across all the physical cells in the design*. Different interleaved ATPG schemes using 3-time frame vectors are described in Section V. The comparison with traditional 2-time frame launch on capture (LOC) scan based test is shown in Figure 3. It can be seen that around 3.5-4% of total defects are exclusively detected by the multi-bit change or multi-time frame test patterns. Note that traditionally, defects not detected by 2-time frame LOC tests can result in test escapes.

In the following we first discuss cell-level test synthesis focusing more on partial short defects (since partial open defects were presented earlier in [15]), We then discuss the proposed SAT based ATPG methodology.

IV. Cell Level Test Synthesis Using Circuit Simulation

For SPICE simulation experiments, the 45nm digital standard cell library from Nangate [16] was used with a power supply of 0.8V. Using open and short circuit defects of varying sizes and at different locations, static and transition delay tests are performed on the parasitic extracted cell netlists using the HSPICE tool from Synopsys. Let a cell netlist have 'M' MOSFETs, 'C' parasitic capacitors, 'R' parasitic resistors, 'n' inputs and 'm' outputs. The open and short circuit fault model and testing experiments are discussed in the following:

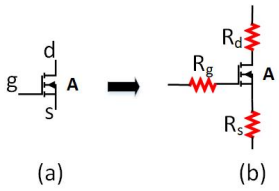

Fig. 4: Fault model for open defects.

Fault Injection: We use the following open and short circuit fault models for fault injection in the parasitic extracted netlists:

Open circuit defects: For open circuit defects, resistances of varying sizes are inserted at the Gate, Drain

and Source terminals of the MOSFETs, R_g, R_d and R_s respectively, as shown in Figure 4. The range of partial open resistances considered in this work consists of 7 defect sizes $\{1k\Omega, 5k\Omega, 10k\Omega, 50k\Omega, 500k\Omega, 500M\Omega, 1G\Omega\}$. The total number of defect sites therefore becomes 21*M.

Drain-Source faults (DS faults or leaky transistor faults): A resistive short fault (R_{ds}) is injected between the Drain and the Source terminals of each MOSFET, which can have 6 possible values $\{1k\Omega, 10k\Omega, 20k\Omega, 30k\Omega, 40k\Omega, 50k\Omega\}$, as shown in Figure 5(b). Thus, the defect universe for each cell with DS faults is 6*M.

Gate-Drain and Gate-Source faults (GD-GS faults): Two resistive short defects (R_{gd} and R_{gs}) are injected between the Gate and the Drain terminals and the Gate and the Source terminals of each MOSFET, which can have 6 possible values $\{1k\Omega, 10k\Omega, 20k\Omega, 30k\Omega, 40k\Omega, 50k\Omega\}$, as shown in Figure 5(b). Thus, the defect universe for each cell with GD-GS faults is 12*M.

Capacitance faults (Cap faults): A resistive short defect (R_{cap}) is injected between the terminals of each parasitic capacitance present in the netlist, which can have 4 possible values $\{1k\Omega, 20k\Omega, 40k\Omega, 50k\Omega\}$, as shown in Figure 5(a). Thus, the defect universe for each cell with Cap faults is 4*C.

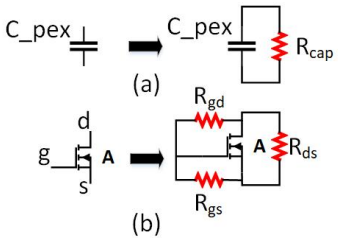

Fig. 5: Fault model for short defects.

Simulation test bench: Automatic fault injection of all the defects from the defect universe of each fault model was performed on parasitic extracted netlists of standard cells, with only a single defect present at a time. A fault free inverter is added to the output of the cell to pull up or pull down the intermediate analog values that may be produced due to the defect as shown in Figure 6. The output is measured at the output 1 and output 2 (both outputs are considered for defect detection). Three types of analysis are performed during circuit simulations. In each analysis, faulty and fault free output values are compared as explained in the following.

DC Analysis: Each cell is subjected to DC simulation for the fault-free and faulty netlist with exhaustive set of inputs (2^n n-bit vectors for each defect, in case of faulty netlist). The voltage is measured at both the outputs 1 and 2 and voltage values between 0V-0.1V are normalized to 0 (logic 0) and between 0.7V-0.8V are normalized to 0.8V (logic 1). From the analysis of the fault free netlist we obtain a "golden" truth table for DC stimuli. For the faulty netlist, the m-bit output vector for each input vector is compared with the corresponding m-bit output vector from the golden truth table and defect is

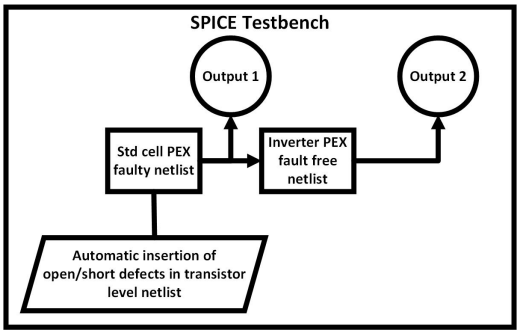

Fig. 6: Simulation testbench.

marked as detected if the fault-free output is different from faulty output at either output 1 or 2.

2-time frame analysis: Defects that are not detected in DC analysis are subjected to 2-time frame transient simulation along with fault free transient simulation for the exhaustive set of input vector patterns, of size $2^n \times (2^n - 1)$ (Note that application of identical vectors in consecutive time frames is equivalent to DC analysis; thus we do not consider them in 2-time frame analysis). Each input vector pattern from the exhaustive set is initialized with all possible initial conditions, resulting into $2^n \times 2^n \times (2^n - 1)$ simulation patterns denoted as $\{V_0, V_1, V_2\}$ where V_0 is the initial vector, V_1 is the first vector and V_2 is the second vector. 2-time frame analysis is done to analyze the delay characteristics of faulty netlist in comparison to delay characteristics of fault-free netlist.

For each two pattern test, as the input vector transits from V_1 to V_2, each output in the output vector will either rise (Out[V_1]=0 and Out[V_2]=1), fall (Out[V_1]=1 and Out[V_2]=0) or remain static ((Out[V_1]=0 and Out[V_2]=0) or (Out[V_1]=1 and Out[V_2]=1)). From the fault-free netlist for each output in the output vector (output 1) and the inverted output (output 2), the rise and fall delays due to each input pattern are measured and the maximum values of these is categorized as worst case rise delay (T_{r-max}) and worst case fall delay (T_{f-max}), respectively. Similarly, the output transition behaviour and delay for each output in the output vector (output 1) and the inverted output (output 2) is measured for each input vector applied to faulty netlist. First, the transition behaviour of each output is compared with the corresponding fault-free output behaviour for the same input pattern. In case of a mismatch in either output 1 or output 2, the defect is said to be detected. Else we determine if the transition delay impact of the defect exceeds the worst case nominal rise or fall delay by more than 20% depending on the transition behaviour. If this condition is satisfied for either output 1 or output 2, then the defect is said to be detected.

3-time frame analysis: Defects not detected in 2-time frames are then subjected to 3-time frame transient simulation with exhaustive set of input vector patterns ($2^n \times 2^n \times (2^n - 1)$ with all possible initial conditions, resulting in $2^n \times 2^n \times 2^n \times (2^n - 1)$ simulation patterns denoted as $\{V_0, V_1, V_2, V_3\}$ where V_0 is the initial vector and V_1, V_2 and V_3 are the first, second

TABLE I: Open defect detection by different input stimuli [15]

Cell	# of MOSFETs	Defects	DC	SBSI	SBDI	MBSI	MBDI	MTF
OR2_X1	6	126	16	85	4	4	4	7
OR2_X2	8	168	8	127	6	8	8	3
OR2_X4	16	336	-	208	28	49	13	9
OR3_X2	10	210	12	162	21	13	1	1
NOR3_X2	12	252	-	179	1	0	2	2
AND3_X1	8	168	20	125	6	3	5	4
AND3_X2	10	210	18	162	14	9	2	1
AND3_X4	20	420	-	353	19	33	6	7
AND2_X4	16	336	-	260	25	3	3	5
NAND2_X4	16	336	-	122	11	15	20	4
AOI21_X1	6	126	2	98	0	2	2	1
XNOR2_X2	16	336	16	177	1	3	2	3
HA_X1	16	336	60	180	8	10	5	27

TABLE II: Defect detection for DS faults and GD-GS faults

		DS faults							GD-GS faults						
Cell	**M**	**Defects**	**DC**	**SBSI**	**SBDI**	**MBSI**	**MBDI**	**MTF**	**Defects**	**DC**	**SBSI**	**SBDI**	**MBSI**	**MBDI**	**MTF**
AND2_X1	6	36	8	13	0	0	1	0	72	13	29	2	0	2	0
AOI21_X1	6	36	13	11	0	1	0	0	72	32	17	0	1	0	1
NAND2_X4	16	96	16	0	0	0	0	0	192	20	4	0	0	0	0
OR2_X2	8	48	10	12	0	2	0	2	96	22	28	0	2	5	5
AND3_X1	8	48	13	24	1	0	0	0	96	21	40	6	0	4	1
AND3_X2	10	60	10	19	7	0	15	0	120	20	38	18	4	6	5
AOI21_X2	12	72	16	16	0	6	0	1	144	36	24	0	16	5	1
NAND3_X4	24	144	12	12	0	0	12	0	288	20	16	0	0	11	5
OR3_X1	8	48	16	10	0	4	0	0	96	37	32	0	1	1	2
OR3_X2	10	60	12	16	2	0	12	3	120	28	50	0	1	2	22

TABLE III: Defect detection for capacitance shorts

Cell	C	Defects	DC	SBSI	SBDI	MBSI	MBDI	MTF
AND2_X1	38	152	12	11	20	0	1	0
OR2_X2	43	172	14	14	0	0	13	13
AND3_X1	53	212	25	55	0	1	0	1
AND3_X2	52	208	17	17	0	1	9	131
OR3_X2	53	212	18	52	0	2	3	9

and third vectors, respectively). The simulation procedure is similar to that of 2-time frame analysis. The output transition behaviour and delay are measured at outputs 1 and 2 for an input transition from V_2 to V_3 and defect detection is performed in the same manner as for 2-time frame analysis. 3-time frame analysis is performed to analyze the increased defect coverage by applying multi-time frame test.

Classification of simulation results: The objective of these experiments is to demonstrate the need for multi-bit change and multi-time frame tests for increasing defect coverage. It is observed that as the complexity of the test increases from DC to 3-time frame more defects are covered. Thus, each defect is characterized as uniquely detected by DC, SBSI, SBDI, MBSI, MBDI or MTF.

Circuit simulation results: For each of the fault models, the defects not detected in DC analysis are simulated for 2-time frame input pattern, which can be of 4 types: SBSI, SBDI, MBSI and MBDI. The defects not detected in 2-time frames are simulated for 3-time frame input pattern (MTF). The results obtained from the exhaustive simulations are shown in Table I for opens [15] and Table II for shorts.

Column 1 of Table I shows the names of the standard cells. Column 2 shows the total number of MOSFETs in the cell. Column 3 shows the defect universe for each cell. Column 4 shows the defects detected by DC test patterns. Columns 5, 6, 7 and 8 show open defects that are detected by the SBSI, SBDI, MBSI and MBDI patterns, respectively. Column 9 shows the open defects which are only detected by multi-time frame test patterns.

In Table II, column 1 shows the cell under observation, column 2 shows the number of MOSFETs present in the cell, column 3 and column 10 show the total defect universe for the DS fault model and the GD-GS fault model, respectively. Column 4 and column 11 show the number of defects detected by DC analysis for each of the fault models. The defects that escape DC detection but are detected by SBSI input patterns are shown in column 5 and column 12. Similarly, the SBDI, MBSI, MBDI and MTF input pattern detected defects are shown in column 6, 7, 8 and 9, respectively, for the DS fault model and in column 13, 14, 15 and 16, respectively, for the GD-GS faults. As can be seen from Table I and Table II, there are on average approximately 3% open circuit defects and approximately 2.5% short circuit defects that escape the DC or traditional 2-time frame test condition (SBSI) and are detected by either multi-bit change and multi-time frame patterns. This necessitates the need for multi-bit change and multi-time frame patterns for detecting additional defects and increasing the defect coverage.

For the parasitic capacitance fault model (Cap faults), it

is observed through exhaustive simulation that only defects located at the output of either a logic stage or an internal node of the cell are detectable by DC, SBSI or SBDI patterns and are equivalent to node stuck-at-0 fault. Defects at locations other than these are detectable only by MBSI, MBDI or MTF analysis. Additionally, it is observed that a large majority of defects are detected by DC or SBSI tests, with a few exceptions, some of which are shown in the Table III.

The cell input stimuli identified using circuit simulation for the different cells is used for scan test generation for a design that contains instances of these cells. The next section presents the SAT-ATPG methodology proposed for scan test generation.

V. SAT-ATPG methodology for scan test generation

The need to generate high coverage scan vectors for a design (or design partition) such that these tests can apply multi-bit change and multi-time frame patterns at the inputs of its cell instances led us to explore non-traditional test application approaches. These new schemes flexibly interleave shift cycles and capture cycles, as needed, during the multi-time frame test to maximize test coverage. Recall that changing the scan flip-flops from the scan shift mode to functional capture mode, or vice versa, during successive test cycles requires switching the global scan-enable signal. Many designs do not support a high speed scan-enable that can reliably change the mode of all the scan flip-flops within the same high speed functional clock cycle. Such designs must therefore hold the scan-enable signal stable between the test launch and capture clock edges of a two-pattern timing test. Since this must be in the capture mode to latch in the functional response, this is called the launch-on-capture (LOC) timing test. Launch-on shift (LOS) tests are further supported only by designs with an at-speed scan-enable. Note however that in the multi-time frame tests that are of interest in this paper, circuit timing is only tightly controlled while detecting the target defect in the last time frame. The earlier time frames are used to initialize the circuit to ensure worst case conditions that maximize delay due to the defect in this final time frame. Consequently, the needed multi-time frame initialization using ATPG generated patterns can be performed during the much slower scan shift cycles. Only the final launch and capture clock edges in the last time frame must conform to the fast functional clock period, exactly as in traditional timing tests. Using the slow scan clock for all except the final time frame in the multi-pattern tests can also allow sufficient time for switching the scan-enable within these clock periods, and thereby support any mix of shift (S) and capture (C) cycles during initialization for all designs. Only the final at-speed functional cycle is limited to LOC in the multi-pattern tests if an at-speed scan enable is not implemented in the design.

A. SAT-ATPG Background

SAT solvers have been known to be effectively used to overcome the challenges related to test quality requirements and ATPG effectiveness [17] [18] [19]. This work uses the power of SAT solvers for the ATPG problem. The test circuit is transformed into a conjunctive normal form (CNF) Boolean expression consisting of consistency checks for every gate along with the additional constraints. There has been a significant amount of work that has been done to improve the efficiency of SAT-ATPG approach [20] [21] [22] [23] [24] [25] [26]. For these reasons, a SAT-based ATPG formulation is used for scan test generation in this work. While the traditional scan test generation is implemented based on 2-time frame Launch on capture (LOC) or a Launch on shift (LOS) ATPG scheme, our approach extends that to allow for interleaved LOC and LOS. Because our focus is (small) timing defects, we assume that the defect is only activated during the final, at-speed, cycle of the multi-pattern test. All earlier (initialization) time frames that employ the much slower scan clock are assumed to be fault free.

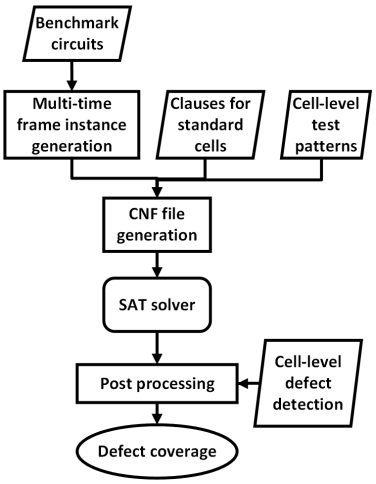

Fig. 7: SAT-ATPG flow

B. SAT-ATPG Architecture

The SAT-ATPG infrastructure is developed using the open source MiniSat SAT solver [27]. Figure 7 shows the overall SAT-ATPG flow. The ISCAS89 benchmark circuits [28] are used as the test cases. In the benchmark circuits, we replace all 4-input gates with 2-input gates and 3-input gates (since exhaustive SPICE simulation is performed for up to 3-input gates in our work). For example, OR4 is replaced with OR2 and OR3, NAND4 is replaced with AND3 and NAND2. We assume that all the flip-flops present in the benchmark circuits are scannable and observable. For each benchmark circuit, multiple instances of the circuit are created based on the number of time frames required. In addition, a faulty instance of the circuit is generated and connected to a XOR gate along with the fault free circuit to make sure that the fault is propagated to the output. The inputs of the gate to be tested are constrained to the pattern to be applied and its output in the faulty instance is constrained to the faulty value for that gate. A library of clauses for each gate is created and then used to create a Boolean expression for the benchmark circuit. Once the CNF representation of the circuit is generated, the

complete Boolean expression is fed to the SAT solver. The SAT solver outputs whether there is a possible solution and if so, what are the primary input (PI) values for different time frames and the initial scan chain values. This process is performed for all the instances and all the defects. Once the SAT solver output is available, the result is analysed to obtain the pattern coverage. From the cell level test identification as explained in Section IV, the test pattern set versus the defects detected is available. Using pattern coverage knowledge at the design partition level and the test conditions identified at the cell level, the overall defect coverage is obtained for the circuit level.

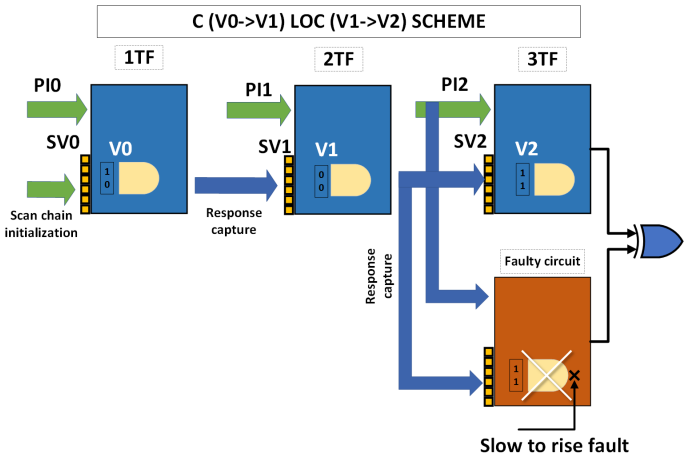

Fig. 8: C_LOC SAT-ATPG Methodology

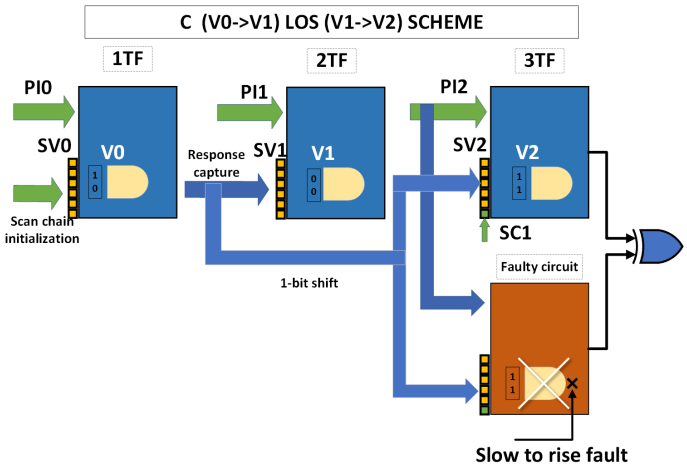

Fig. 9: C_LOS SAT-ATPG Methodology

C. SAT-ATPG Test Schemes

The following capture (C), shift (S), LOC and LOS interleaving schemes are developed for finding the defect coverage gain using 3-time frame patterns over 2-time frame patterns. We investigate 4 different interleaving schemes for 3-time frame analysis as illustrated in Figure 8-11. Consider an example of a cell level pattern $\{V_0,V_1,V_2\}=\{10,00,11\}$ that is required to be applied at the circuit level. The three fault free instances of the circuit, represented by blue blocks, are generated for three time frames, respectively. A faulty instance, represented by orange block, is generated for the third time frame and connected to the XOR gate for the fault propagation check. The green arrows represent the primary input values and initial scan chain values solved by the SAT solver, whereas the blue arrows represent the wire connections. The inputs of gate in different instances are constrained to the pattern $\{10,00,11\}$ and the output in the faulty gate is constrained to 0, representing the slow to rise fault. In all schemes, SV_0 is scanned into the flip-flips as scan chain initialization. SV_1 and SV_2 are applied based on the scheme, which will be explained as follows.

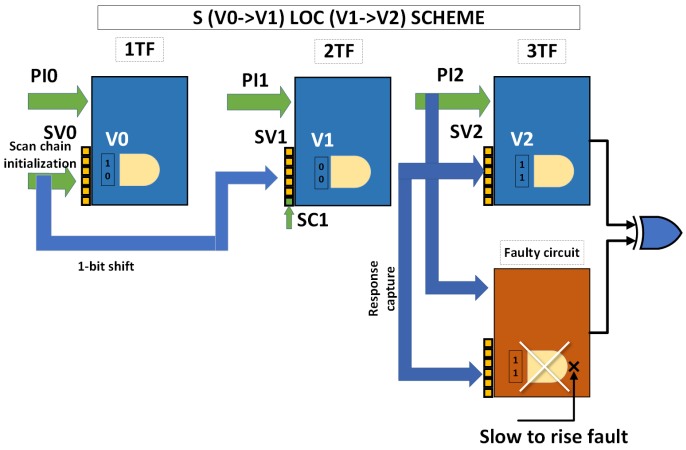

Fig. 10: S_LOC SAT-ATPG Methodology

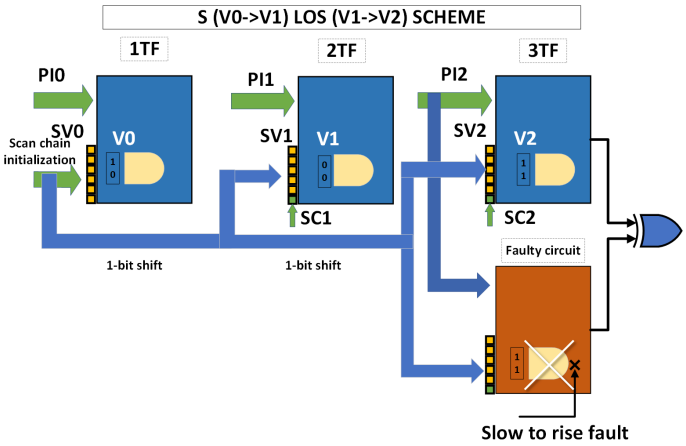

Fig. 11: S_LOS SAT-ATPG Methodology

Capture_LOC scheme (C_LOC): In this scheme, both SV_1 and SV_2 are applied by capturing the circuit's response. As shown in Figure 8, SV_1 is the circuit's response to PI_0 and SV_0 captured in the scan chain. Similarly, SV_2 is the circuit's response to PI_1 and SV_1 captured in the scan chain.

Capture_LOS scheme (C_LOS): In this scheme, SV_1 is applied in the same way as that for the C_LOC scheme, while

SV_2 is applied by shift of the scan chain. As shown in Figure 9, SV_2 is the 1-bit shift of SV_1. The 1-bit input to scan chain is added to the second time frame circuit instance, which is also solved by the SAT solver.

Shift_LOC scheme (S_LOC): Similar to C_LOS scheme, this scheme also adopts the interleaved technique. As shown in Figure 10, SV_1 is the 1-bit shift of SV_0, whereas SV_2 is the circuit's response to PI_1 and SV_1 captured in the scan chain.

Shift_LOS scheme (S_LOS): In this scheme, both SV_1 and SV_2 are the 1-bit shift of the previous vector. As shown in Figure 11, SV_1 is the 1-bit shift of SV_0 and SV_2 is the 1-bit shift of SV_1. Two 1-bit inputs to scan chain are added to the second and third time frame circuit instances, respectively.

VI. Experimental Results

Experiments were performed on all of the ISCAS89 benchmark circuits with the SAT-ATPG infrastructure described in Section V. Pattern coverage for the circuit level is obtained by the analysis of the SAT solver output for all the DC, 2-time frame and 3-time frame test patterns for all the instances of standard cells. The pattern versus defect detection matrix obtained during the cell level characterisation is used to calculate the defect coverage at the circuit level (defect universe consists of all defect sizes and locations for all instances). The analysis for open defect coverage for circuit s13207 is shown in Table IV. The total defect coverage using the traditional 2-time frame LOS scheme is 59.81% with the increment of 0.12% with 2-time frame multi-bit change patterns as shown in row 2 of Table IV. The increment in defect coverage gain for each individual 3-time frame interleaved C/S and LOC/LOS ATPG scheme is shown in rows 3, 4, 5 and 6. Each scheme shows successive incremental gain in defect coverage for different categories of patterns. For C_LOC scheme the total defect coverage gain is ≈8% over the 2-time frame LOS scheme.

Table V shows similar analysis for open defect coverage gain with respect to the traditional 2tf LOC scheme. The overall defect coverage gain obtained by 2-time frame LOC scheme is 59.63% and the total incremental coverage gain by the 3-time frame S_LOS scheme is ≈9.5%. Similar analysis is done for various benchmark circuit for open and short defects. Figure 12 shows the defect coverage gain for open defects which can be obtained using different interleaved LOC and LOS schemes over the the traditional 2-time frame LOS scheme. It can be seen that the improvement of 0.9% to 8% defect coverage gain for different benchmark circuits can be achieved using 3-time frame ATPG schemes. Similar analysis is done for observing defect coverage gain of open defects over traditional 2-time frame LOC scheme as shown in Figure 13. The defect coverage gain of 1% to 13% for different benchmark circuits is achieved for different benchmark circuits using 3-time frame ATPG schemes.

Similar observations are shown for short defect coverage analysis. The defect coverage gain for DS short defects is shown in Figure 14, ranging from 0.1% to 2.6% for different benchmark circuits over traditional 2-time frame LOS ATPG Scheme. Figure 15 shows coverage gain for DS short defects

TABLE IV: Opens Defect analysis for circuit s13207 w.r.t 2TF LOS

	SBSI	MBSI	SBDI	MBDI
LOS	59.81%	+0.12%	NA	NA
C_LOC	+6.07%	+1.43%	+0.09%	+0.08%
C_LOS	-	-	+0.92%	+0.07%
S_LOC	+1.86%	+1.70%	+.08%	+0.08%
S_LOS	-	-	+1.39%	+0.08%

TABLE V: Opens Defect analysis for circuit s13207 w.r.t 2TF LOC

	SBSI	MBSI	SBDI	MBDI
LOC	59.63%	+0.33%	NA	NA
C_LOC	-	-	+1.43%	+0.08%
C_LOS	+5.22%	+0.92%	+0.02%	+0.07%
S_LOC	-	-	+1.70%	+0.08%
S_LOS	+8.01%	+1.40%	+0.04%	+0.08%

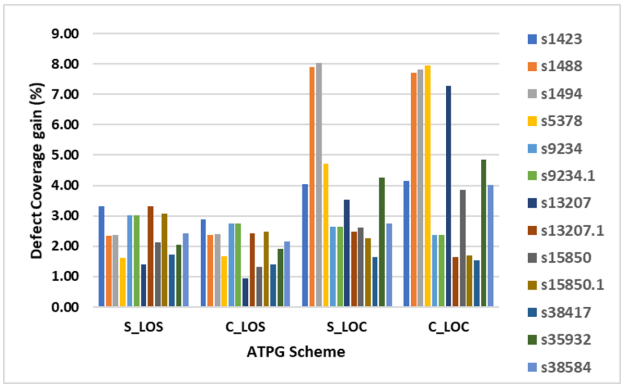

Fig. 12: Open Defect Coverage Gain over 2TF LOS

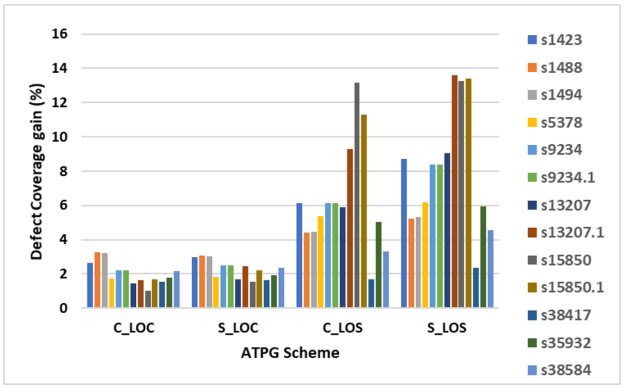

Fig. 13: Open Defect Coverage Gain over 2TF LOC

ranging from 0.1% to 2.4% for different benchmarks over traditional 2-time frame LOC ATPG scheme. The coverage gain for GD-GS short defects is shown in Figure 16, ranging from 0.7% to 7.1% over 2-time frame LOS scheme and Figure 17 , ranging from 0.9% to 8% over 2-time frame LOC scheme.

The defect coverage gain analysis was performed for DC and multi-time frame test patterns as well. The SAT-ATPG experiments were performed for DC test patterns for all instances in the benchmark circuits. Pattern coverage infor-

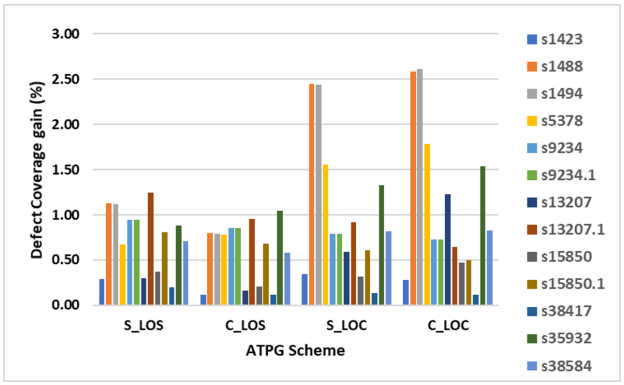

Fig. 14: DS Shorts Defect Coverage Gain over 2TF LOS

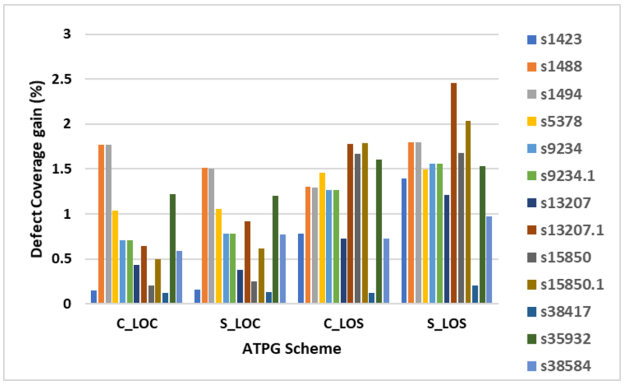

Fig. 15: DS Shorts Defect Coverage Gain over 2TF LOC

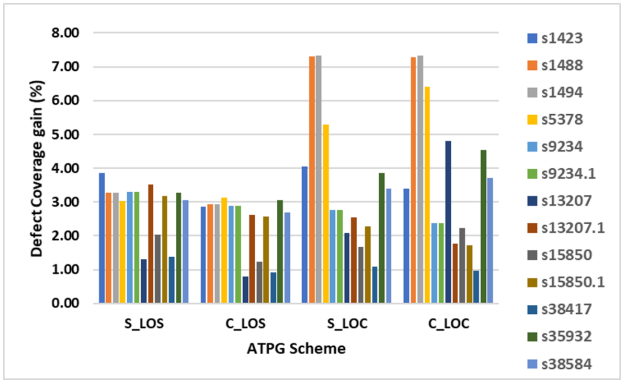

Fig. 16: GDGS Shorts Defect Coverage Gain over 2TF LOS

mation obtained from the SAT solver is translated to calculate the % of faults covered at the circuit level with respect to the faults covered at the cell level. As shown in column 2 of Table VI, the defects covered by DC patterns at circuit level versus cell level are ≈97% on average.

The 3-time frame analysis was further extended to 4-time frames, experiments with different combinations interleaved LOC and LOS SAT-ATPG schemes were performed. The possible combinations of ATPG schemes can be X_Y_Z where X,Y and Z can either LOC or LOS. The average number of multi-time frame defects detected are shown in column 3 of Table VI. The average % of MTF faults covered by the 4-time frame ATPG scheme are shown in column 4. Similar trend is

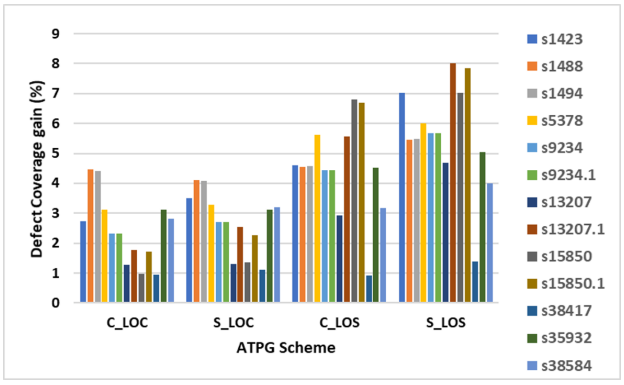

Fig. 17: GDGS Shorts Defect Coverage Gain over 2TF LOC

observed for short defects.

TABLE VI: DC and MTF Open Defect analysis

Benchmark	DC def. covered	MTF def. detected	MTF def. covered
s1423	99.17%	321	76.85%
s1488	100%	197	28.67%
s1494	99.63%	202	28.81%
s5378	97.66%	263	40.40%
s9234	93.46%	468	33.09%
s9234.1	93.46%	468	33.09%
s13207	98.14%	255	15%
s13207.1	98.14%	523	30.68%
s15850	96.88%	416	18.99%
s15850.1	96.88%	416	18.99%
s35932	94.44%	1152	33.33%
s38417	99.56%	628	70.09%
s38584	96.10%	2670	30.67%

Another key observation from this work is shown in Tables VII and Table VIII. We analyse the different defects detected by the individual 3-time frame interleaved ATPG schemes. We further divide them based on the common defects and the exclusive defects detected between the schemes. It can be seen that the different combinations of LOS and LOC schemes are able to exclusively detect a number of defects which are not detected by other schemes and this is shown in columns 3, 4, 5 and 6. Column 2 shows the common defects detected between all the schemes. Similar trend has been observed for short circuit defect analysis.

TABLE VII: LOC 2TF Opens Defect analysis

Benchmark	Common defects	C_LOC	C_LOS	S_LOC	S_LOS
s1423	2.44%	0.21%	3.67%	0.54%	6.24%
s1488	1.53%	1.72%	2.90%	1.52%	3.72%
s1494	1.54%	1.70%	2.93%	1.51%	3.80%
s5378	1.42%	0.31%	3.95%	0.40%	4.78%
s9234	2.13%	0.07%	4.01%	0.38%	6.26%
s13207	0.52%	0.90%	5.38%	1.16%	8.51%
s13207.1	1.61%	0.02%	7.65%	0.84%	11.97%
s15850	0.78%	0.21%	12.37%	0.78%	12.49%
s15850.1	1.63%	0.03%	9.66%	0.60%	11.75%
s35932	1.40%	0.14%	0.28%	0.24%	0.96%
s38417	1.39%	0.38%	3.63%	0.51%	4.54%
s38584	1.90%	0.24%	1.42%	0.47%	2.63%

From the above results, it can be seen that there are certain open and short defects which need multi-time frame patterns for their detection and for these patterns to be applied at the circuit level, there are different interleaved ATPG choices

TABLE VIII: LOS 2TF Opens Defect analysis

Benchmark	Common defects	C_LOC	C_LOS	S_LOC	S_LOS
s1423	2.44%	1.69%	0.42%	1.59%	0.86%
s1488	1.53%	6.16%	0.85%	6.35%	0.81%
s1494	1.54%	6.28%	0.86%	6.48%	0.82%
s5378	1.42%	6.52%	0.24%	3.29%	0.19%
s9234	2.13%	0.22%	0.60%	0.51%	0.88%
s13207	0.52%	6.74%	0.40%	3.00%	0.87%
s13207.1	1.61%	0.02%	0.80%	0.85%	1.69%
s15850	0.78%	3.05%	0.53%	1.83%	1.34%
s15850.1	1.63%	0.06%	0.84%	0.61%	1.42%
s35932	1.40%	0.14%	0.014%	0.24%	0.34%
s38417	1.39%	3.45%	0.51%	2.85%	0.65%
s38584	1.90%	2.11%	0.24%	0.85%	0.51%

available and each scheme can achieve different defect coverage. The defect coverage gain by multi-time frame patterns is more when compared against 2-time frame LOC scheme as can be seen from Figure 13, 15, 17 and Table VII. More importantly each scheme may detect a unique set of defects which escape the other schemes.

VII. Conclusion

Using exhaustive SPICE simulation, we show that there exist partial open circuit and short circuit defects of different sizes within standard cells that require multi-bit change and multi-time frame input stimuli for their detection. A hierarchical test generation approach is developed that permits significant coverage improvements of such defects in embedded standard cells of complex sequential logic designs when the tests are applied through standard scan DFT infrastructure. The test generation approach exploits combined use of an interleaved capture, shift, launch-on-capture and launch-on-shift multi-pattern test application strategy. A SAT based test generation approach is used to facilitate such multi-pattern scan-enabled test application. It is observed that a fraction of defects are exclusively detected by the multi-time frame test patterns thus justifying use of the proposed test approach.

Acknowledgment

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