An Interleaved Multi-Phase Boost Converter with Coupled Inductors for High Power Density

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***Abstract*— To reduce the size of passive components, especially the magnetics, is one of the major challenges of boost converters operating in continuous conduction mode. This can be addressed by increasing the switching frequency, which however is infeasible in high power applications. This paper presents an interleaved multi-phase boost converter utilizing the six-pack silicon carbide (SiC) power module as a single-phase building block to triple the ripple frequency of the inductor current at the same switching frequency, hence, reducing the size of passives by three-fold and achieving higher power density while improving performance and maintaining high efficiency. In addition, planar inversely coupled inductors were designed to further decrease the inductor size and to improve the steady-state and transient performance of the boost converter. The analysis and hardware design of the converter are presented in this paper with the experimental results at full load presented to validate the effectiveness of the proposed design.**

Keywords—Boost converter, coupled inductor, interleaving, power density.

I. INTRODUCTION

There is a consistent demand for efficient, high power density, reliable DC-DC converters for a wide variety of applications. In high power applications, e.g., over 50kW rated power, the interleaved boost converter is an effective solution due to its advantages such as enhanced efficiency, modularity and reduced input and output ripples. Moreover, by distributing load current over interleaved phases, the enhanced thermal performance, higher power density, and lower EMI can be attained. The emerging SiC power devices can enable high power density, high performance converters. Compared to their silicon counterparts, the high switching frequency at low switching losses brought by SiC devices make it possible to reduce the size of the passives. In addition, the ability to operate at higher temperature alleviates the cooling requirements, which leads to further volume reduction of the power stage. However, in the SiC high-power boost converters [1], inductors and their cooling systems can still be bulky and difficult to design.

To achieve high power density, operating the converter at higher switching frequency is an effective approach, which reduces the size of the passive components and improve the performance by reducing the current ripple. For high power applications, the switching frequency is limited by the switching losses, the maximum power dissipation of the power module package, and effectiveness of the thermal management.

Several solutions were proposed to minimize the passive components size. Very high switching frequency has been used in [2] and [3] to miniaturize the inductor. However, the switching losses can be excessive when using this method in high power applications. Paralleling the semiconductors is another option such as in [4] and [5]. However, evenly sharing the current among the switches can be a challenging task. The current mismatch can lead to unbalanced distribution of losses among the switches, which further decrease the converter reliability. Soft switching techniques can enable high switching frequencies with lower losses. This can be achieved by operating in the discontinuous conduction mode (DCM) [1] or using soft-switching cells [6]. In DCM, the converter is subject to higher current stresses and higher ripples. In addition, the switching frequency is limited by the inductor losses, especially if the inductor core is non-ferrite which is usually the case for high currents. Soft switching cells can be an effective solution to increase the switching frequency [6] if the extra components and associated controls do not complicate the system nor affect the volume of the converter. An alternative solution is to indirectly increase the inductor ripple frequency using a lower switching frequency instead of direct increasing the switching frequency. A multi-device interleaved boost converter topology is proposed in [7], which doubles the inductor ripple frequency using the same switching frequency. Similarly, [8] uses a configuration of three inductors to further increase the inductor ripple frequency. In these designs, the switching losses are distributed among the parallel semiconductor devices, hence simplifying the thermal management of the converter while reducing the volume of the passive components due to the increased effective frequency without the need for current balancing among parallel switches.

In this paper, a high-power density, high performance boost converter design is presented. A four-phase interleaved boost topology is selected with a six-pack SiC power modules used in each phase, tripling the inductor current ripple frequency while keeping the same switching frequency. In addition, coupled inductors were designed to further reduce the volume of the inductors and enhance the performance by reducing the flux in the cores. The steady state analysis is presented, and the

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converter design is discussed. A 50kW prototype was built to verify the proposed concepts and the results are shown.

II. The Proposed Converter

Achieving high power density while maintaining a good efficiency and thermal stability are the main technical targets. Since no isolation is required, an interleaved boost operating in the continuous conduction mode (CCM) under hard switching is very efficient to convert a wide input voltage to a constant output voltage [5]. CCM allows the ripples to be lower, which enhances the overall performance of the converter. However, hard switching CCM limits the switching frequency for high power applications due to increased switching losses.

A. Circuit Configuration

The proposed bidirectional four-phase interleaved boost converter is shown in Fig. 1. An input capacitor C_{in} is connected in parallel to the input stage supplying total current I_{in} to four inductors. Each inductor is connected to a boost phase which is comprised of a parallel-connected six-pack SiC power module. The four phases are then connected to the output capacitor C_{out} to filter the output voltage V_{out} connected to the load drawing a current I_{out}.

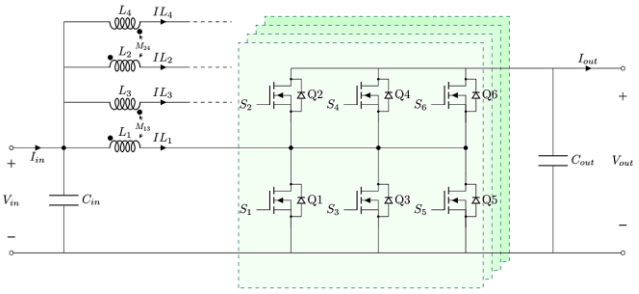


Fig. 1. Circuit diagram of the proposed converter

B. Operating Principles and Driving Scheme

Fig. 2 shows the theoretical steady state waveforms of the interleaved boost under CCM operation. The main switches of a single phase, i.e., Q1, Q3 and Q5, are switched with a 120° (360°/m) phase shifted PWM with a switching frequency f_{sw} and 30° (360°/(n×m)) phase shift among the interleaved phases, where n and m are the number of phases and the number of legs in each phase, respectively. Table I summarizes the phase shift relations between the different switches. All the main switches have the same duty cycle D, and the synchronous switches, i.e., Q2, Q4 and Q6, are driven in complementary mode with duty cycle D', where D'= (1/m–D). During the dead time period, the body diodes of the three synchronous switches share the inductor current and lead to zero-voltage turn-on for the synchronous switches which help reduce the switching losses since the synchronous switches turn on at peak inductor current. As shown in Fig. 2, the driving sequence triples (m times) the ripple frequency of the inductor current and increase the input/output ripple frequencies by 12 (n×m) folds. This significantly reduces the size of the passive components and hence increase the power density. Moreover, the losses are distributed over a larger number of devices and modules, which simplifies the design for thermal management considerably.

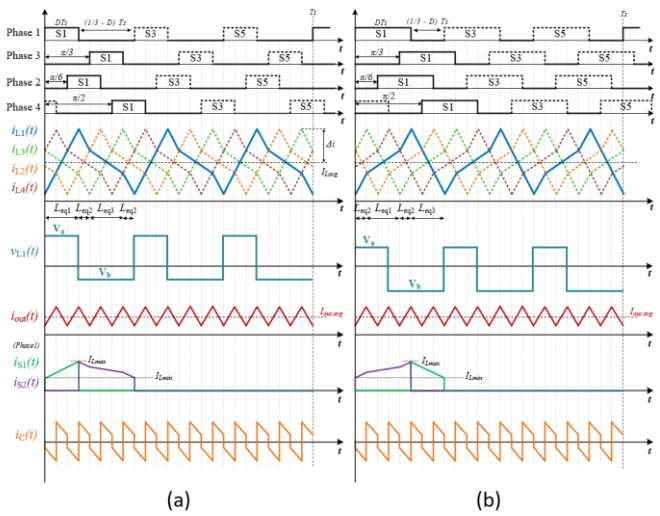


Fig. 2. Ideal steady-state waveforms of the proposed boost converter in CCM operation for (a) $D < 0.5/m$ (b) $D > 0.5/m$

TABLE I. PHASE SHIFT PATTERN FOR N = 4, M = 3

Phase	Switch PWM Signal		
	S_1	S_3	S_5
1	0°	120°	240°
2	30°	150°	270°
3	60°	180°	300°
4	90°	210°	330°

From Fig. 2 and over a time period of T_s/m, where $T_s = 1/f_{sw}$ the following relation can be derived according to the inductor voltage-second balance:

$$V_a D T_s + V_b D' T_s = 0 \tag{1}$$

Neglecting the inductor coupling effect yields V_a=V_{in} and V_b = V_{in} – V_{out}. Then the voltage conversion ratio M can be written as:

$$M = \frac{V_{out}}{V_{in}} = \frac{1}{1-mD} \tag{2}$$

And the maximum theoretical duty cycle is then D= 1/m.

From the inductor current slope, and neglecting the effect of coupling for the moment, the minimum self-inductance required to maintain a ripple current $\Delta i = r_I \cdot I_L$ can be derived as:

$$L \geq \frac{V_{in}\left(1-\frac{V_{in}}{V_{out}}\right)}{2 \cdot r_I \cdot I_L \cdot m \cdot f_{sw}} \tag{3}$$

The output capacitance can be initially estimated from the required voltage ripple $\Delta V_{out} = r_v \cdot V_{out}$, given a load R, from:

$$C_{\text{out}} \geq \frac{V_{in}\left(1-\frac{V_{in}}{V_{out}}\right)}{2 \cdot r_v \cdot V_{out} \cdot R \cdot n \cdot m \cdot f_{sw}} \tag{4}$$

From (3) and (4) it is seen that L and C_{out} requirements are significantly reduced by a factor of m compared to an equivalent conventional interleaved boost converter.

The value of C_{in} is less critical in the boost converter, but it can be estimated for the worst-case ripple, i.e., when only one phase is active, as [2]:

$$C_{in} \geq \frac{L\cdot(I_{L.peak}^2 - I_{L.min}^2)}{V_{in.max}^2 - V_{in.min}^2} \tag{5}$$

C. Coupled Inductor Effect on Converter Operation

Since there are four phases in total, the phase shift between the inductors currents is 90°. Therefore, inductors of phases 1 and 3 are coupled together on one core, the same for inductors of phases 2 and 4. This maintains a 180° phase shift between the inductor currents on the same core and maximizes the flux cancelation effect, hence reduces the core losses and increases the saturation point. The interactions between the inductor currents coupled on the same core will alter the voltages applied on each inductor through mutual flux causing the current slope to change in three distinct periods resulting in L_{eq1}, L_{eq2} and L_{eq3}. L_{eq1} and L_{eq3} set the peak inductor current for $D<0.5/m$ and $D>0.5/m$ respectively, consequently they directly impact the inductor ripple current. From [9], L_{eq1} or L_{eq3} can be written as:

$$L_{eq1,3} = \alpha \cdot L \tag{6}$$

where α is the factor by which the ripple current will change, it is a function of the coupling coefficient k and the duty cycle D and is given as:

$$\begin{cases} \alpha = \frac{1-k^2}{1+k.\frac{D}{D'}} & D < 0.5/m \\ \alpha = \frac{1-k^2}{1+k.\frac{D}{D'}} & D > 0.5/m \end{cases} \tag{7}$$

If k is negative, i.e., inverse coupling, then it is possible to get α > 1, this means that $L_{eq1,3} > L$. The coupling factor k is a constant once the inductor is designed, hence it should be selected at the design stage to achieve the required performance across the operating duty cycle range.

Fig. 3 plots α versus the duty ratio according to (7). The α greater than 1 indicates that the equivalent inductance is more than the self-inductance. This translates to a reduction in ripple current at the same self-inductance. This might be preferred if the associated increase in switching losses does not negate the benefits of wider CCM range and reduced input/output ripples. The reduced inductor ripple current can be calculated from (8).

$$\Delta i_L = \frac{V_{in}\left(1-\frac{V_{in}}{V_{out}}\right)}{2.\alpha.L.m.f_{sw}} \tag{8}$$

Conversely, if the ripple current is to be maintained, this could translate to a smaller inductance value with smaller inductor size. Then the reduced inductance value can be calculated from (9) rather than (3).

$$L \geq \frac{V_{in}\left(1-\frac{V_{in}}{V_{out}}\right)}{\alpha.2.r_I.I_L.m.f_{sw}} \tag{9}$$

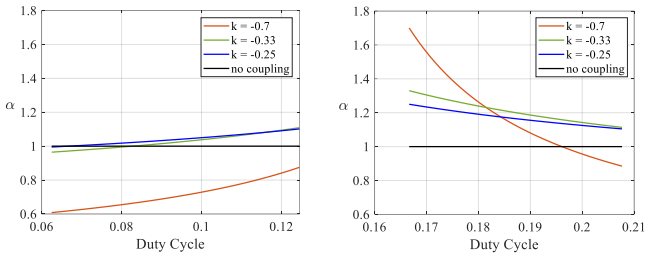


Fig. 3. L_{eq} to L ratio for (a) $D < 0.5/m$ (b) $D > 0.5/m$

Whether the design objective is to minimize the ripple or to minimize the inductance value, an α greater than 1 is preferred. Since the duty cycle depends on the operating point, the only way to adjust α is by selecting an appropriate coupling coefficient value k that will keep $\alpha > 1$ for most of the converter operating range. However, not every k value can be easily achieved since it depends on the physical magnetic core geometry, which imposed another design constraint. Therefore, the objective in selecting k is to choose one that achieves α >1 in a wide operation range and at the same time can be realized without using complicated magnetic core geometries.

In contrast to the steady state operation, where a large inductance value is preferred, it slows down the dynamic response of the converter. Luckily for the inverse coupled inductor $L_{eq2} = (1+k)\ L$ is responsible for the dynamic response of the converter [9] and since k is negative, L_{eq2} is always smaller than L. Therefore, the converter can have faster dynamic response than that with uncoupled inductors. Moreover, due to the increased inductor ripple frequency, the proposed converter could have faster dynamic response than the conventional interleaved boost.

III. Converter Prototype Design

The designed converter parameters are given in Table II. The switching frequency is chosen as 50kHz in a process of manual optimization to balance between the losses and the passives size. The target volume of the converter is less than 1.5L in order to achieve a target power density greater than 33kW/L [10]. To achieve more than 50kW of output power, the input current needs to be at least 100A. Therefore, a converter with four phases was selected. This leads to 25A current in each phase. This low current will help reduce the copper losses as well as the EMI. Because of the coupled inductors, the number of phases needs to be even. Fig. 4 shows a 3D rendering of the power stage and its components. The power modules are placed on the bottom side of the PCB and mounted on the cold plate. Each module has its own gate driver board mounted on top through stacked board to board connectors. Input capacitors are placed on the input side of the PCB on the bottom layer to save space. The output capacitors are placed on the opposite side of the PCB, i.e., the output side, very close to the power modules to reduce the commutation loop stray inductance. They are distributed on the top and bottom sides of the PCB and their series connection is established by an array of top-bottom through hole vias. The inductors are external to the power board and connected to it through power terminals.

TABLE II. DESIGN TARGETS AND PASSIVE COMPONENTS

Parameter	Symbol	Value
Power	P_{out}	50kW
Output Voltage	V_{out}	800V
Input Voltage	V_{in}	350–500V
Max. Input Current	$I_{in.max}$	100A
Switching Frequency	f_{sw}	50kHz
No. of phases/Parallel legs	n/m	4/3
Output Voltage Ripple	r_v	<1%
Inductor Current Ripple	r_I	50%
Efficiency	ζ	>97%
Volume	V	<1.5L
Inductance	L	50µH
Inductor Coupling factor	k	-0.33
Output Capacitance	C_{out}	4.8µF
Input Capacitance	C_{in}	12µF

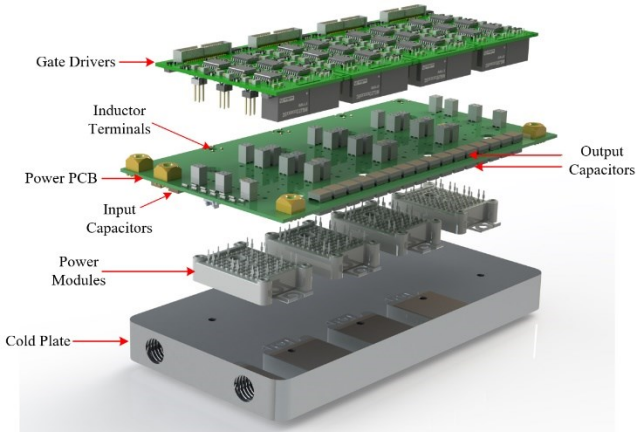


Fig. 4 Power stage CAD rendering of the proposed converter

The overall dimensions of the power stage including the gate drivers is 205*mm*×105*mm*×30*mm* yielding a 0.65L volume excluding the cold plate.

A. Semiconductor Selection

SiC power modules has become attractive when it comes to high power density high performance converters. SiC MOSFET can operate at high frequency with low switching losses because of the steep switching slopes of the device voltage and current. Consequently, this will reduce the thermal requirements and hence reduce the size of the heatsink and further contribute to higher power density. The CCB021M12FM3 [11] power module from Wolfspeed is an off-the-shelf all SiC six-pack module in a small 64×32mm package which is capable of 30A continuous current (limited by the press fit pins) and 106A pulse current. It has very low switching losses, hence it is capable of higher switching frequencies. Moreover, it has low on-resistance, low parasitic inductance and low thermal resistance. In addition, it has low output capacitance C_{oss}, which is important when the MOSFETs are paralleled because their output capacitance will be summed and this will lead to increased switching losses. For these reasons, this module is a good match for this application.

B. Input and Output Capacitors

The output capacitors in a boost converter plays an important role. A high rms current flows in the output capacitor, hence it must have very low ESR values. In addition, it should have low ESL values in order to minimize the overall parasitic inductance in the switching loop and allow steep switching slopes without the need for a snubber. A capacitor network of multiple parallel capacitors is more effective in reducing the impedance than just using one. Furthermore, distributing the high output current among several parallel branches will significantly reduce the output capacitor losses and facilitate their thermal management, hence, prevent their failure and increase their life. The output current ripple frequency of a four-phase interleaved boost is 4× the inductor current ripple frequency. Therefore, a high frequency capacitor is desired with a self-resonant frequency well beyond the output current ripple frequency which is 600kHz in this design ($12\times f_{sw}$). For these reasons, the output capacitor is realized using a network formed by 32 of the CeraLink® B58031U5105M062 capacitors from TDK arranged in 16 parallel branches with two series capacitors comprising each branch. This leads to 4.8µF 1kV of output capacitance.

The input capacitor in the boost converter is less critical but is required to smooth the input current and keep the input volage ripple below a certain level. A 12µF value is estimated from equation (5) with some margin and realized by a series-parallel network of 8 CeraLink® B58035U5106M001 arranged in four branches with each branch consists of two series connected capacitors yielding a 12µF 1kV input capacitance.

C. Power PCB Layout

Due to the fast switching of SiC, it is important to minimize the stray inductance in the switching loop to prevent the drain-source voltage overshoot from exceeding the device limit. According to [12], for high current PCB busbars, increasing the number of layers, using less copper weight per layer and interleaving the DC+ and DC– layers are all good strategies to decrease the parasitic inductance. These techniques have the effect of decreasing the self-inductance and increasing the negative mutual inductance between the layers hence the overall parasitic inductance decrease. For these reasons a 6-layer 1oz copper PCB is selected as a tradeoff between cost and performance. Of which, four layers are used to interleave the DC+ and DC- copper planes, and the other two layers are used for other connections such as the gate driver terminals, power module AC terminal, etc. The low inductance PCB design is verified through a double pulse test. Fig. 5 shows the switching

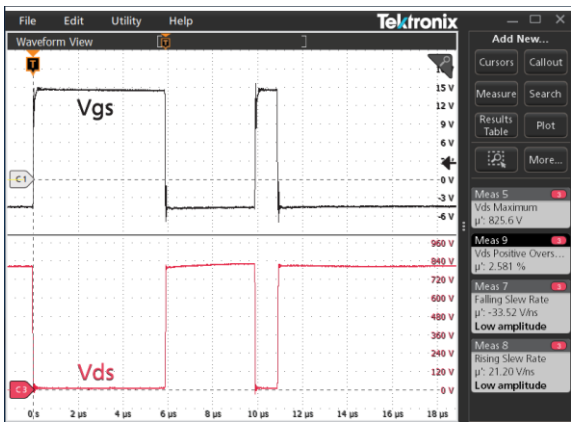


Fig. 5. Gate and switching node voltage during a double pulse test at 800V and 30A.

node voltage of the main switch during a double pulse test at 30A and 800V, the overshoot in voltage is less than 3% and the switching slew rates for on and off are 33V/ns and 22V/ns, respectively.

D. Gate Driver

The gate drivers are essential for proper operation of the converter. The size of the power module poses a challenge in the gate driver design; the six-pack gate driver should be as small as possible so as not hinder the power density but at the same time ensure reliable operation and protection of the power module.

Fig. 6 shows a block diagram of the gate driver architecture, while Fig. 7 shows a CAD rendering of the gate driver board. It features a miller clamp as well as a desaturation protection circuit, a high CMTI (100V/ns) enabled by the gate driver IC and the low capacitance of the isolated power supply. The gate driver signals as well as system health signals are interfaced with the controller through LVDS differential protocol for high signal integrity. Since the six-pack is connected in parallel, i.e., the top switches share a common source and the bottom switches share a common source, only two isolated power supplies are necessary as long as each can provide gate drive power for the three switches.

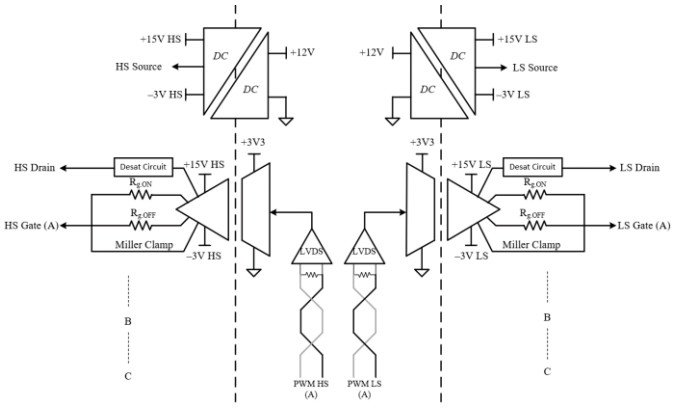


Fig. 6 Simplified block diagram of the gate driver

This helps save valuable space on the gate driver board. The total gate drive power for 3 switches can be calculated from:

$$P_{g.total} = 3 \times Q_g \times f_{sw} \times \left(V_{gs+} - V_{gs-}\right) \qquad (10)$$

where Q_g=162nC is the total gate charge of the MOSFET and is provided in the manufacturer's datasheet. The positive and negative gate voltages are +15V and –3V respectively which yields less than 0.5W of total gate power at 50kHz switching.

The power module has an internal gate resistance of 3.3Ω and the gate driver IC, UCC21750 from Texas Instruments, has an internal on and off resistance of 0.7Ω and 0.3Ω respectively, therefore, to achieve the fastest switching and the lowest switching losses, an external zero-ohm resistor is used for both the turn-on and turn-off of the low side switches since the majority of the switching losses comes from the low side switch. Several potential problems can rise from using such low gate resistance: first is the overshoot in the drain-source voltage due

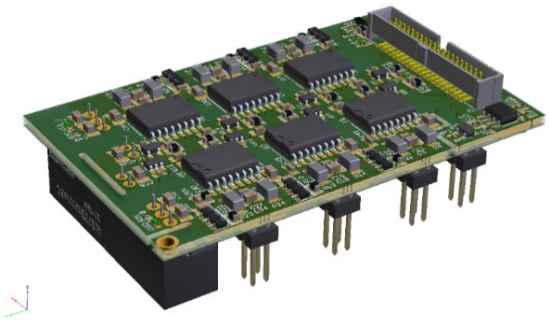


Fig. 7 CAD rendering of the gate driver

to the fast-switching slope, the second is an overshoot in the gate-source voltage due to an underdamped gate drive circuit. It can be seen from Fig. 5 that neither is an issue in this design. Because of the low stray inductance of the module and the low inductance design of the busbar, there is little overshoot on the drain-source voltage of the MOSFET, at the same time, due to proper layout of the gate driver circuit and minimizing the gate-source loop, the gate-source voltage overshoot does not exceed the device maximum rating. In Fig. 5 the gate-source voltage V_{gs} is measured using an IsoVu™ probe. Finally, the fast turn on of the low side switch will increase the reverse recovery losses of the body diodes of the high side switches which are conducting current during the dead time period and since this module has body diodes rather than Schottky diodes, the reverse recovery losses is severe, and a tradeoff must be made between turn-on losses of the low side switch and the reverse recovery losses of the body diodes.

E. Inductor Design

Fig. 8 shows the inductor construction used in this work. In order to reduce the size of the inductor, planar ferrite cores are selected. They are low profile cores with greater surface area, resulting in improved heat dissipation capability. There are many methods in literature to choose the core size. In this work the largest off the shelf planar E core (E64/50/10) was selected and arranged in EE core configuration. For a 150kHz inductor current ripple frequency ($m \times f_{sw}$), a 3F36 ferrite core from Ferroxcube is selected, which is suitable for high frequency operation with low losses, in addition, it has high saturation flux. To ensure enough safety margin, the maximum flux was set to 350mT in this design.

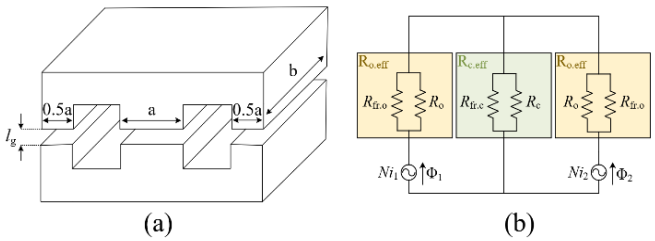


Fig. 8. The coupled inductor (a) core geometry and (b) equivalent reluctance circuit.

From the reluctance circuit in Fig. 8 (b), the ideal inductances and coupling coefficient k can be derived as:

$$\begin{cases} L = \frac{N^2.(R_o+R_c)}{R_o.(R_o+2R_c)} \\ M = -\frac{N^2.R_c}{R_o.(R_o+2R_c)} \\ k = \frac{M}{L} = -\frac{R_c}{R_o+R_c} \end{cases} \quad (11)$$

Choosing an equal air gap in the outer and center legs will yield k = –1/3 by substituting $R_o = 2R_c$ in (11) which will simplify the core structure from one hand and keep α >1 for a wide converter operation region as seen from Fig. 3.

The minimum number of turns that will keep the flux density in the core below a maximum value B_{max} caused by a peak inductor current I_{pk} in the core's outer leg of cross-sectional area A_o is calculated from:

$$N_{min} = \left\lceil \frac{(L+M)I_{pk}}{B_{max}.A_o} \right\rceil \quad (12)$$

Then the ideal air gap length not considering the fringing effect can be calculated from:

$$l_{g.ideal} = \frac{3.N_{min}^2.\mu_o.A_o}{4.L} \quad (13)$$

The fringing effect caused by the air gap will increase the effective cross-sectional area of the air gap and hence reduce the reluctance causing the actual inductance value to increase and the core will saturate early due to the increased flux density. Therefore, the air gap length needs to be increased to account for the fringing effect and keep the core from saturation. One simple method to account for the fringing effect is to treat the fringing effect as a parallel reluctance [13] as shown in Fig. 8 (b) Then the air gap length can be adjusted according to the following equations:

$$\begin{cases} A_{c.eff} = (a+2l_g) \times (b+2l_g) \\ A_{o.eff} = (0.5a+2l_g) \times (b+2l_g) \end{cases} \quad (14)$$

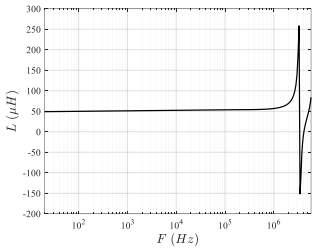
$$\begin{cases} R_{c.eff} = R_c \parallel R_{fr.c} = \frac{l_g}{\mu_o.A_{c.eff}} \\ R_{o.eff} = R_o \parallel R_{fr.o} = \frac{l_g}{\mu_o.A_{o.eff}} \end{cases} \quad (15)$$

The inductance values can be recalculated from (11) using the effective reluctances from (15). Finally, the maximum flux density can be rechecked using the recalculated inductances to ensure it does not exceed the maximum value:

$$B = \frac{(L+M)I_{pk}}{N.A_{o.eff}} < B_{max} \quad (16)$$

The inductor prototype is shown in Fig. 9 and its design parameters are given in Table III, the volume of the four inductors is 0.2L. Litz wire was used to form the coil around the outer legs, both coils are wound in the same direction to achieve inverse coupling. The core is wrapped with thermal interface tape to improve the heat dissipation of the top half of the core. Fig. 9 (b) shows the self-inductance value measured using the Keysight 4990A impedance analyzer, the plot also shows the resonant frequency above 2MHz which is well beyond the current ripple frequency of the inductor. The AC resistance was also measured at 150kHz as 62mΩ.

(a)



(b)

Fig. 9. The realized coupled inductor (a) protoype and (b) impedance analyzer measurement.

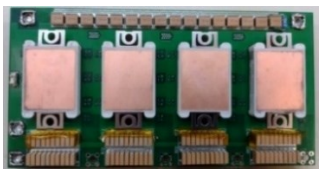
TABLE III. DESIGN PARAMETERS OF THE COUPLED INDUCTOR

Parameter	Value
L	50μH
k	–1/3
Core	EE64/50/10 – 3F36
B_{max}	350mT
a	10.2mm
b	50.8mm
N	15
l_g	2mm

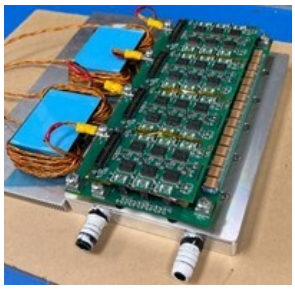
IV. EXPERIMENTAL RESULTS

The actual converter prototype is shown in Fig. 10, with the input connected to a high-power DC source and the output connected to a high-power resistive load. Fig. 11 shows the typical experimental results at 40kW. The data was collected using a Tektronix MSO58 scope, the inductor currents was measured with the high bandwidth TCP0030A current probes while the input current is measured with TCP404XL. The voltages were measured with 1.5kV THDP0200 differential voltage probes.

(a)



(b)



(c)

Fig. 10. 50kW boost converter protoype (a) top view, (b) bottom view and (c) assembled converter.

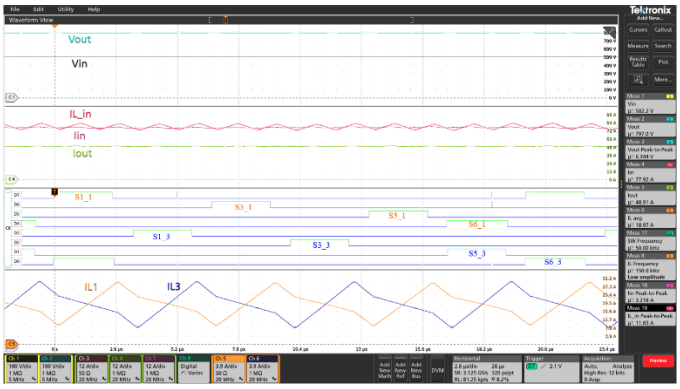


Fig. 11. Experimental waveforms for a 40kW test

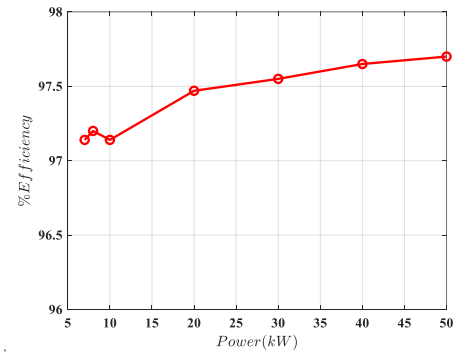


Fig. 12. Efficiency plot of the converter prototype up to 50kW

The input voltage is 500V and the output voltage is 800V, this is achieved using a 12.5% duty cycle calculated from (2). The results show the switching pattern for phases 1 and 3 and the corresponding inductor currents. It is clear that, while the switching frequency is 50kHz, the inductor ripple current is 150kHz. The input/output ripple frequency is 600kHz, this high frequency results in a low output voltage ripple of less than 1% which meets the design targets. The input current ripple is less than 4A because of the filtering effect of the input capacitor, the ripple current measured after the input capacitor, i.e., the sum of the inductor currents, is a triangular current with a peak-to-peak ripple value of 11.65A and an average value of 78A. Fig. 12 shows the efficiency of the converter measured with a Hioki power analyzer up to 50kW. A peak efficiency of 97.7% is achieved. The overall volume of the converter was 0.85L excluding the cold plate which achieves a power density of 60kW/L which exceeds the design target.

V. Conclusion

In this paper, the analysis and hardware design of a four-phase interleaved boost converter with coupled inductors is presented. A six-pack SiC module was used as a single-phase building block to triple the inductor ripple frequency and distribute the switching losses over a larger number of semiconductors to simplify the thermal management. Thus, the volume of the passive components can be significantly reduced compared to conventional interleaved boost. In addition, input current and output voltage ripples are also reduced, and their frequencies are pushed beyond 500kHz. Moreover, the coupling of inductors further reduced the size and weight of the inductor and improved the performance and efficiency. The volume of the power stage is 0.65L while that of the inductor is 0.2L which leads to a higher power density of 60kW/L excluding cold plate. As a first prototype, some extra safety margins were considered in the design, such as decreasing the current ratings of the power module, therefore, there is more room with the same prototype to increase the output power further and hence push the power density higher which will be done in the future.

References

[1] S. Christian, R. A. Fantino, R. A. Gomez, Y. Zhao and J. C. Balda, "High Power Density Interleaved ZCS 80-kW Boost Converter for Automotive Applications," in *IEEE Journal of Emerg. and Selected Topics in Power Electron.*, doi: 10.1109/JESTPE.2021.3099408.J.

[2] A. H. Wienhausen, R. W. de Doncker, and A. Vescan, "High integration of power electronic converters enabled by 3d printing," Institut fur Stromrichtertechnik und Elektrische Antriebe, Tech. Rep., 2019.

[3] A. H. Wienhausen, A. Sewergin and R. W. De Doncker, "Highly Integrated Boost Converter featuring a Power Density of 98 kW/dm3 and 56 kW/kg," PCIM Europe digital days 2020; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management, 2020, pp. 1-5.

[4] J. Guo et al., "A Comprehensive Analysis for High-Power Density, High-Efficiency 60 kW Interleaved Boost Converter Design for Electrified Powertrains," in *IEEE Trans. on Vehicular Tech.*, vol. 69, no. 7, pp. 7131-7145, July 2020, doi: 10.1109/TVT.2020.2991395.

[5] O. Kreutzer, B. Eckardt and M. März, "Unidirectional fast switching non-isolated 100 kW fuel cell boost converter," 2014 16th European Conference on Power Electronics and Applications, 2014, pp. 1-10, doi: 10.1109/EPE.2014.6910797.

[6] H. N. Tran, T. -T. LE, H. Jeong, S. Kim and S. Choi, "A 300 kHz, 63 kW/L ZVT DC–DC Converter for 800-V Fuel Cell Electric Vehicles," in *IEEE Trans. on Power Electron.*, vol. 37, no. 3, pp. 2993-3006, March 2022, doi: 10.1109/TPEL.2021.3108815.

[7] O. Hegazy, J. V. Mierlo and P. Lataire, "Analysis, Modeling, and Implementation of a Multidevice Interleaved DC/DC Converter for Fuel Cell Hybrid Electric Vehicles," in *IEEE Trans. on Power Electron.*, vol. 27, no. 11, pp. 4445-4458, Nov. 2012, doi: 10.1109/TPEL.2012.2183148.

[8] R. Mayer, M. B. E. Kattel and S. V. G. Oliveira, "Multiphase Interleaved Bidirectional DC/DC Converter With Coupled Inductor for Electrified-Vehicle Applications," in *IEEE Trans. on Power Electron.*, vol. 36, no. 3, pp. 2533-2547, March 2021, doi: 10.1109/TPEL.2020.3015390.

[9] Pit-Leong Wong, Peng Xu, P. Yang and F. C. Lee, "Performance improvements of interleaving VRMs with coupling inductors," in *IEEE Trans. on Power Electron.*, vol. 16, no. 4, pp. 499-507, July 2001, doi: 10.1109/63.931059.

[10] "Electrical and electronics technical team roadmap - energy," Oct-2017. [Online].Available:https://www.energy.gov/sites/prod/files/2017/11/f39/EETT%20Roadmap%2010-27-17.pdf.

[11] Wolfspeed, "1200 V, 21 mΩ All-Silicon Carbide Six-Pack Module", CCB021M12FM3, Jan. 2021.

[12] L. Wen, L. Yang, W. Yu and I. Husain, "PCB Busbar Optimization for High Power SiC Module," 2019 IEEE 7th Workshop on Wide Bandgap Power Devices and Applications (WiPDA), 2019, pp. 225-230, doi: 10.1109/WiPDA46397.2019.8998882.

[13] Z. Yang, H. Suryanarayana and F. Wang, "An Improved Design Method for Gapped Inductors Considering Fringing Effect," 2019 IEEE Applied Power Electronics Conference and Exposition (APEC), 2019, pp. 1250-1256, doi: 10.1109/APEC.2019.8721811.