A Ge-Channel Ferroelectric Field Effect Transistor With Logic-Compatible Write Voltage

Dipjyoti Das, *Member, IEEE*, Prasanna Venkatesan Ravindran, *Graduate Student Member, IEEE*, Chinsung Park, *Graduate Student Member, IEEE*, Nujhat Tasneem, *Graduate Student Member, IEEE*, Zheng Wang, *Graduate Student Member, IEEE*, Hang Chen, Winston Chern, *Member, IEEE*, Shimeng Yu, *Senior Member, IEEE*, Suman Datta, *Fellow, IEEE*, and Asif Khan, *Senior Member, IEEE*

***Abstract*— A major roadblock for the integration of ferroelectric-field-effect transistors (FEFETs) at advanced technology nodes for embedded memory applications is their high, logic-incompatible write voltages. Herein, we explore Ge as a channel material to reduce write voltage of FEFET and report the first demonstration of p-type Ge-FEFETs with record low write voltages of ±1.4 V with a memory window (MW) of 0.6 V at DC and write voltages of ±1.4 V, ±1.8 V and ±2.4 V for MW of 0.2 V, 0.5 V and 0.8 V for a write time of 10 μs, respectively. The write voltages observed in Ge-pFEFETs are ∼50% lower than that of a Si-pFEFETs when compared against iso-memory window condition [±2.5 V with a MW of 0.6 V at DC, ±3.5 V for MW of 0.5 V for a write time of 10 μs]. Such dramatic reduction of write voltages in Ge-pFEFETs is achieved due to the fact that the native oxide of Ge (GeO_x), formed at the Ge interface, has a larger dielectric constant and lower thickness than those for SiO_2 on the Si platform. In addition, the lower bandgap and higher dielectric constant of Ge may lead to a lower surface potential for a given semiconductor charge, leading to further reduction in the write voltage. Further, our Ge-pFEFETs show write endurance of 10^7 cycles (the best-in-class for Ge-pFEFETs, as reported in the literature), excellent data retention, and immediate read-after-write capability. Our results indicate the attractiveness of Ge platform for FEFETs for embedded memory applications.**

***Index Terms*— Ge-channel, FEOL, FEFETs, write voltage, memory window, endurance, retention, read-after-write.**

I. Introduction

FERROELECTRIC field effect transistors (FEFETs) are one of the most promising candidates among emerging memory technologies for data centric computing due to their best-in-class energy profile, high speed, low area footprint, high scalability as that of state-of-the-art logic transistors, multi-bit storage and neuromorphic capabilities [1], [2], [3], [4]. However, a critical roadblock for the integration of Si-based FEFETs at advanced technology nodes is their write voltages (≥2.5 V) being significantly larger than logic compatible ones (≤1.5 V), primarily due to the voltage drops across the interfacial oxide layer (IL) and the semiconductor (∼ 60%), rather than across the ferroelectric (FE) layer. This increases the overhead requirements at the peripheral circuits and reduces FEFET density and array efficiency for memory applications.

In past decade, numerous efforts have been made to reduce the write voltage of FEFETs by means of FE and IL engineering [5], [6], [7], [8], [9], [10], [11], [12], [13]. Interestingly, despite semiconductor substrates playing an important role in defining the IL and surface potential, semiconductor engineering has received less attention in the context of low voltage FEFETs. Ge, in this regard, presents unique opportunities. The low bandgap and higher dielectric

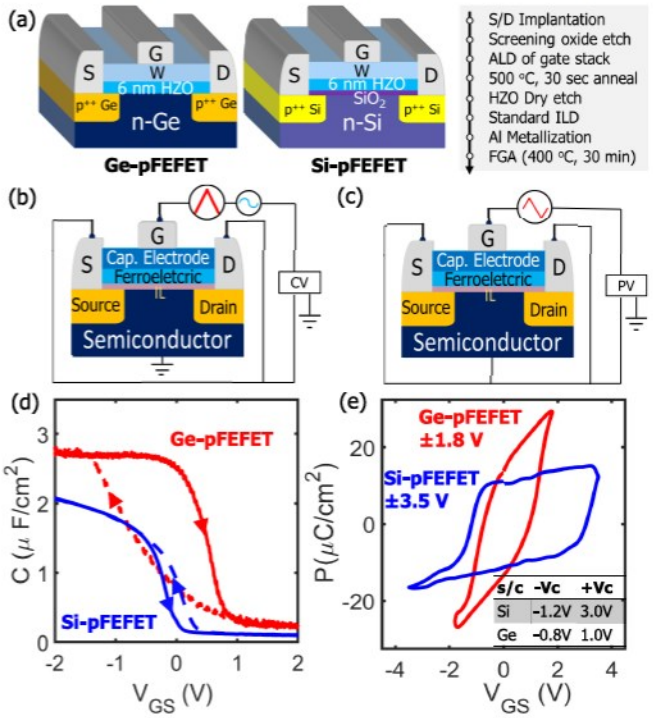

Fig. 1. (a) Device schematic and the fabrication process flow (b,c) Experimental setup used to obtain the capacitance vs. voltage (C-V) and polarization vs. voltage (P-V) characteristics (d) C-V [100 kHz] and (e) P-V characteristics of the Ge-pFEFETs and Si-pFEFETs.

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Dipjyoti Das, Prasanna Venkatesan Ravindran, Chinsung Park, Nujhat Tasneem, Zheng Wang, Winston Chern, Shimeng Yu, and Suman Datta are with the School of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta, GA 30318 USA (e-mail: dip.iitg@gmail.com).

Hang Chen is with the Institute of Electronics and Nanotechnology, Georgia Institute of Technology, Atlanta, GA 30318 USA.

Asif Khan is with the School of Electrical and Computer Engineering and the School of Material Science and Engineering, Georgia Institute of Technology, Atlanta, GA 30318 USA.

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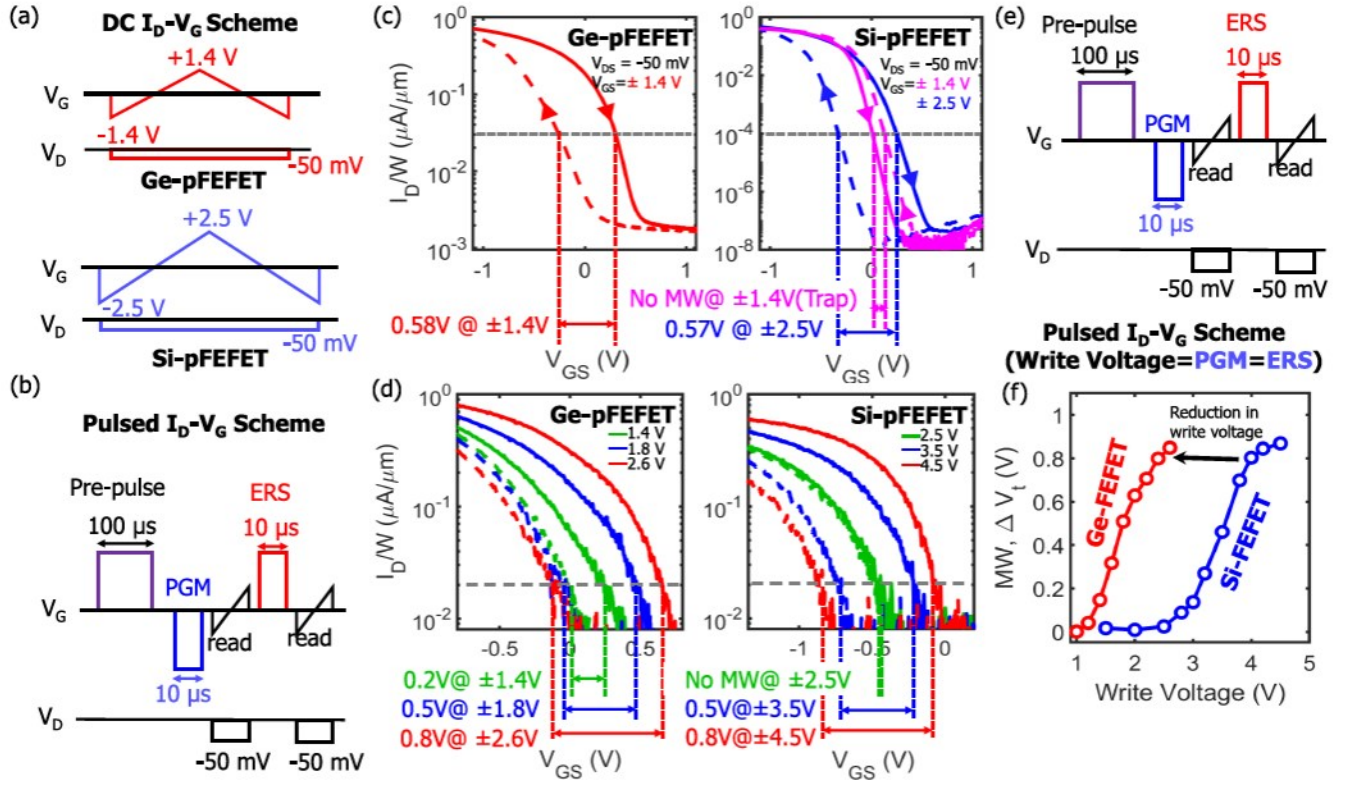

Fig. 2. (a) DC and (b) pulsed I_D-V_G scheme (c) DC I_D-V_G characteristics of the Ge-pFEFETs [@ ±1.4 V] and Si-pFEFETs [@ ±1.4 V and @ ±2.5 V] (d) Pulsed I_D-V_G characteristics of the Ge-pFEFETs and Si-pFEFETs measured for different write voltages [write duration 10 μs] (e) Pulse scheme used to measure MW as a function of write voltage (f) MW as a function of write voltage [write duration 10 μs].

constant of Ge leads to a lower surface potential for a given semiconductor charge. In addition, the native oxide of Ge (GeO_x) has a larger dielectric constant, and its thickness is more controllable (compared to SiO_2 in the Si-platform). Both effects can lead to ultra-low write voltages in Ge-channel FEFETs.

In this letter, we demonstrate a front-end-of-the-line (FEOL) FEFET with record low write voltage of <1.5 V with a significant MW >0.5 V by exploring Ge as the channel material. The write voltages observed in Ge-pFEFETs are ~ 50% lower than that of a Si-pFEFETs for iso-MW condition. Further, the Ge-pFEFETs demonstrates write endurance of 10^7 cycles, excellent data retention and immediate read-after-write capability. The results discussed herein highlight the attractiveness of Ge platform for FEFETs for embedded memory applications.

II. Experimental Details

The device schematic and the fabrication process flow of the 6 nm HZO Ge-pFEFET and Si-pFEFET investigated in this study are shown in Fig.1 (a). The source (S) and drain (D) are formed using ion-implantation (BF_2, 15 keV (Si)/40 keV (Ge), 4×10^{15} cm^2) followed by dopant activation. Ge wafers are cleaned by repetitive HF:DI cycles whereas the Si wafers are cleaned using 7:1 HF and SC1. The HZO film was crystallized by rapid thermal annealing at 500 °C for 30 sec. The detail fabrication procedure of the FEFETs can be found in our previous report [14]. All the FEFET characterizations were done using Keysight B1500A semiconductor device analyzer.

III. Results and Discussion

The capacitance vs. voltage (C-V) and polarization vs. voltage (P-V) characteristics of the FEFETs are measured using the experimental set-up shown in Fig. 1(b) and 1(c), respectively. Fig. 1(d) shows the as measured C-V characteristics of the Ge-pFEFETs and Si-pFEFETs. The capacitance of the gate stack in Ge-pFEFET was found to be significantly higher than that of Si-pFEFET. Likewise, a much reduced coercive voltage for the 6 nm HZO gate stack was observed in a Ge platform as compared to that of Si platform (from ~3.0 V to ~1.0 V) as can be seen from the P-V characteristics shown in Fig. 1(e). This might be due to two reasons: (1) Ge, has a lower surface potential due to its lower band gap and high dielectric constant and (2) the native oxide of Ge (GeO_x) has a larger dielectric constant (compared to SiO_2 in the Si-platform), and its thickness is more controllable. Both effects can lead to ultra-low write voltages in Ge-channel FEFET. A thinner (GeO_x) with high dielectric constant results in a higher IL capacitance reducing the voltage drop across the IL. Similarly, the lower surface potential of Ge reduces the voltage drop across the semiconductor. Consequently, a higher fraction of the gate voltage drops across the FE layer and it switches at a much lower write voltage.

We measured the DC and pulsed drain current vs. gate voltage (I_D-V_G) characteristics of FEFETs fabricated in Ge

and Si platform by using the DC and pulsed I_D-V_G scheme shown in Fig. 2(a) and 2(b), respectively. Fig. 2(c) shows the DC I_D-V_G characteristics of the Ge-pFEFETs for a voltage sweep of ±1.4 V and that of Si-pFEFETs for a voltage sweep of ±1.4 V and ±2.5 V, respectively. The Ge-pFEFET demonstrates a D.C. memory window (MW) of ∼0.6 V for a D.C. sweep range as low as ±1.4 V. On the contrary, while no MW can be observed in Si-pFEFETs at ±1.4 V, a MW of ∼0.6 V was observed for a D.C. sweep range of ±2.5 V. Overall, the write voltage in Ge-pFEFETs in case of DC I_D-V_G, was ∼1.75 times lower than that of Si-pFEFETs.

Pulsed I_D-V_G characteristics of the Ge-pFEFETs and Si-pFEFETs for different write voltages for a write duration of 10 μs are shown in Fig. 2(d). MW was extracted from the pulsed I_D-V_G curve at drain current of 20 $nA/\mu m$. The Ge-pFEFETs demonstrated a MW of ∼0.2 V, ∼0.5 V and ∼0.8 V for a write voltage of ±1.4 V, ±1.8 V and ±2.6 V, respectively. However, no MW was seen in the Si-pFEFETs for a write voltage of ±2.5 V, and a MW of ∼0.5 V and ∼0.8 V was observed for a write voltage of ±3.5 V, ±4.5 V, respectively. The MW of both the FEFETs was also measured at different write voltage using the pulse scheme shown in Fig. 2(e). The MW of the Ge-pFEFETs and Si-pFEFETs as a function of write voltage for a write duration 10 μs is shown in Fig. 2(f). The significant reduction (∼ 50%) in write voltage for a given MW in Ge-pFEFETs as compared to that of a Si-pFEFETs highlights the importance of Ge as a channel material for low voltage FEFETs.

The delay required to read after write operation is another critical metrics for evaluating the performance of an FEFET. Fundamentally, this read delay is due to the trapping of electron or hole at the FE-IL interface. Due to trapping, the interfacial states present at the FE-IL interface becomes charged and screen the ferroelectric polarization which is supposed to be screened by the channel charge. Therefore, the interfacial charges states need to be neutralized to ensure that the correct polarization state is read [15], [16], [17]. MW as a function of read delay are measured for Ge-pFEFET, Si-pFEFET and Si-nFEFET by applying delay (t_{Delay}) after program and erase pulse as shown in Fig. 3(a). Fig. 3(b) shows read-after-write characteristics of the aforesaid FEFETs at iso-MW condition. While MW in Si-nFEFET increases with t_{Delay}, no significant changes in MW was observed with t_{Delay} in Ge-pFEFET and Si-pFEFETs, indicating the presence of less significant interfacial traps, which is characteristic of p-type FEFETs [18].

To evaluate the reliablity, write endurance of the Ge-pFEFETs are measured by applying fatigue pulses as shown in Fig. 3(c). The endurance of the Ge-pFEFETs for different write times, with write voltages adjusted for iso-MW conditions, is shown in Fig. 3(d). The Ge-pFEFETs were found to demonstrate an endurance of 10^5 cycle,10^6 cycle and 10^7 cycle, respectively, when fatigue pulse of duration 10 μs (±1.8 V), 1 μs (±2.5 V) and 100 ns (±3.7 V) were applied. Application of fatigue pulses faster than the trap capture/generation time is reported to reduce the amount of traps in the gate oxide of the FEFETs [19]. The higher endurance observed in the Ge-FEFETs for smaller fatigue

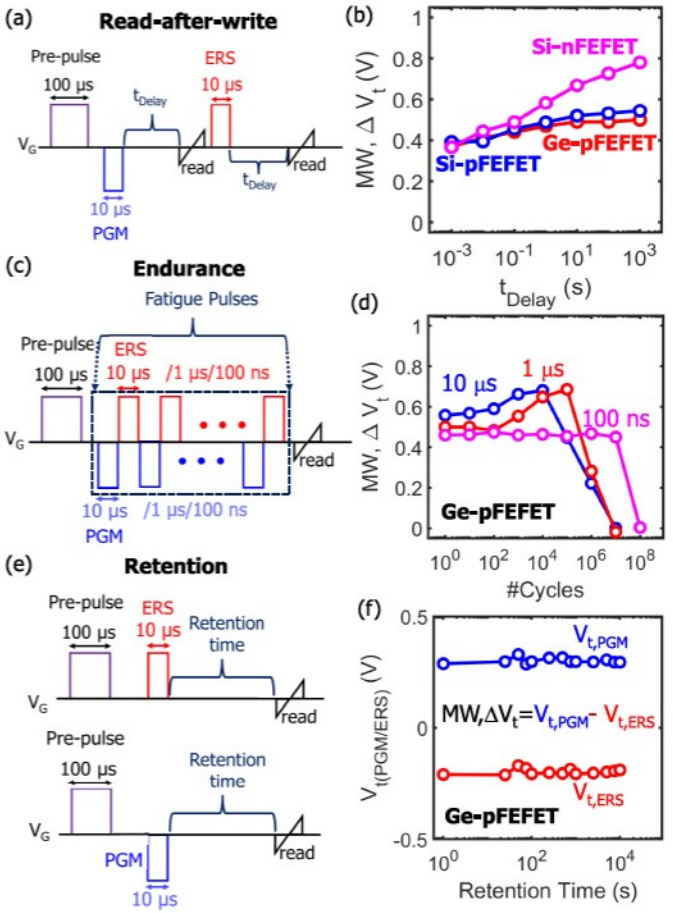

Fig. 3. (a,b) Measurement scheme and MW of the Ge-pFEFETs, Si-pFEFETs and Si-nFEFETs as a function of read-after-write delay [±1.8 V, ±3.5V, ±3.5V] (c,d) Measurement scheme and endurance characteristics of the Ge-pFEFETs at different write time under iso-MW condition [±1.8 V @ 10 μs, ±2.5V @ 1μs, ±3.7 V @100 ns] (e,f) Measurement scheme and retention property of the Ge-pFEFETs at room temperature.

pulses is therefore assumed to be due to less charge trapping and defect generation in the gate oxide.

The retention property of the Ge-pFEFETs were also measured [Fig. 3(e)] at room temperature for a write voltage and write time of ±1.8V and 10 μs respectively and is shown in Fig. 3(f). No deduction in MW was observed in the Ge-pFEFETs till 10^4 s suggesting excellent data retention.

IV. Conclusion

In conclusion, we report Ge-channel p-type FEFETs with record low write voltages: ±1.4 V with MW of 0.6 V at DC and ±1.4 V, ±1.8 V and ±2.4 V for MW of 0.2 V, 0.5 V and 0.8 V for a write time of 10 μs, respectively. The write voltages observed in Ge-pFEFETs are ∼50% lower than that of a Si-pFEFETs when compared against iso-memory window condition. Further, the Ge-pFEFETs demonstrate write endurance upto 10^7 cycles, excellent data retention and no read-after-write delay. Our results indicate the attractiveness of the Ge platform for FEFETs in the context of low voltage/logic-compatible operation.

REFERENCES

[1] J. Hoffman, X. Pan, J. W. Reiner, F. J. Walker, J. P. Han, C. H. Ahn, and T. P. Ma, "Ferroelectric field effect transistors for memory applications," *Adv. Mater.*, vol. 22, nos. 26–27, pp. 2957–2961, Jul. 2010.

[2] A. I. Khan, A. Keshavarzi, and S. Datta, "The future of ferroelectric field-effect transistor technology," *Nature Electron.*, vol. 3, no. 10, pp. 588–597, Oct. 2020.

[3] D. Das and A. I. Khan, "Ferroelectricity in CMOS-compatible hafnium oxides: Reviving the ferroelectric field-effect transistor technology," *IEEE Nanotechnol. Mag.*, vol. 15, no. 5, pp. 20–32, Oct. 2021.

[4] X. Chai, J. Jiang, Q. Zhang, X. Hou, F. Meng, J. Wang, L. Gu, D. W. Zhang, and A. Q. Jiang, "Nonvolatile ferroelectric field-effect transistors," *Nature Commun.*, vol. 11, no. 1, pp. 1–9, Jun. 2020.

[5] A. J. Tan, Y.-H. Liao, L.-C. Wang, N. Shanker, J.-H. Bae, C. Hu, and S. Salahuddin, "Ferroelectric HfO_2 memory transistors with high-κ interfacial layer and write endurance exceeding 1010 cycles," *IEEE Electron Device Lett.*, vol. 42, no. 7, pp. 994–997, Jul. 2021.

[6] A. J. Tan, M. Pešić, L. Larcher, Y.-H. Liao, L.-C. Wang, J.-H. Bae, C. Hu, and S. Salahuddin, "Hot electrons as the dominant source of degradation for sub-5nm HZO FeFETs," in *Proc. IEEE Symp. VLSI Technol.*, Jun. 2020, pp. 1–2.

[7] S. Dünkel, M. Trentzsch, R. Richter, P. Moll, C. Fuchs, O. Gehring, M. Majer, S. Wittek, B. Müller, T. Melde, H. Mulaosmanovic, S. Slesazeck, S. Müller, J. Ocker, M. Noack, D.-A. Lohr, P. Polakowski, J. Müller, T. Mikolajick, J. Hontschel, B. Rice, J. Pellerin, and S. Beyer, "A FeFET based super-low-power ultra-fast embedded NVM technology for 22 nm FDSOI and beyond," in *IEDM Tech. Dig.*, Dec. 2017, pp. 19.7.1–19.7.4.

[8] M.-C. Nguyen, S. Kim, K. Lee, J.-Y. Yim, R. Choi, and D. Kwon, "Wakeup-free and endurance-robust ferroelectric field-effect transistor memory using high pressure annealing," *IEEE Electron Device Lett.*, vol. 42, no. 9, pp. 1295–1298, Sep. 2021.

[9] H. Liu et al., "ZrO_2 ferroelectric FET for non-volatile memory application," *IEEE Electron Device Lett.*, vol. 40, no. 9, pp. 1419–1422, Sep. 2019.

[10] C. Zacharaki, S. Chaitoglou, N. Siannas, P. Tsipas, and A. Dimoulas, "$Hf_{0.5}Zr_{0.5}O_2$-based germanium ferroelectric p-FETs for nonvolatile memory applications," *ACS Appl. Electron. Mater.*, vol. 4, no. 6, pp. 2815–2821, Jun. 2022.

[11] N. Tasneem, M. M. Islam, Z. Wang, H. Chen, J. Hur, D. Triyoso, S. Consiglio, K. Tapily, R. Clark, G. Leusink, S. Yu, W. Chern, and A. Khan, "The impacts of ferroelectric and interfacial layer thicknesses on ferroelectric FET design," *IEEE Electron Device Lett.*, vol. 42, no. 8, pp. 1156–1159, Aug. 2021.

[12] K. Ni, P. Sharma, J. Zhang, M. Jerry, J. A. Smith, K. Tapily, R. Clark, S. Mahapatra, and S. Datta, "Critical role of interlayer in $Hf_{0.5}Zr_{0.5}O_2$ ferroelectric FET nonvolatile memory performance," *IEEE Trans. Electron Devices*, vol. 65, no. 6, pp. 2461–2469, Jun. 2018.

[13] H.-K. Peng, J.-Z. Chen, and Y.-H. Wu, "Improved memory window and robust endurance for Ge p-channel ferroelectric FET memory using microwave annealing followed by rapid thermal annealing," *IEEE Electron Device Lett.*, vol. 43, no. 12, pp. 2073–2076, Dec. 2022.

[14] N. Tasneem, M. M. Islam, Z. Wang, Z. Zhao, N. Upadhyay, S. F. Lombardo, H. Chen, J. Hur, D. Triyoso, S. Consiglio, K. Tapily, R. Clark, G. Leusink, S. Kurinec, S. Datta, S. Yu, K. Ni, M. Passlack, W. Chern, and A. Khan, "Efficiency of ferroelectric field-effect transistors: An experimental study," *IEEE Trans. Electron Devices*, vol. 69, no. 3, pp. 1568–1574, Mar. 2022.

[15] S.-H. Kuk, S.-M. Han, B.-H. Kim, S.-H. Baek, J.-H. Han, and S.-H. Kim, "Comprehensive understanding of the HZO-based n/pFeFET operation and device performance enhancement strategy," in *IEDM Tech. Dig.*, Dec. 2021, pp. 33.6.1–33.6.4.

[16] E. Yurchuk, J. Müller, S. Müller, J. Paul, M. Pesic, R. van Bentum, U. Schroeder, and T. Mikolajick, "Charge-trapping phenomena in HfO_2-based FeFET-type nonvolatile memories," *IEEE Trans. Electron Devices*, vol. 63, no. 9, pp. 3501–3507, Sep. 2016.

[17] S. Deng, Z. Zhao, Y. S. Kim, S. Duenkel, D. MacMahon, R. Tiwari, N. Choudhury, S. Beyer, X. Gong, S. Kurinec, and K. Ni, "Unraveling the dynamics of charge trapping and de-trapping in ferroelectric FETs," *IEEE Trans. Electron Devices*, vol. 69, no. 3, pp. 1503–1511, Mar. 2022.

[18] D. Kleimaier, H. Mulaosmanovic, S. Dunkel, S. Beyer, S. Soss, S. Slesazeck, and T. Mikolajick, "Demonstration of a p-type ferroelectric FET with immediate read-after-write capability," *IEEE Electron Device Lett.*, vol. 42, no. 12, pp. 1774–1777, Dec. 2021.

[19] J. Duan, H. Xu, J. Xiang, X. Wang, and W. Wang, "Significant improvement of endurance of Si FeFET through minor hysteresis loop and narrow write pulse width," *Appl. Phys. Exp.*, vol. 15, no. 12, Dec. 2022, Art. no. 121005.