Backgated Graphene Varactors with Quality Factor - Frequency Product Above 300 GHz

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***Abstract*—Back-gated, multifinger graphene RF varactors with a de-embedded quality factor frequency product, $Q \times f$, above 300 GHz are demonstrated. The effect of different design parameters on the tuning ratio and quality factor at 77 K and room temperature are explored at frequencies between 1 MHz and 18 GHz. The best device has Q of 18.4 at 18 GHz. We also perform small signal equivalent circuit modeling on different designs to further explain the effect of design parameters on the RF performance. These results are promising for future integration of graphene varactors in high-speed analog applications.**

***Index Terms* – Graphene, Varactors, Quantum Capacitance, RF**

I. INTRODUCTION

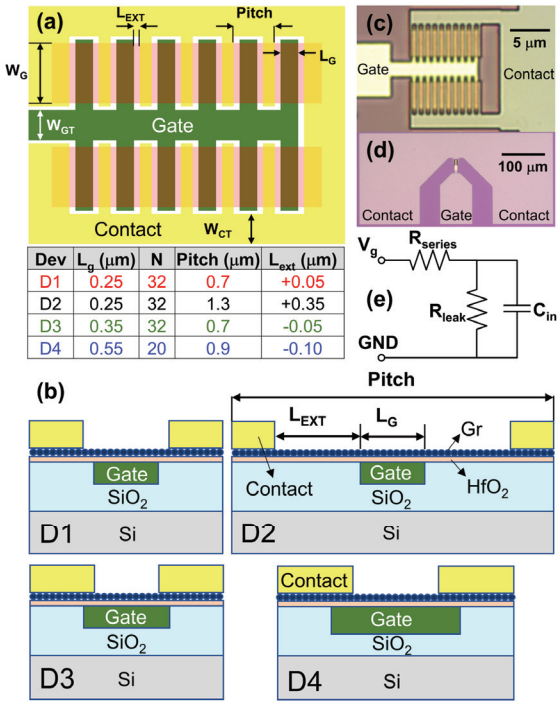
Graphene is a two-dimensional sheet of carbon with one-atom thickness, extremely high electron mobility [1], high mechanical strength [2], and high transparency [3]. These unique properties of graphene make it a promising candidate for high-speed, transparent, and flexible electronics. The use of graphene as a transistor channel material is limited by the high off current due to its zero bandgap [4]. Therefore, in this work, we focus on another interesting property of graphene, the quantum capacitance effect [5], which allows it to act as a variable capacitor (varactor).

Most common state-of-the-art varactors include micro-electro-mechanical (MEMS) and metal-oxide-semiconductor (MOS) devices. MEMS varactors have achieved high quality factor, however, they often require actuation voltages of 20-100 V to achieve high tuning ratio [6]. MEMS varactors are also limited by packaging and reliability issues and have relatively low speed. Varactors based on III-V semiconductors or MOS technology typically show high quality factor and tuning ratio. MOS varactors providing tuning ratio of 1.6 with a quality factor of 24 at 100 GHz have been reported [7]. However, these devices are not well-suited for use on transparent or non-conventional substrates.

Graphene varactors, on the other hand, offer several key advantages over these more conventional varactor technologies. The first is that graphene varactors can produce large capacitive tuning slope, defined as dC/dV, as first pointed out in [8]. Secondly, and more importantly, they do not require single-crystal material, and can readily be integrated onto transparent and flexible substrates without the need for flip-chip bonding, suggesting excellent potential for transparent and flexible antennas and RF circuits [9]. Graphene varactors do have smaller tuning ratios (< 2) than III-V and Si devices, but for many applications [10], these tuning ratios could be adequate. In fact, the achievable tuning ratios are comparable to MEMS varactors (~1.5) when those devices are operated at low voltages (< 2 V) [11].

Graphene varactors have tremendous potential for extremely high-speed operation, yet to date, they have mainly been investigated for lower-frequency applications such as wireless sensing [12]-[14], and very few studies of high-frequency performance have been performed [8],[15]. The first experimental demonstration of GHz-range graphene varactors was reported in 2016 by Moldovan, *et al.* [8], where the authors demonstrated top-gated varactors with Q up to 12 at 1 GHz and a tuning ratio (in vacuum) of 1.34. However, for many applications, such as automotive applications, much higher frequency operation is needed. Therefore, additional studies are needed to develop device geometries that can provide higher frequency performance.

Here, we report the performance of graphene varactors



Dev	L_g (μm)	N	Pitch (μm)	L_{ext} (μm)
D1	0.25	32	0.7	+0.05
D2	0.25	32	1.3	+0.35
D3	0.35	32	0.7	-0.05
D4	0.55	20	0.9	-0.10

FIG 1. (a) Top view schematic of the varactor geometry (top) with the parameters in devices: D1, D2, D3, D4 (bottom). W_g is 2.8 μm for all designs. This set of dimensions was chosen to study the effects of access resistance and overlap capacitance on varactor performance. (b) Cross-section schematic of the four designs. (c) Optical image of the active region of a D4 device. (d) Optical image of a varactor showing the GSG pad structure for RF measurements. (e) SSEC model of a graphene varactor.

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designed for extremely-high frequency operation. The devices use an inverted back-gate configuration which allows the gate dielectric to be nucleated directly on the gate metal, thus allowing extremely small equivalent oxide thickness to be obtained without having to resort to the use of seeding layers for dielectric growth on top of the graphene [16]. We also use a multi-finger structure and thick gate/contact metal to reduce series resistance, which has substantial effects on Q at high frequency. We evaluate the trade-offs of various device geometries and show that devices without overlapping contact and gate metal provide the best overall performance. With these design optimizations, we demonstrate varactors with a Q as high as 18.4 at 18 GHz and a $Q \times f$ product above 300 GHz.

II. DEVICE FABRICATION

The fabrication started with a substrate of high-resistivity silicon with 475 nm of SiO_2 on top to minimize substrate losses. The bottom multi-finger gates, illustrated by the dark green area in Fig. 1(a), were first defined by electron beam lithography followed by reactive ion etching 230-nm-deep trenches into the SiO_2, followed by evaporation and lift-off of Ti (10 nm) / Au (218 nm) gate metal. Lateral ion milling and oxygen plasma clean were performed next to remove any resist residue or metal "flags". Next, an 8-nm HfO_2 gate oxide layer was deposited using atomic layer deposition at 250 °C. Single-layer graphene grown by chemical vapor deposition was then transferred onto the HfO_2 using a PMMA-assisted aqueous transfer method. The graphene was then patterned and etched using an oxygen plasma to define the channel region. Finally, the contact metal consisting of Cr (10 nm) / Au (218 nm) was evaporated and lifted off. The thick gate and contact metal were used to minimize series resistance. Out of 60 devices fabricated, the yield was of 93.3%, with only 4 non-functional devices.

We explored four designs with different gate length, L_g, finger pitch, extension length, L_{ext}, and number of gate fingers N, as shown in Figs. 1(a)-(b). Two designs (D3 and D4) had overlapping gate/contact electrodes and thus negative L_{ext}, while in the other two designs (D1 and D2) gate and contact electrodes were not overlapping and thus had positive L_{ext}. The overlap is expected to decrease access resistance but increase fixed oxide capacitance. The study on the effect of overlap on Q and tuning ratio (TR) aims to provide important guideline for future device optimization of high-speed multi-finger varactors based on graphene or any possible 2D materials. All devices were fabricated in a ground-signal-ground (GSG) geometry for RF characterization. Optical images of the devices are shown in Figs. 1(c)-(d). Fig. 1(e) shows the small-signal equivalent circuit (SSEC) model of a graphene varactor. The SSEC model consists of an intrinsic capacitor C_{in} connected in parallel with a leakage resistance R_L, and then in series with a resistance R_S corresponding to access and contact resistances.

III. RESULTS

All devices were first characterized in air using a vector network analyzer with frequency up to 18 GHz, then subsequently measured in vacuum at 1 MHz using a semiconductor parameter analyzer, both at room temperature (RT), and then measured again at 1 MHz in vacuum, post bake-out, using semiconductor parameter analyzer at 77 K. Open-short deembedding [17] was performed for the high frequency measurement, and open-deembedding was performed for the low frequency measurement. The capacitance-voltage (C-V) curves from all measurements of a D2 device are shown in Fig. 2(a). For the two sets of low-frequency measurements at

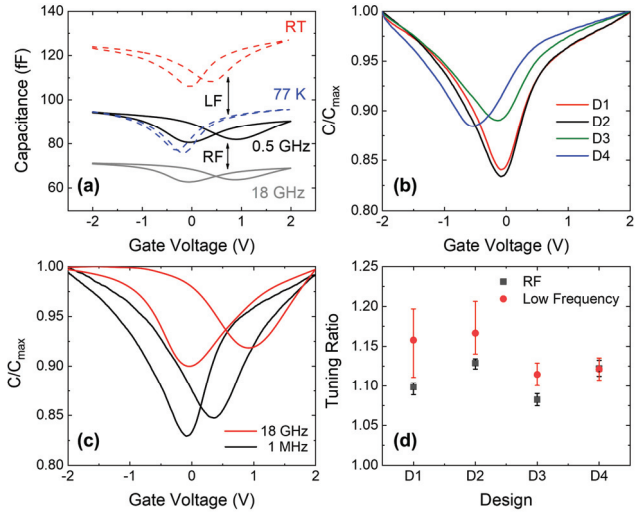

FIG 2. (a) Measured capacitance at 1 MHz in vacuum at room temperature (dashed, red) and 77 K (dashed, blue) of a D2 device, and extracted capacitance of the same device in air at room temperature at 0.5 GHz (solid, black) and 18 GHz (solid, grey). (b) Normalized C-V of the device with highest tuning ratio in each design at 1 MHz in vacuum. (c) Normalized C-V of the D2 device in (b) at 1 MHz and 18 GHz, both at RT. (d) TR of all devices at 18 GHz in air (black, squares) and 1 MHz in vacuum (red, circles), both at RT. Error bars show the minimum and maximum TR of devices with the same design.

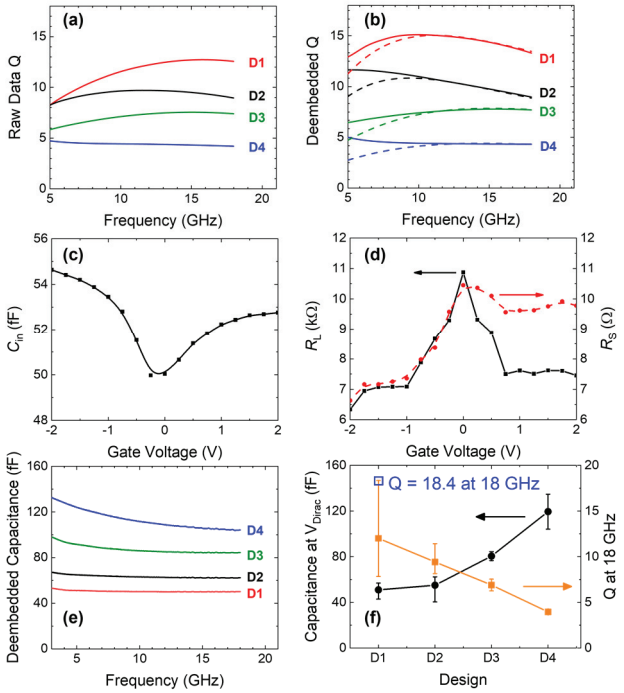

FIG 3. (a) Raw and (b) deembedded quality factor, Q. Dashed lines in (b) are from SSEC modelling. (c)-(d) Gate voltage dependent (c) intrinsic capacitance C_{in} and (d) leakage resistance R_L and series resistance R_S of the D1 device in (a-b) at 18 GHz. (e) Frequency dispersion of the capacitance at the Dirac point calculated from the deembedded S_{11}. (f) Calculated capacitance (black, circle) and quality factor (orange, square) at 18 GHz at the Dirac point. The error bars show the minimum and maximum values of devices with the same design. For (a),(b) and (e), results of the typical devices from each of the four designs are shown.

1 MHz, the room-temperature C-V curve shows a larger hysteresis and more positive Dirac voltage than at 77 K, which we attribute to the freeze out of border trap charging and discharging at or near the HfO_2/graphene interface [18]. The C-V curves at 0.5 and 18 GHz extracted from RT measurements are also shown in Fig. 2(a) for comparison. The high-frequency C-V curve measured at RT at 0.5 GHz has similar overall capacitance as the 1-MHz C-V curve measured at 77 K, which we attribute to the same moisture/border traps that produce the temperature-dependent-effects. At 18 GHz, the overall capacitance continues to decrease, which is consistent with the expected dielectric relaxation in HfO_2 [19].

We then compared the normalized C-V characteristics of the different designs at 1 MHz in vacuum, RT, as shown in Fig. 2(b). In the D3 and D4 designs, the contacts overlap the gate electrodes, and this results in lower *TR* due to the parasitic overlap capacitance. The normalized C-V characteristics of a D2 device measured at 1 MHz (RT) and 18 GHz are shown in Fig. 2(c). Compared to the 1 MHz measurement, the C-V characteristics measured at 18 GHz have larger hysteresis and more positive Dirac voltages. This is a result of the RF measurements being perform in air vs. vacuum for the low-frequency measurements. A comparison of the *TR* for all devices is shown in Fig. 2(d), confirming the trend that devices without metal overlap have higher *TR*.

The Q of the varactors was extracted from the s-parameters and evaluated as a function of frequency, bias and device configuration. The frequency trends of the raw and deembedded Q at the Dirac voltage are shown in Fig. 3(a)-(b, solid curves). Deembedding improves the Q at lower frequencies, while only a small increase is observed at higher frequencies.

The value of Q using the SSEC model in Fig. 1(e), can be expressed as

$$Q = \frac{1}{R_S \omega C_{in} + \frac{(1+R_S/R_L)}{\omega R_L C_{in}}}, \quad (1)$$

where $\omega = 2\pi f$ is the angular frequency. The peaked behavior in the deembedded Q in Fig. 3(b), is due to the competition of the two terms in the denominator of (1). A comparison of the designs provides insight into the limitations on Q. The overlapping contact and gate electrodes can reduce access resistance but increase fixed capacitance. Considering that Q is inversely proportional to the product of total resistance and capacitance at high frequency, lower Q for D3 and D4 compared to D1 and D2 shows that the decrease in resistance created by the overlap does not compensate the increase in fixed capacitance. This further suggests that the series resistance in our devices is dominated by contact resistance rather than access resistance.

TABLE I. EXTRACTED INTRINSIC CAPACITANCE AND RESISTANCE VALUES FROM DEEMBEDDED *S*-PARAMETERS AT THE DIRAC VOLTAGE AT 18 GHz.

Design	C_{in} (fF)	R_S (Ω)	R_L (kΩ)
D1	50.0	10.5	10.9
D2	62.4	13.0	6.3
D3	84.6	8.1	2.0
D4	103.0	12.2	0.95

We performed additional analysis to fit the SSEC model in Fig. 1(e) to our experimental s-parameter data. The simulated Q fits the measured deembedded Q at higher frequency, as shown in Fig. 3(b). We attribute the disagreement at lower frequencies to an increase in C_{in} due to dielectric relaxation, and at lower frequencies Q increases with increasing C_{in}, as in (1). The SSEC parameters are shown in Table I. The extracted series resistance confirms that the channel resistance has small impact on total resistance, and the lower leakage resistance for devices D3 and D4 implies that broken regions of the graphene may exist in the overlapping regions allowing the top contact metal to directly interact with the HfO_2. To consider the effect of gate voltage on the intrinsic values, SSEC modeling was performed at all gate biases for the D1 device. The results show a V-shaped C_{in}, and reverse V-shaped R_S and R_L, as shown in Figs. 3(c), (d). The high R_S at the Dirac voltage is due to graphene channel resistance modulation by the gate voltage, while we suspect that the resistance asymmetry around the Dirac voltage is due to p-type doping of the extension region [20].

Fig. 3(e) shows the frequency dispersion of the deembedded capacitance at the Dirac voltage, and Fig. 3(f) plots the extracted deembedded capacitance and Q at the Dirac voltage at 18 GHz for all devices. The plots show decreasing Q with increasing capacitance, which supports the argument that the contact resistance, not the access resistance limits the Q in our devices. We note that the device with highest Q is from D1, which has a gate length of 0.25 µm and an extension length of 0.05 µm. This device has a Q of 18.4 at 18 GHz, and a $Q \times f$ product above 300 GHz.

The Q vs. f at different bias voltages is shown in Fig. 4(a) for the D1 device in Figs. 3(a)-(e), while Q vs. V_g at 18 GHz of the device with highest Q is shown in Fig. 4(b). The smaller Q at the Dirac voltage can be attributed to the high channel resistance, and the large asymmetry is attributed to the p-type doping of the extension region [20].

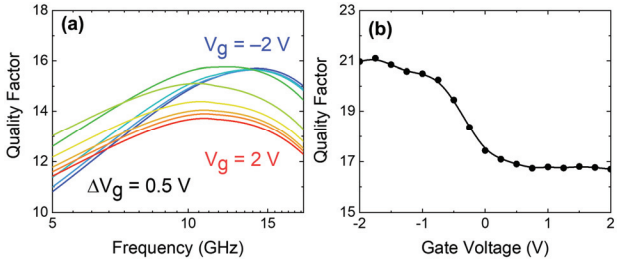

Fig. 4. (a) Q vs. f of the D1 device in Fig.3(a)-(e) at bias voltage from –2 V to 2 V. (b) Q vs. V_g of the device with highest Q in Fig. 3(f) at 18 GHz.

IV. CONCLUSION

In conclusion, we have performed a comprehensive analysis on design parameters for back-gated RF graphene varactors, with specific focus on the effect of gate/contact overlap on tuning ratio and quality factor. This report provides new insights into the design trade-offs of RF graphene varactors with a back-gated configuration. We achieved a Q of 18.4 at 18 GHz, which is a large improvement compared to previous RF graphene varactors. The results provide importance guidance for optimizing the design to enable in a variety of analog applications, or to be adapted to novel solutions such as integrating with ferroelectric materials and achieve varactors with non-volatile tuning. Several techniques are possible to further improve the tuning ratio and quality factor, including further reducing the HfO_2 thickness and using chem-mechanical polishing for the buried gate electrode.

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