High-Toughness Aluminum-N-Doped Polysilicon Wiring for Flexible Electronics

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***Abstract*—One of the essential requirements of any flexible substrate electronic system is the availability of reliable, high density, fine pitch interconnects between components. In this work, we demonstrate a high-toughness two-layer (aluminum, N-doped polysilicon) composite wiring scheme. The top aluminum layer carries most of the current while the polysilicon underlayer electrically bridges any cracks present on the top aluminum induced by flexing thus maintaining electrical conductivity even at very high stresses. When composite and Al control wires on a flexible tape were subject to 4000 cycles of bending, we observed that Al control wires fracture at a 2.5 mm radius of curvature but the composite wires maintain electrical conduction with an increased resistance.**

Keywords—flexible interconnects; transfer-printing; aluminum N-doped polysilicon interconnects; bend testing

I. INTRODUCTION

The wire interconnects in flexible electronic systems need to be robust enough to tolerate long-term static or dynamic, multi-axial strains put on the system. Hence, these interconnects are desired to be flexible, bendable, twistable, and stretchable yet the resistance of the wiring must be sufficiently low to carry high currents in many applications. High conductivity metals such as Cu, Au, and Al are the most suitable materials for the construction of wires; however, these materials are relatively rigid and cannot easily withstand the bending and stretching deformations generally experienced by flexible systems. Additionally, most metals experience severe cracking when deposited on compliant and much softer substrates due to relaxation of deposition residual stresses [1]–[4].

There are primarily two approaches in the literature for enhancing the flexibility of the interconnects. The first approach deals with improving the geometry of the interconnects while the other deals with utilizing novel materials or their combination with traditional interconnect materials. Different wire and substrate surface geometries have been used to improve the stretchability of wires made with conventional sputtered metals systems [5]–[14]. Different materials such as conductive polymers like Poly(3,4-ethylene dioxythiophene): poly(4-styrene sulfonate) (PEDOT:PSS) [15], and Polyaniline (PANi) [16], Ag-nanowire composites [17], and even liquid metals like eutectic gallium indium (EGaIn) [18] have been used to produce flexible interconnects. While all of these methods improve the survival of the wiring under bending and flexing, they introduce severe constraints on either the interconnect density, require a highly complex fabrication process, or cannot maintain high conductivity.

In this paper, we present a simple flexible wiring system that can produce fine pitch straight-line metal wires with high density that maintain low resistance even in the presence of strains that exceed the fracture strain of the metal. This is achieved by a composite wiring scheme consisting of a two-layer stack of a high-toughness conductive polysilicon underlayer and a top high-conductivity aluminum layer. Both of these layers consist of CMOS-compatible materials used for fabricating interconnects [14], [19]. The silicon underlayer provides a high elastic modulus surface for the Al growth. This results in the deposition of a continuous Al film without residual-stress-induced fractures thus eliminating one of the major sources of metallization failure on flexible substrates.

The resistance to bending without fracture for a uniform conductive wire film material can be determined from the film bending stress σ_s under bending by (1) [20]

$$\sigma_s = \frac{E \cdot h}{2R} \tag{1}$$

where E is the film Young modulus, h is the film thickness and R is the bending radius. The wire develops cracks when the stress exceeds the fracture strength.

Aluminum has Young's modulus of 69 GPa and fracture strength of 47 MPa. Polysilicon has Young's modulus of 160 GPa and fracture strength of 2.11 GPa [21], [22]. Thus, ideally for the 2 μm aluminum film, the maximum bending radius should be 1.61 mm but for the polysilicon film should be around 34 μm. Therefore the resistance to cracking of polysilicon is much higher than that of Al. On the other hand, the calculated sheet resistance of Al is very low in the order of 28 mΩ/□ while for heavily doped silicon is much higher 7.2Ω/□.

We can obtain the benefits of the high strength of polysilicon underlayer and the low resistance of the Al upper layer together with the observation that when the Al fractures, the width of the fracture crack is extremely small, a few nanometers [23]. Because the crack width is so small it is possible to shunt the fracture with the polysilicon layer below without much increase in the wire resistance. For example, a 50 nm-wide crack shunted by the polysilicon underlayer on a 10 μm-wide wire produces approximately 0.025 Ω/crack. It is thus possible to maintain low wire resistance even after many cracks in the aluminum develop.

Fig. 1 below illustrates the basic principle of the two-layer composite shunting metallization and the resulting electrical equivalent of the wire under fractures in the Al top layer. An additional layer of silicon dioxide is added at the bottom as a

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result of the fabrication and transfer process discussed in the next section.

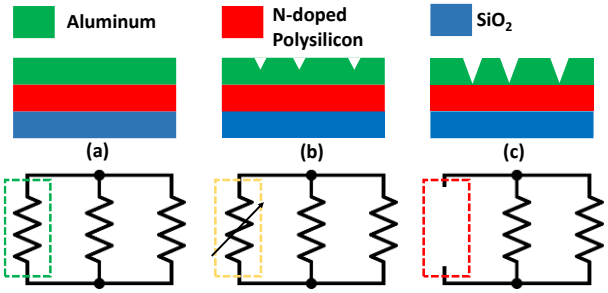

Fig. 1. Working principle of interconnects stack. (a) No cracking, therefore resistance dominated by aluminum. (b) Aluminum cracks and resistance increases. (c) Aluminum crack deepens and resistance is dominated by doped polysilicon.

The basic idea of shunting of a metallic film by a flexible conductive layer has been previously shown with a stacked Au wire with an underlying conductive PEDOT:PSS layer [15]. Our new two-layer scheme provides a lower shunt resistance and lower wire resistance due to the lower resistivity of doped polysilicon compared to PEDOT:PSS. Furthermore, our new methods also prevents process induced cracking [1] of the metal due to the high Young modulus of polysilicon compared to the soft PEDOT underlayer.

II. Experimental

A. Fabrication Process

We have fabricated the wire structures on a silicon carrier substrate and then transferred the composite wires to a flexible substrate. The simplified fabrication process on the carrier wafer is shown in Fig. 2.

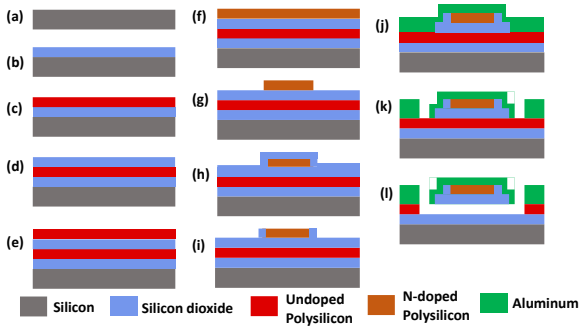

Fig. 2. Flexible composite wire fabrication process flow

First, 400 nm thermal silicon dioxide was grown on a bare silicon mechanical wafer using wet oxidation at 1050°C. This layer is used as an etch-protection barrier for the substrate during the final dry release process. Next, 2 µm undoped sacrificial polysilicon was deposited using low-pressure chemical vapor deposition (LPCVD). Then, 700 nm of thermal SiO_2, was grown on this polysilicon layer using wet oxidation. This oxide layer serves to protect the wires from the final dry etch. Following this, 1 µm polysilicon was deposited using LPCVD. The polysilicon was then N-doped using solid source phosphorus doping and annealed at 1050 °C for 2 hours. This N-doped polysilicon is the underlayer of the wire stack. After doping, a final sheet resistance of 7.2 Ω/□ was measured using a 4-point probe. The polysilicon was next dry etched with SF_6 using the RIE technique to pattern the 10 µm wide wires. The poly-Si was then thermally oxidized at 1050 °C for 60 minutes. This results in the top surface and the sidewalls of the wire getting oxidized. The oxide from the top surface was selectively etched using Ar-ion milling. The oxide layer was then lithographically patterned and etched using BOE. The patterned oxide layer was wider (24 µm) than the polysilicon layer to provide complete protection during dry release.

A 2.2 µm aluminum film was sputter deposited. The aluminum was then lithographically patterned using using an aluminum etchant (Transene). The aluminum wire was kept wider (38 µm) than the oxide to facilitate complete encapsulation of the N-doped polysilicon with aluminum. Rapid thermal annealing (RTP) was performed at 450 °C for 146 s (80 s ramp up followed by 60 s steady temperature) to form a thin Al-Si alloy at the interface. The wafer was then diced into smaller pieces. Next the wires were dry released using 50 cyles (with an etch-time of 11 seconds per cycle) isotropic XeF_2 etching at a pressure of 1 Torr. Tapered aluminum tethers held the wires in place during the etch and purge-cycles. The bond pads of the wires were also designed to be of the same width as the wires in grid configuration to facilitate their simultaneous release. Control Al samples which featured only single-layer Al wires, (without any doped poly-Si), of identical dimensions were also fabricated.

B. Transfer Printing on a Flexible Substrate

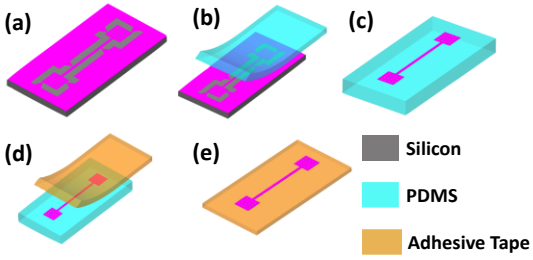

Fig. 3. (a),(b) Wire transfer from a rigid silicon substrate to a PDMS stamp. (c), (d) Wire transfer from PDMS stamp to flexible adhesive tape.

A 2-step transfer approach shown in Fig. 3 is utilized for both the stacked wire and the control samples. First, a polydimethylsiloxane (PDMS) stamp is placed on the silicon substrate to make conformal contact with the wires. It is then retrieved rapidly to take advantage of the rate-controlled adhesion of elastomers [24]. Second, a strip of adhesive tape (Scotch Magic Tape) is cut and placed adhesive side down on the PDMS stamp containing wires, and conformal contact is established. The adhesive of the tape is stronger than the adhesion between aluminum on the stacked wire and PDMS. Hence, the wire gets transferred to the flexible substrate when detached from the stamp. The area where the wires are not

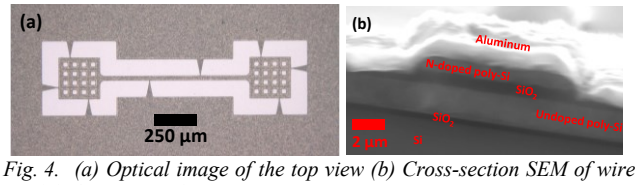

Fig. 4. (a) Optical image of the top view (b) Cross-section SEM of wire stack before XeF_2 release

attached is covered with another piece of tape to avoid the tape sticking to the bending apparatus.

The mold for the stamp was prepared by laser cutting and gluing together an acrylic sheet. The mold was then glued to a glass slide coated with FluoroPel™ 800 1% (purchased from Cytonix) to form a hydrophobic Teflon film to enable the easy release of PDMS. PDMS (Sylgard® 184) was mixed in a 10:1 ratio of base to curing agent, degassed, and then poured into the mold (2 cm * 2 cm * 8 mm). Another Teflon-coated glass slide was placed on the top to achieve the flatness required for transfer printing. PDMS was then cured at 150 °C for 30 minutes. The stamp is then released from the mold. A glass slide and the stamp are treated with atmospheric plasma for 2 minutes and then bonded together under a weight at 120 °C for 2 hours. This glass backing helps to avoid unintentional stretching, i.e., putting tensile strain on the wires during stamp retrieval. Fig. 4 (a) and (b) shows the optical image of the top and high-resolution SEM image of the cross-sections of a composite wire structure, respectively.

C. Bend Testing Setup

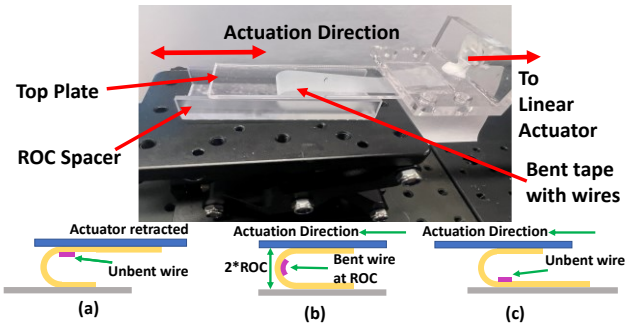

Fig. 5. Schematic representation of one complete cycle of wire-bending.

A cyclic bend testing setup was built to test the bendability of the wires over different radii of curvatures. Bending was performed over 10 mm, 7.5 mm, 5 mm, and 2.5 mm radii of curvatures. One half cycle corresponds to bending the wire once. Resistance of the wires was measured using an HP 4145b semiconductor parameter analyzer connected to a probe station, before bending and after every 1000 cycles of bending for each radius of curvature, up to 4000 cycles. The setup utilized two lab jacks, an Arduino UNO board, a linear actuator (L16-R, Actuonix), a dc power supply, and 3D printed structures serving as two plates. The bottom plate had side supports matching the height of the diameter of curvature, and the top plate, attached to the linear actuator, slid over this support to maintain precise bending radii of curvatures.

III. Results

The resistance of the transferred wires under ROCs 7.5 mm, 5 mm and 2.5 mm was monitored as a function of the number of bending cycles. As shown in Fig. 6 (a) the change in resistance for the control and wire stack was below 3% over 4000 bending cycles for a bending ROC of 10 mm. For 7.5 mm ROC (Fig. 6 (b)), the change in resistance was below 5% over 4000 cycles. For 5 mm ROC, cracks in the control wire could be seen throughout the length of the wire, perpendicular to the bending direction. As a result, a significant change in resistance was observed. For the wire stack however, after 4000 cycles, the change in resistance was limited to less than 15% increase. At 2.5 mm ROC, the control samples exhibited complete fractures after 3000 cycles. The resistance of the wire stack also increased to about four times the initial resistance due to the presence of shunted cracks on the Al , but it maintained electrical conductivity as intended.

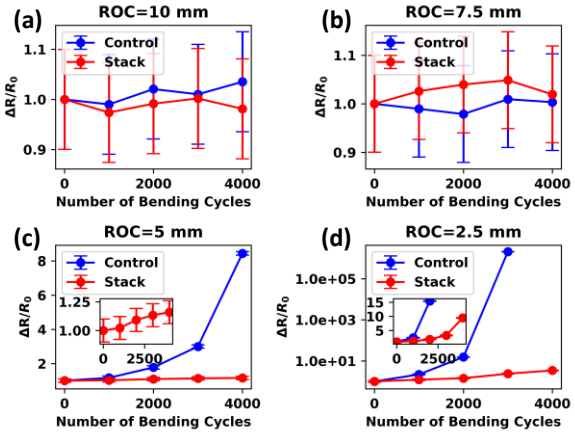

Fig. 6. Change in resistance over 4000 bending tests for 2.5 mm, 5mm, 7.5mm, and 10 mm radii of curvature.

The standard deviation bars are representative of fluctuations in contact-resistance due to the grid-like structure of our contact-pads. However, these fluctuations are minor in comparison with the bending induced increase in resistance as shown in Fig. 6(c-d). Fig. 7 shows optical images of, the control and the stacked wire before and after 4000 bending cycles. The uniform control wire displays a catastrophic fracture and loss of electrical conductivity at 2.5 mm bend radius, whereas negligible cracks were observed on the Al/poly-Si composite stack, thus confirming the reduction in crack formation and the integrity of the wire electrical conductivity due to the presence of the poly-Si underlayer. No delamination was observed during the tests.

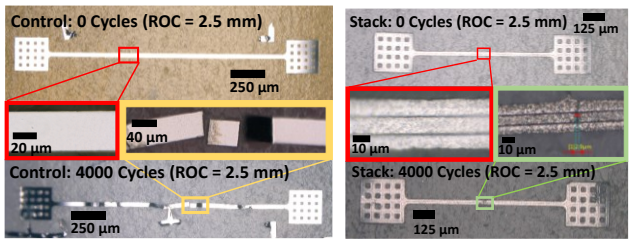

Fig. 7. Optical images of the control and wire stack, before and after 4000 cycles of bending experiments.

IV. Conclusion

In this work we demonstrate a high-toughness composite two-layer wiring scheme consisting of a layer of Al and an underlayer of conductive n-doped polysilicon. Straight composite wires were relatively crack-free and able to maintain low resistance and high electrical conductivity even after 4000 cycles of 2.5 mm radius bending while the control pure Al wire fracture at 2.5 mm radius bending. Such a fabrication scheme can be easily utilized for building flexible wire systems and flexible PCBs for a plethora of applications which require high-density and high-conductivity flexible wires such as smart-contact lens sub-systems [25]–[33].

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