High-Voltage Triboelectric Energy Harvesting Using Multi-Shot Energy Extraction in 70-V BCD Process

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***Abstract*—Triboelectric Nanogenerators (TENG) suitable for mechanical energy harvesting typically have ultra-high open-circuit voltage in several hundreds of volts, challenging the energy extraction circuit (EEC) design required for charging load battery/capacitor. Here, we present a novel multi-shot switched EEC that extracts energy in multiple discrete steps to regulate the TENG voltage below the breakdown limit of the technology (70 V in our case), making it suitable for Integrated Circuit (IC) implementation. The proposed strategy maintains high TENG voltage just below the breakdown limit to offer a high electrostatic retardation, enhancing the work done against it by the mechanical source in the form of transduced electrical energy. Mathematical derivation of the circuit's output shows a constant transduction power at all load voltages, fully eliminating Maximum Power Point (MPP) Tracking and saving power for the same. The design and simulation of the proposed EEC in TSMC 0.18 μm BCD process achieve a maximum power conversion efficiency of 63.3% and a 1.91x gain over even an *ideal* conventional Full Wave Rectifier (FWR) circuit at its optimal MPP load (gain will be higher for a real FWR implementation).**

***Index Terms*—Switched circuits, transducers, energy harvesting.**

I. Introduction

TRIBOELECTRIC Nanogenerators (TENGs) have received significant recent interest for harvesting ambient mechanical energy to prolong the battery-life of low-powered Internet of Things (IoT) devices. TENGs enjoy the advantage of wide material choice and versatile operating modes over other types of ambient mechanical energy transducers [1].

In practical applications, an Energy Extraction Circuit (EEC) is required to rectify the TENG's AC output to charge a DC load. Also, during the cyclic operation of TENG, the EEC architecture/operation together with load-voltage affect the TENG voltage/charge, influencing the TENG's electrostatic retardation force. The work done by the ambient mechanical force against this electrostatic retardation is the transduced electrical energy (denoted $E_{T,cycle}$ per cycle), and so the choice of EEC and load-voltage determine the transduced energy or equivalently, the average output power ($P_T = E_{T,cycle} \times f_e$, with f_e denoting the average source frequency). The Power Conversion Efficiency (PCE) is the fraction of P_T power delivered to the load (P_L), i.e., PCE $= P_L/P_T$. To this end, several EEC architectures have been explored in the literature and their corresponding optimal loads have been derived to enhance P_T and PCE [2], [3].

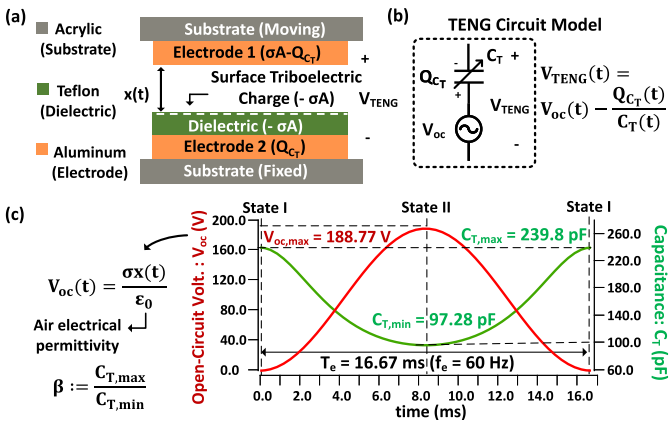

Fig. 1. (a) Cross-section schematic of a standard contact-separation TENG, (b) its lumped circuit model, and (c) the plot of TENG parameters used for simulation in this brief.

For normalized comparison of an EEC, the standard Full Wave Rectifier (FWR) circuit acts as the reference. FWR's MPP analysis shows that the P_T is maximized for load voltage, $V_{L,MPP}^{FWR} = \frac{V_{oc,max}}{2(\beta+1)}$ [4], where $V_{oc,max}$ denotes TENG's maximum open-circuit voltage and is achieved when the two plates of the contact-separation TENG (shown in Fig. 1(a)) are maximally apart (State II in Fig. 1(c)); the TENG capacitance (C_T) also varies during the operation, and the parameter β denotes the ratio of maximum to minimum TENG capacitances achieved respectively at State I (plates in contact) and State II (plates maximally separated). For a TENG with experimentally measured parameters as in [4], and used in this brief (see Fig. 1(c) for values), the FWR MPP load is calculated as 27.2 V. The corresponding time-varying TENG voltage waveform simulated under *ideal conditions* is shown in purple in Fig. 2(a). The transduced per-cycle energy ($E_{T,cycle}$) of the

Manuscript received February 8, 2022; accepted March 14, 2022. Date of publication March 18, 2022; date of current version May 3, 2022. This work was supported in part by the U.S. National Science Foundation under Grant NSF-CSSI-2004766 and Grant NSF-PFI-2141084, and in part by the Iowa State University under Regents Innovation Fund. This brief was recommended by Associate Editor D. Chen. *(Corresponding author: Madhav Pathak.)*

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Color versions of one or more figures in this article are available at https://doi.org/10.1109/TCSII.2022.3160676.

Digital Object Identifier 10.1109/TCSII.2022.3160676

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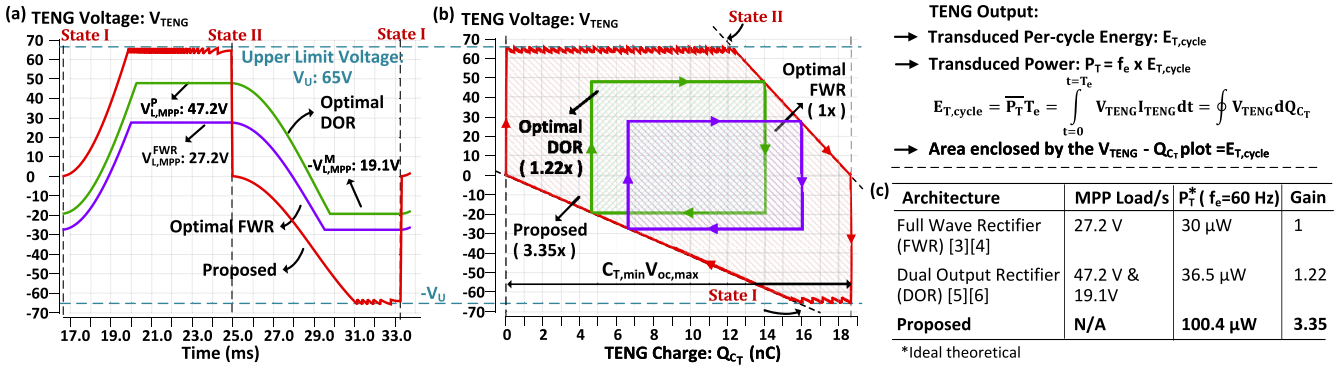

Architecture	MPP Load/s	P^*_T (f_e=60 Hz)	Gain
Full Wave Rectifier (FWR) [3][4]	27.2 V	30 µW	1
Dual Output Rectifier (DOR) [5][6]	47.2 V & 19.1V	36.5 µW	1.22
Proposed	**N/A**	**100.4 µW**	**3.35**

*Ideal theoretical

Fig. 2. (a) The time-varying TENG Voltage (V_{TENG}) waveforms of load-optimized FWR, load-optimized DOR, and the proposed circuit for one periodic operation cycle; (b) corresponding TENG Voltage- Charge ($V_T - Q_{C_T}$) plots. (c) Calculated transduced power (P_T) for the circuits under ideal implementation.

ideal FWR EEC can be visualized as the area enclosed by the TENG voltage-charge (V_T-Q_{C_T}) plot shown in purple in Fig. 2(b). The corresponding transduced power at $f_e = 60$ Hz (typical excitation frequency for a machine health monitoring IoT) is listed in Fig. 2(c) and serves as a baseline for comparison with the proposed architecture of this brief.

A. EEC ICs for TENG and Our Contribution

Only a handful of EECs have been designed on-chip for TENG, such as [5]–[8], primarily due to the challenge with its high voltage. In [5], a FWR followed by a switched capacitor charge pump (SCCP) is implemented in 65 nm CMOS technology. However, the operating voltage is restricted by their used technology to 2.5 V, and hence the typically high MPP load ($V^{FWR}_{L,MPP} = \frac{V_{oc,max}}{2(\beta+1)}$) cannot always be achieved. Thus, this implementation's P_T shall actually be smaller than that of the load-optimized FWR listed in Fig. 2(c).

The two half-cycles in TENG operation, i.e., separation (State I→II) and retraction (State II→I) of the TENG plates, are asymmetric due to the varying TENG capacitance (refer green curve in Fig. 1(c)). Hence, [6], [7] implemented a dual-output rectifier (DOR) followed by a dual-input buck converter in 70 V, 0.18 μm BCD node that offers a separate MPP load for each half-cycle. The two MPP loads (denoted $V^P_{L,MPP}$ and $V^M_{L,MPP}$) calculated for our test TENG with this approach are marked in the green curve of Fig. 2(a). Also, its transduced $E_{T,cycle}$ is co-plotted in green in Fig. 2(b) and its corresponding P_T is tabulated in Fig. 2(c).

We note that other techniques such as parallel synchronized switching harvesting on inductor (P-SSHI), that pre-bias (pre-charge) the TENG, can exceed the load-optimized FWR output, with [8] reporting an experimental gain of 1.62x over the FWR in 70 V, 0.18 μm BCD process. However, similar to FWR, P-SSHI's P_T also shows a parabolic power response to the load-voltage with optimal load typically equal to several times the $V_{oc,max}$ [4], making it challenging to implement on-chip. Another alternative is Synchronous Charge Extraction (SCE) circuit [9] that is CMEO (Cycle for Maximized Energy Output) [10] optimal guaranteeing at least a 4x gain over load-optimized FWR, but only under no constraint on operational voltage, making it again impractical for chip implementation.

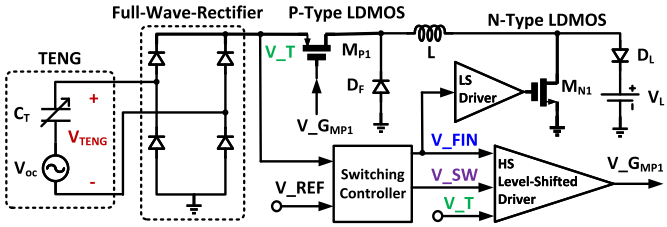

Fig. 3. Schematic block diagram of the top architecture.

In this context, we propose an optimal voltage-constrained SCE approach with a multi-shot operation.

The main *contributions* of this brief are 1) A new multi-shot energy extraction method that optimizes the transduced power (P_T) within the given voltage-constraint (IC technology's breakdown voltage); 2) Mathematical derivation of the per-cycle transduced energy (equivalently, power) that turns out to be independent of load-voltage, obviating the need for separate MPP tracking (unlike FWR, Parallel/Series-SSHI circuits [4]); 3) Circuit implementation in 70 V BCD process achieving net PCE of 63.3%, a 1.91x gain over even an ideal load-optimized FWR.

II. Proposed Circuit Operation and Analysis

The proposed circuit architecture shown in Fig. 3 functions with the High-Side (HS) PMOS switch M_{P1} and Low-Side (LS) NMOS switch M_{N1} being normally off, and are enabled only for brief periods to extract the stored charge (equivalently, energy) from the TENG. The circuit operation commences with the two TENG plates together (State I in Fig. 1(c)), and as they separate, the TENG voltage rises in open-circuit condition (the 'red' curve in Fig. 2(a)). On reaching the upper limit voltage (V_U), selected as 65 V for a safety margin of 5 V from the breakdown voltage, as sensed by a comparator, the controller closes the HS PMOS switch for a brief period to start the "buck" action, transferring a part of the energy to the inductor L and load battery V_L, thereby reducing the voltage below but close to V_U. Subsequently, on opening the PMOS switch, the remaining stored energy on L is moved to the load via the freewheeling diode, D_F. This partial energy extraction is executed repeatedly at each instance the rectified V_{TENG}

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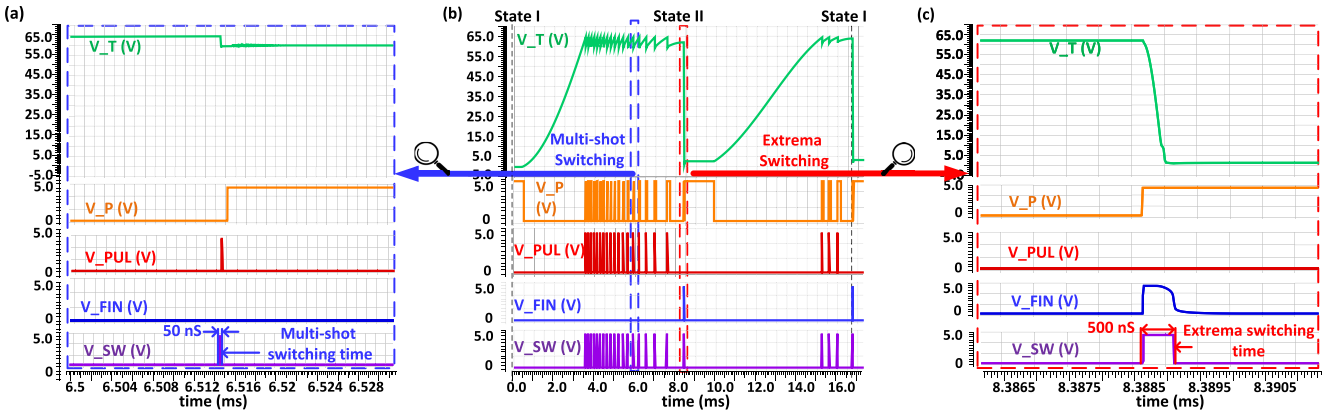

Fig. 4. (a) Zoomed-in view of various control signals and the rectified TENG voltage (V_T) during one of the multi-shot switching step. (b) Various controller signals and V_T during one operation cycle. (c) Zoomed-in view of various control signals and V_T during the extrema switching at State II.

reaches V_U (=65 V) limit, and hence the name "multi-shot", signified by the "see-saw" portion of the red-curve in Fig. 2(a). The rationale for maintaining ~65 V rather than extracting all the built-up energy (and letting TENG voltage fall to zero) is to maintain a higher electrostatic retardation to enhance the net transduced energy. Eventually, when the two TENG plates are maximum apart, i.e., at the end of the first half-cycle (State II), the peak value prior to the continued dropping voltage is sensed by a peak detector circuit, closing the PMOS as well as the NMOS switch for sufficient time ($\geq$ 1/4th the $LC_{T,min}$ oscillator time-period) to extract the energy until the voltage falls to zero. Subsequently, with the start of the second half-cycle (Fig. 2(a)), V_{TENG} rises in negative polarity and, post its rectification by the FWR, undergoes the same-as-before multi-shot energy extractions to regulate the voltage at V_U. Finally, at the end of the operation cycle (State I), all the energy on C_T is extracted, resetting the TENG for a new cycle. Note since the TENG capacitance is small, varying between $C_{T,min} = 97.28$ pF and $C_{T,max} = 239.8$ pF, and the inductor L is chosen to be 400 μH, the switch-on times ($\sim\pi\sqrt{LC_T}/2 \leq 0.5$ μs) are negligible compared to the TENG operation time ($T_e = 16.67$ ms).

The proposed multi-shot operation can also be understood visually from the red V_T-Q_{C_T} plot of Fig. 2(b) as the strategy to maximize the enclosed area (equivalently transduced per-cycle energy) with the constraint of 65 V as the upper limit. From the same plot, the per-cycle transduced energy for the proposed circuit can be derived as, $E_{T,cycle} =$

$$\begin{cases} C_{T,min}V_U\left[2V_{oc,max} - \frac{1}{2}(1+\beta)V_U\right], & V_U \leq \frac{V_{oc,max}}{\beta} \\ C_{T,min}V_U\left[V_{oc,max} - \frac{1}{2}V_U\right] & \\ \quad + \frac{1}{2\beta}C_{T,min}V_{oc,max}^2, & \frac{V_{oc,max}}{\beta} < V_U < V_{oc,max} \\ \frac{1}{2}\left(1+\frac{1}{\beta}\right)C_{T,min}V_{oc,max}^2. & V_U \geq V_{oc,max} \end{cases} \quad (1)$$

For this brief, the first case applies as $V_U = 65$ V is less than $V_{oc,max}/\beta = 76.43$ V, and as per it, the calculated $E_{T,cycle}$ is 1.674 μJ which corresponds to P_T of 100.4 μW at $f_e = 60$ Hz. From Fig. 2(c), this translates to a 3.35x gain over the load-optimized FWR (in ideal conditions). Fig. 5(a) plots $E_{T,cycle}$ as a function of TENG's $V_{oc,max}/V_U$ with demarcation between the above-defined three cases under $\beta = 2.47$ (as per the TENG used in this brief). Also from the inset of Fig. 5(a), note the three distinct V_{TENG} waveforms: The multi-shot operation occurs only during the first-half cycle in the second case, while the third case equals the SCE circuit case [9] (when $V_U \geq V_{oc,max}$, the switching occurs only at the extremes as in a normal SCE circuit [9]). Further, from the above equations, it is evident that the transduced energy (equivalently, power) is independent of the load-voltage, another novelty of the proposed circuit, obviating the need for a separate MPP circuit (thereby avoiding its overhead loss).

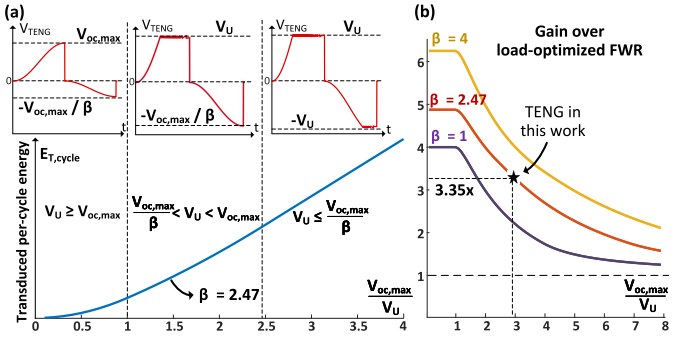

Fig. 5. (a) Transduced per-cycle energy vs. ratio of maximum open-circuit voltage to breakdown voltage: $V_{oc,max}/V_U$ at max. to min. TENG capacitance ratio, $\beta = 2.47$. (b) Gain over load-optimized FWR at β =1, 2.47, and 4 vs. $V_{oc,max}/V_U$.

The gain of proposed circuit over load-optimized FWR obtained by dividing the $E_{T,cycle}$ of Eq. (1) with optimized FWR's output, E_{MPP}^{FWR} [4] is as below:

$$\text{Gain} = \frac{E_{T,cycle}}{E_{MPP}^{FWR}}, \text{ where } E_{MPP}^{FWR} = \frac{C_{T,min}V_{oc,max}^2}{2(1+\beta)}, \quad (2)$$

and is plotted in Fig. 5(b) for three different values of β over a range of $V_{oc,max}/V_U$ values. The gain is always greater than 1 for any set of TENG parameters.

III. Proposed Circuit Implementation

The proposed circuit shown in Fig. 3 comprises of on-chip 70 V rated diodes, a P-Type LDMOS for the HS switch, a N-Type LDMOS for the LS switch, and a 400 μH inductor with

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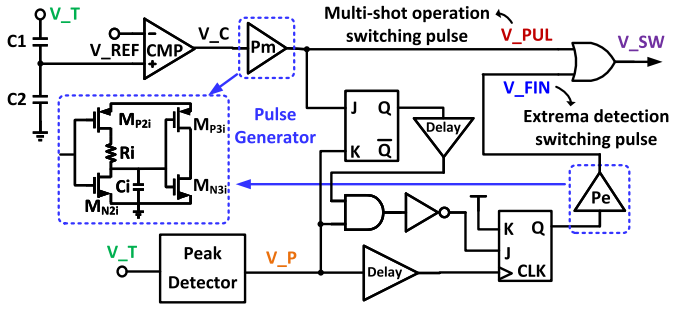

Fig. 6. Schematic block diagram of the switching controller.

ESR of 1 Ω. The circuit is designed for handling the expected ∼100 μW power level. The top-level simulated waveforms for one operation cycle are shown in Fig. 4(b).

A. Switching Controller

The role of switching controller in Fig. 3 is to generate two types of gate voltage pulses: *multi-shot operation* switching pulses on sensing V_U (=65 V) and the *extrema-detection* switching pulses at the two TENG operation extrema of States I and II. As shown in Fig. 6, rectified TENG voltage (V_T) is scaled down using a voltage divider and fed to a comparator whose output (V_C) on sensing 65 V, triggers Pm, the pulse generator unit (Fig. 6). The required multi-shot operation switching signal (V_PUL) with a fixed pulse-width of ∼50 ns is generated by setting the RC values of Pm and is passed on as the controller's output (V_SW). Fig. 4(a) shows the zoomed-in view of one of the multi-shot switching instances with the fall of V_T from 65 V to ∼60 V due to this switching step.

For the switching at the two extrema of States I and II, a peak detector circuit inspired from [11] and modified to suit the current application is used. The zoomed-in view of this switching process is shown in Fig. 4(c). The peak detector triggers the required switching pulse (V_FIN) with a width sufficient for the TENG voltage (V_T) to reach zero at both States I and II. For our TENG parameters, it is set to ∼500 ns using the pulse generator unit Pe (Fig. 6). Note that the transition of V_T from 65 V to 60 V during multi-shot switching creates a local maxima that unnecessarily triggers the peak detector (V_P in Fig. 4(a)) and to avoid issuing a spurious switching pulse (V_SW) through the V_FIN route, additional logic using gates and flip-flops is added as in Fig. 6.

B. Level-Shifted High-Side PMOS Driver

The level-shifted driver shown in Fig. 7(a) is utilized to switch the HS PMOS M_{P1} (see Fig. 3) since its source terminal is connected to the floating V_T signal. As in Fig. 7(a), for the multi-shot switching, the transistor M_{N6} is enabled to raise the gate signal level through the V_T fed resistor divider R3-R4. The divider ratio is chosen to pull down the gate (V_GMP1) ∼5 V lower than V_T to fully turn on M_{P1} as V_T transitions from 65 V to 60 V. However, the extrema switching requires the V_T to fall fully to zero. This leads to the $|V_{gs}|$ set by the fixed R3-R4 divider falling short of fully turning on M_{P1} at a low V_T value (refer 'blue' waveform in Fig. 7 (b)), in turn, increasing the PMOS conduction losses. Hence, to

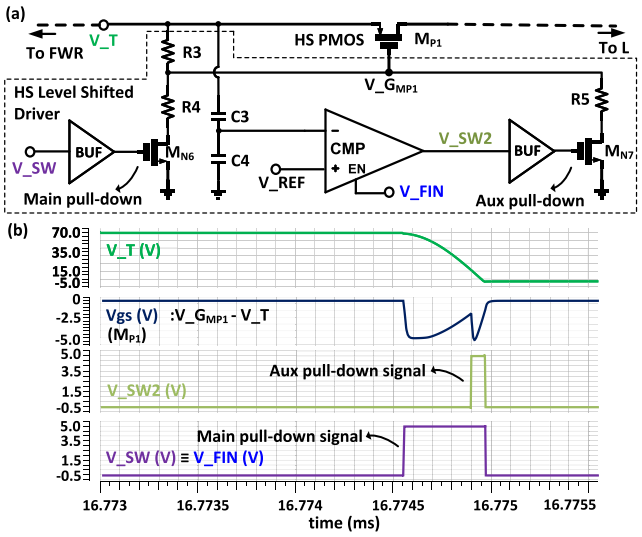

Fig. 7. (a) High-Side Level-Shifted driver circuit diagram and (b) zoomed-in view of switching signals and the V_{gs} voltage of M_{P1} during the extrema switching at State I.

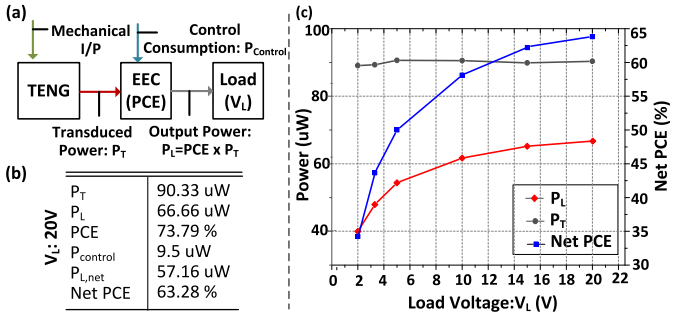

Fig. 8. (a) Overall power flow diagram. (b) List of simulated EEC performance metrics at 20V load-voltage (V_L). (c) Plot of simulated transduced power (P_T), load (output) power (P_L) and Net Power Conversion Efficiency (Net PCE) against load voltage (V_L).

achieve "adaptive divider ratio" during extrema switching, an auxiliary path is designed as shown in Fig. 7(a): Here using a comparator, V_T falling below 10 V is detected and the resistor R5 is activated (using V_SW2 signal) to increase the $|V_{gs}|$ for M_{P1}. The comparator here is enabled only during the extrema switching to reduce its average quiescent power consumption. The zoomed-in view of this switching process at State I is shown in Fig. 7(b). The size of M_{P1} and the driver design have been optimized for maximum PCE.

IV. Simulation Results

The presented circuit for triboelectric ambient energy harvesting is for *low frequency* (f_e= 60 Hz) and *low power* (in microwatts) operation and hence, any added parasitics in the post layout simulations are expected to have a negligible impact. For validating this, we layout the most *critical circuit blocks*, namely, peak detector, comparators in the controller, and the HS level-shifted switch driver, and report the post-layout simulation results for the TENG with parameters marked in Fig. 1(c). The proposed circuit transduced $P_T = 90.33$ μW of power and delivered $P_L = 66.66$ μW to the load at PCE of 73.79% (for the load-voltage of $V_L = 20$ V as listed in Fig. 8(b)). Note that the mathematically calculated

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TABLE I
PERFORMANCE COMPARISON WITH REPORTED ICS FOR TENG

Ref/Parameter	JSSC'19 [6]	JSSC'20 [7]	TCAS-I'20 [8]	This Work[a]
Process	0.18 μm 70V BCD	0.18 μm 70V BCD	0.18 μm 70V BCD	0.18 μm 70V BCD
Energy Extraction Method	Dual output rectifier with MPPT	Dual output rectifier with integrated MPPT	P-SSHI	Multi-shot SCE
MPPT Requirement Operation freq. [Hz]	Yes 50	Yes 40 - 60	Yes 1 - 5	No 60
# Off-chip LR components	1L (1 mH)+ 4R (30 GΩ)	1L (10 mH)	2L (1 mH)	1L (0.4 mH)
Input Voltage [V]	3.5 - 70	$<$ 70	12 - 70	$<$ 70
Transduced[b] (Input) Power [μW]	4.5 - 20.7	3.9 - 10.5	2214	90.33
Output Voltage [V]	2 - 5[c]	2.8 - 3.3[c]	2	2 - 20[c]
Net Output[b] Power [μW]	10.95	4.22	772	57.16
Peak Net PCE [%]	54.5	84.7	32.71[d]	63.28
Transduced Power Gain over FWR	1.11$\times$[a]	N/A	1.62$\times$	$>$ 1.91$\times$

[a] Simulation Results; [b] At Peak PCE; [c] Unregulated; [d] Including the output voltage regulation stages.

P_T of 100.4 μW is for idealized implementation corresponding to a constant $V_U = 65$ V during the multi-shot operation. It is intuitive from the V_T-Q_{C_T} plot of Fig. 2(b) that in real implementation with a finite multi-shot switching ripple voltage of $\sim$5 V, transitioning between 65 V and 60 V as in Fig. 4(b), the area under the V_T-Q_{C_T} is gets diminished leading to a lower P_T. Note the trade-off of increasing P_T by a reduction in the V_T ripple is in the form of higher switching loss due to an increased number of switching instances that eventually reduce P_L.

The flat response of the transduced power (P_T) to the varying load voltage (see Fig. 8(c)) validates the mathematized load-voltage agnostic power extraction behavior of the proposed EEC. The mild dependence of the output power (P_L) on V_L at lower values of V_L seen in Fig. 8(c) is primarily due to the voltage drop across the two diodes (D_F and D_L) of $2V_D \approx 1.5$ V that reduces the P_L by roughly the factor of $\frac{V_L}{V_L+2V_D}$, which manifests more significantly at lower V_L.

All of the active controller circuit components are powered at 5 V supply voltage and consume an overall power of $P_{control} = 9.5$ μW, yielding the net output power of $P_{L,net} = 57.16$ μW with net PCE of 63.28%. The operation with output voltage in the range of 2-20 V is verified as in Fig. 8(c); however, it can be set upto V_U. Note the presented battery charging application does not require voltage regulation as also in [6], [7], but if demanded by the application, a second stage inductive or capacitive switched-converter can be integrated for output voltage regulation. With the DC-DC converter's expected efficiency of 85%, the output power with regulated voltage can be expected to be 48.58 μW, offering an end-to-end PCE of 53.78%.

A comparison with prior chip-level designs for TENG energy extraction is provided in Table I. Note since the goal is to maximize the power extracted from the given transducer, the *Transduced Power Gain* over the standard FWR circuit is the key figure of merit for a normalized comparison. The proposed implemented circuit achieves a net 1.91x Transduced Power Gain over even the *ideal* FWR's P_T of 30 μW at its MPP load (gain shall be higher with respect to a real FWR owing to the MPPT overhead consumption and the parasitic losses). When compared to the methods of [6] and [7], the net 1.91x gain is also higher than even their ideal-circuit theoretical gain of 1.22x (refer Fig. 2(c)), clearly showing the superiority of the proposed method over [6] and [7].

V. CONCLUSION

This brief presents an IC design in a 70 V BCD process of a universally optimized voltage-constrained synchronous charge extraction (SCE) energy extraction circuit (EEC) for the Triboelectric Nanogenerator (TENG) transducers. The proposed strategy addresses the challenge of TENG's high open-circuit voltage nature by extracting energy in multiple short bursts (termed "multi-shot" operation) at the upper (breakdown) voltage limit of the given IC technology. Additionally, the constant level of transduced power of the proposed EEC design, regardless of the load-voltage, automatically offers MPP tracking, unlike the case of other EECs such as FWR, P-SSHI, S-SSHI, etc. Mathematical derivation of the proposed EEC's transduced power revealed a 3.35x gain over the load-optimized FWR circuit using our test TENG parameters at an operating upper limit of 65 V. The simulation of the proposed EEC in TSMC 70 V BCD process showed a net output of 57.16 μW at 20 V load, achieving a net PCE of 63.28% that translates to a 1.91x gain over even an ideal load-optimized FWR circuit (gain will be higher with respect to a real FWR implementation).

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