Self-Propelled Pre-Biased Synchronous Charge Extraction Circuit for Triboelectric Nanogenerator

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***Abstract*— Triboelectric nanogenerators (TENGs) are suitable for harvesting ambient mechanical energy to increase the battery life of the Internet of Things (IoT) devices. Energy extraction circuits (EECs) are required as an interface between TENG and the onboard battery load to rectify and improve the energy transfer efficiency. Here, for the first time, a novel "self-propelled pre-biased synchronous charge extraction (spSCE)" EEC is presented with theoretical analysis as well as experimental results. The proposed EEC offers a universal plug-and-play solution for any TENG operating under any ambient vibration, due to its self-propelled switching feature. In addition, its inbuilt pre-biasing (precharging of TENG capacitor at the operation extremes) action enhances the net transduced energy from the mechanical source beyond the per-cycle energy limit for any non-pre-biasing EEC set by the existing synchronous charge extraction (SCE) circuit. Accounting for the energy costs of spSCE actions, our experiments validated 119.7% (resp., 163.7%) energy gain over the SCE circuit at a load of 5 V (resp., 15 V).**

***Index Terms*— Energy harvesting, switched circuits, transducers, triboelectric nanogenerator (TENG).**

I. Introduction: Motivation and Objectives

AMBIENT micro energy harvesting is a promising green solution to prolonging the battery life of the Internet of Things (IoT) devices. Energy harvesters that transduce from solar, thermal, chemical, electromagnetic, and mechanical energy have been developed for the same [2]. Among those, mechanical energy harvesters have a universal appeal due to the ready availability of motion energy in a wide variety of forms, such as wind/water flow, machine/structure vibration, and human body motion [2], [3]. Amidst the choice of various mechanical-to-electrical energy transducers, the triboelectric nanogenerator (TENG) has received significant recent interest for its versatility of material choices and fabrication methods [4], [5]. Furthermore, since TENG can capture mechanical energy from different forms of reciprocating motions such as lateral (vibration), bending, and stretching through its multiple possible operating modes [4]–[6], they are suitable for harnessing energy from sources ranging from ocean waves to human body motion [4], [5], [7].

TENGs rely on the triboelectric phenomenon in which any two different materials under repeated contact develop surface charge with opposite polarity. Relative contact-separation motion between these layers then induces electromotive force (EMF) (through electrostatic induction) across the attached pair of electrodes that can be connected to an external circuit to extract electrical energy [4]. A typical TENG implementation has a parallel-plate capacitor structure with a pair of electrodes and dielectrics of different materials over each electrode (or a dielectric layer on top of one of the electrodes) operating in the contact-separation mode. For a self-powered IoT sensing application, the integrated TENG charges the onboard energy storage (battery/capacitor), which then powers the complete IoT system, for example, machine health monitoring in [8]. In such a system, an energy extraction circuit (EEC) interfacing TENG source with load is additionally required to address the following: TENG has AC output and requires rectification for charging dc loads, such as onboard battery or capacitor. Also, there is a need for source to load impedance matching to account for TENG's typically time-varying capacitive internal impedance, which leads to low energy transfer efficiency when the load is directly connected to the TENG.

A full-wave rectifier (FWR) is the simplest EEC one can use. To improve the charging efficiency of the FWR circuit, strategies, such as use of an optimized load battery voltage [9], optimized capacitor load [10], and transfer of energy to a switched intermediate capacitor and extraction from it at an optimized voltage [11], [12], have been devised. TENG's operational parameters, namely, TENG capacitance at the operation extremes (minimum and maximum separation of the TENG plates) and its open-circuit voltage, however, vary as per the fluctuations in the ambient mechanical source (e.g., bridge vibrations change as the traffic changes). Hence, to operate at the optimal point, EECs require either manual tuning or a complex closed-loop control circuit with several active components, requiring external power, reducing TENG's net energy output.

In addition to FWR and the aforementioned optimizations around it, several switched EECs with mechanical or electronic switching, synchronous to the TENG operation extremes, have also been proposed [13]. In particular, Zi *et al.* [6] proposed a cycle for maximized energy output (CMEO) using a parallel synchronous switch that can attain the highest possible

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energy output under a simple-minded closing of the switch to allow the flow of charges from one plate to the other via the load at each extremity of plate separation. Under ideal conditions, the CMEO energy output limit is realizable at any load using synchronous charge extraction (SCE) circuit, which was introduced earlier in the context of piezoelectric transducers [14]–[16] and later shown in the triboelectric context in [17]–[20]. To attain an optimized SCE operation, its serial switch's "ON" period must be synchronized and tuned to the TENG characteristics and operation, and an autotuned design that is universally applicable to any TENG and any source vibration does not exist. The existing implementations in the literature use preset/hard-coded switching periods that are not universally tuned [17]–[20].

Accordingly, in this work, we study both in theory and experiment, a novel EEC termed "self-propelled pre-biased synchronous charge extraction (spSCE)" for TENG with the following salient features.

1) Self-propelled switching with automatic tuning of the switch-ON period, making it a universal plug-and-play EEC, i.e., applicable for any TENG and any operating condition of ambient vibration.
2) Inbuilt pre-biasing (precharging of TENG capacitor at each operation extreme) to yield per-cycle energy output beyond the CMEO limit realized using SCE by increasing the net energy transduced from the mechanical source.
3) An innovative low-power control circuit for synchronous switching (with only one active component) that employs the proposed depletion-type MOSFET (as opposed to a typical enhancement-type MOSFET) switch. This scheme is measured to consume 161.2% lesser per-cycle energy than its SCE counterpart.
4) Experimental validation showing 119.7% per-cycle net energy gain measured over the SCE circuit at a battery load of 5 V, which rises to 163.7% at a battery load of 15 V.

The use of pre-biasing the TENG to potentially increase the energy output beyond the CMEO limit can alternatively be achieved via LC circuit oscillation as in the case of a parallel or series synchronous switched harvesting on inductor (P-SSHI or S-SSHI) EECs, as presented in our earlier works [21], [22] and in [23] and [24]. However, the P-SSHI or S-SSHI circuit's energy output exceeds the CMEO limit only for a specific load voltage range [22]. In contrast, the presented EEC delivers higher energy than CMEO at all possible load voltages. Another approach for pre-biasing is by way of "charge pump", i.e., by feeding back a fraction of the TENG output charge stored on a bank of intermediate (flying) capacitors, switched between series and parallel modes [25]–[27]. This method, however, crosses the CMEO output typically at very high load voltage (few tens to hundreds of volts). Hence, this method is also not universally optimized across all loads and is suited more for a capacitor load (that has rising voltage) as opposed to a fixed voltage battery load of few volts or requires an additional switched circuit stage between the charge pump and the end load [27]. Our previous work also proposed a pre-biasing scheme for TENG using the load battery itself that always delivers higher energy output than the CMEO [20] but requires a manually tuned and comparatively complex control circuit (with 13 active components). In contrast, the presented EEC requires only one active component and is self-tuned for any TENG and any ambient vibration. In addition, the pre-biasing level in the proposed spSCE can be any multiple of the load battery, whereas, in pSCE in [20], it was limited to be twice the load battery. The proposed spSCE circuit architecture has been studied previously for piezoelectric energy harvesters [28], and here, for the first time, it is introduced for TENG, where its analysis methodology, results, gains, and so on are entirely different compared to piezoelectric harvesting. This difference fundamentally stems from the different circuit models of the two transducers: piezo has a variable current source in parallel to a fixed capacitor, while tribo has a variable voltage source in series to a time-varying capacitor. To tackle the varying nature of TENG capacitor in the analysis, we introduce a smart discretization approach and, in experiments, introduce a switch control circuit different from that used in piezo setting.

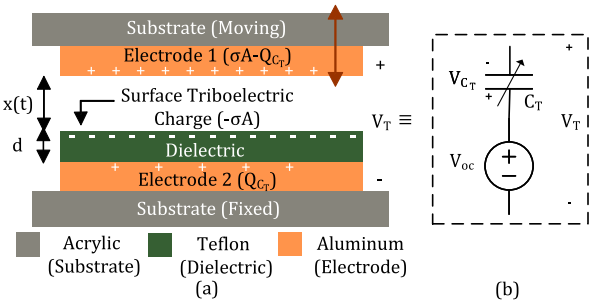

Fig. 1. (a) Cross-sectional view of a contact-separation TENG. (b) Equivalent circuit model of TENG.

In this article, we first summarize the TENG circuit model. Also, the SCE circuit's operation, its per-cycle energy output, and challenges associated with different possible approaches for its control circuit are briefly discussed to serve as a reference for comparison with the proposed spSCE circuit. Next, the proposed spSCE circuit operation is mathematically analyzed, and its per-cycle energy output is derived. The energy gain of spSCE over the SCE circuit is mathematically shown to be always positive and increasing with the value of load battery voltage. Finally, for experimental validation, both the spSCE and the SCE circuits are implemented employing a standard contact-separation mode TENG. Their measured per-cycle energy output and control circuit energy consumption are compared to quantify the energy gain. At the end, the conclusions are presented.

II. Background and Preliminaries

A. TENG Circuit Model

Fig. 1(a) shows the cross-sectional view of a contact-separation TENG, consisting of a dielectric (Teflon) tape atop an aluminum electrode to form the bottom fixed plate together with an upper moving aluminum electrode plate. External periodic mechanical excitation drives the upper plate in a vertical reciprocating motion relative to the stationary bottom

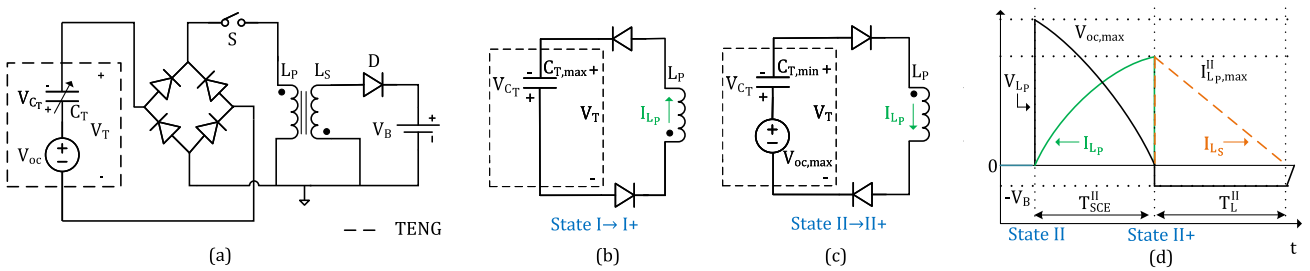

Fig. 2. SCE circuit's. (a) Diagram, simplified circuit during energy extraction with switch S turned on at (b) State I and (c) State II. (d) Primary inductor current: I_{L_P}, voltage: V_{L_P}, and secondary inductors current: I_{L_S} during switching at State II for the SCE circuit.

TABLE I
TENG PARAMETERS AT THE OPERATION EXTREMES

Operation State	Airgap (x)	Capacitance (C_T)	Open circuit voltage (V_{oc})
State I	$x_{min}=0$	$C_{T,max}=\frac{\epsilon_0 A}{d_{eff}}$	$V_{oc,min}=0$
State II	x_{max}	$C_{T,min}=\frac{\epsilon_0 A}{x_{max}+d_{eff}}$	$V_{oc,max}=\frac{\sigma x_{max}}{\epsilon_0}$

plate. The repeated contact of the two plates generates equal and opposite triboelectric surface charge, $\pm\sigma A$. This static surface charge induces open-circuit voltage, $V_{\rm oc}$, between the two electrodes that is linearly proportional to their separation

$$V_{\rm oc}(t)=\frac{\sigma x(t)}{\epsilon_0}, \tag{1}$$

where ϵ_0 is the electrical permittivity of air and $x(t)$ is the distance between the two plates (air gap) that varies periodically between zero and a certain maximum value termed $x_{\rm max}$. Furthermore, the TENG forms a variable parallel-plate capacitor with an air gap $x(t)$ along with a dielectric of thickness d between the two electrodes. If A is the contact surface area of the plates and ϵ_d is the relative permittivity of the dielectric layer, the capacitance $C_T(t)$ is given by

$$C_T(t)=\frac{\epsilon_0 A}{x(t)+\frac{d}{\epsilon_d}};\quad d_{eff}=\frac{d}{\epsilon_d}. \tag{2}$$

When connected with an external circuit, the electrodes draw equal and opposite conduction charges, $\pm Q_{C_T}(t)$ (adding to the fixed triboelectric $\pm\sigma A$ charge) to generate additional voltage $V_{C_T}(t)$ across those. Accordingly, the overall TENG voltage $V_T(t)$ is given by the superposition of the two voltages:

$$V_T(t)=V_{\rm oc}(t)-V_{C_T}(t)=\frac{\sigma x(t)}{\epsilon_0}-\frac{Q_{C_T}(t)}{C_T(t)}. \tag{3}$$

The above TENG operating equation leads to the circuit model shown in Fig. 1(b) [4]. One cycle of TENG operation commences with the two plates in contact, i.e., $x=0$ (termed State I) and rises to reach maximum separation of $x=x_{\rm max}$ (termed State II) to complete the first half-cycle, followed by return to the initial position $x=0$ in the second half-cycle. TENG electrical parameters $V_{\rm oc}$ and C_T at these two states are listed in Table I. For ease in subsequent analysis, we denote the ratio of maximum to minimum capacitance to be: $\beta=(C_{T,\rm max}/C_{T,\rm min})$.

B. SCE Circuit

It is obtained by serially connecting an FWR to a flyback converter, as shown in Fig. 2(a). Serial switch S is normally open, and the TENG's built-up energy is efficiently transferred to the primary inductor L_P at States I and II by closing the switch S for quarter the period of L_P–C_T oscillator [see Fig. 2(b) and (c)]. Upon reopening the switch, the stored magnetic energy in the inductor core is subsequently transferred to the load. Here, based on previous works [17]–[20], we summarize the SCE circuit operation, its per-cycle energy output, and different existing implementations of the control circuits for operating switch S, serving as motivation for our proposed spSCE circuit.

1) Circuit Operation: The SCE circuit operation can be understood by following the TENG voltage $V_T(t)$ waveform (blue) of Fig. 7(a). Starting with State I, with the two plates in contact (i.e., $x=0$ and both the TENG voltage V_T and charge on the TENG capacitor Q_{C_T} equal to zero), as the two plates separate with the switch S open, V_T reaches its highest value of $V_{\rm oc,max}$ at State II of maximum separation. Next, to extract energy, the switch S is closed, simplifying the SCE circuit to an L_P–$C_{T,\rm min}$ oscillator [Fig. 2(c)]. The current in the oscillator loop I_{L_P} rises sinusoidally and reaches its peak value at the end of one-fourth the L_P–$C_{T,\rm min}$ oscillator time period, denoted $T^{\rm II}_{\rm SCE}$. At this point, denoted State II+, the energy transferred to L_P is at its peak value of $(1/2)L_P(I^{\rm II}_{L_P,\rm max})^2$ and switch S is reopened, forcing a sharp cutoff of I_{L_P} in the primary loop [Fig. 2(d)]. The negative voltage developed on the coupled inductors due to this current fall is conducive for current flow in the secondary side, and the load battery is charged through the diode D. $T^{\rm II}_{\rm SCE}$ equaling one-fourth the L_P–$C_{T,\rm min}$ resonator cycle is given by

$$T^{\rm II}_{\rm SCE}=\frac{\pi}{2\omega^{\rm II}_{\rm SCE}}=\frac{\pi\sqrt{L_P C_{T,\rm min}}}{2};\ \omega^{\rm II}_{\rm SCE}=\frac{1}{\sqrt{L_P C_{T,\rm min}}}, \tag{4}$$

where $\omega^{\rm II}_{\rm SCE}$ is the resonance frequency of the oscillator. At $T^{\rm II}_{\rm SCE}$, V_{C_T} rises to $V_{\rm oc,max}$ and overall TENG voltage V_T falls to zero. With the start of the second half-cycle, the upper plate starts to descend, and V_T increases in value with negative polarity to reach its peak negative value at State I [see Fig. 7(a)]. Next, switch S is closed for one-fourth the L_P–$C_{T,\rm max}$ oscillator time period $T^{\rm I}_{\rm SCE}$ to extract energy, with the circuit simplified, as shown in Fig. 2(b). Similar to the switching action at State II [shown in Fig. 2(d)], the primary inductor current rises to its maximum value, while the voltage

across it falls to zero in $T^{\mathrm{I}}_{\mathrm{SCE}}$, which is when the switch S is reopened to trigger the load current flow in the secondary inductor. Note that

$$T^{\mathrm{I}}_{\mathrm{SCE}} = \frac{\pi}{2\omega^{\mathrm{I}}_{\mathrm{SCE}}} = \frac{\pi\sqrt{L_P C_{T,\max}}}{2} = \sqrt{\beta}\, T^{\mathrm{II}}_{\mathrm{SCE}}. \tag{5}$$

Thus, the required switch-ON duration at State I is larger by a factor of $\sqrt{\beta}$ compared to that at State II due to a change in C_T from its minimum to maximum value. The switch-ON periods ($T^{\mathrm{I}}_{\mathrm{SCE}}$ and $T^{\mathrm{II}}_{\mathrm{SCE}}$) are designed to be small compared to the TENG operating time period.

2) Per-Cycle Energy Output: For a TENG operating with time period T, the energy extracted per cycle, E_{cycle}, can be obtained from integrating the power over a cycle [6]

$$E = \int_0^T V_T I_T dt = \int_0^T V_T d Q_{C_T}. \tag{6}$$

Thus, the per-cycle energy equals the area enclosed by the V_T-Q_{C_T} cycle, as plotted in Fig. 7(b) (the areas marked ① and ② enclosed by the blue curve). The area ① corresponds to the energy extracted at the end of the first half-cycle by closing switch S at State II ($E^{\mathrm{I}}_{\mathrm{SCE}}$), which equals the triangular area under the II and II+ sloping line and is given by

$$E^{\mathrm{I}}_{\mathrm{SCE}} = \frac{1}{2} \times C_{T,\min} V_{\mathrm{oc},\max} \times V_{\mathrm{oc},\max}. \tag{7}$$

Similarly, the area ② in Fig. 7(b) corresponds to the energy extracted at the end of the second half-cycle ($E^{\mathrm{II}}_{\mathrm{SCE}}$), which equals the triangular area above the I and I+ sloping line and is given by

$$E^{\mathrm{II}}_{\mathrm{SCE}} = \frac{1}{2} \times C_{T,\min} V_{\mathrm{oc},\max} \times \frac{V_{\mathrm{oc},\max}}{\beta}. \tag{8}$$

The combined energy output over a full cycle is the sum

$$E_{\mathrm{SCE}} = E^{\mathrm{I}}_{\mathrm{SCE}} + E^{\mathrm{II}}_{\mathrm{SCE}} = \frac{1}{2}\left(1 + \frac{1}{\beta}\right) C_{T,\min} V^2_{\mathrm{oc},\max}. \tag{9}$$

It can be seen that a useful feature of the SCE circuit is that its per-cycle energy output, E_{SCE}, is independent of the load voltage due to its decoupling with the source (primary versus secondary side currents, I_{L_P} and I_{L_S}, are never simultaneously nonzero).

3) Switching Control Circuit Alternatives: For the SCE switching action, a dedicated control circuit is required to detect the two extrema of States I and II and issue the gate pulses to a MOSFET switch of desired durations $T^{\mathrm{I}}_{\mathrm{SCE}}$ and $T^{\mathrm{II}}_{\mathrm{SCE}}$, respectively. Next, we discuss the pros and cons of various existing means of implementing the switch control logic. There are three possible scenarios based on the exerted timing control.

a) Fixed timing: Fig. 3(a) shows the simplest implementation that has a fixed "hard-wired" switch-ON period, as in the case of [17]–[19]. Referring to the schematic waveforms of Fig. 3(b), the rectified TENG voltage (V'_T) is fed to a CR differentiator converting voltage peaks at States I and II to zero crossings (V'_{DT}), which triggers state change of a comparator (V'_G), whose one input is tied to ground. The rising edges of the comparator signal (V'_G) at States I and II trigger a pulse (V_G) for the gate of nMOS with its pulsewidth set by the time charging constant ($\tau = R_1 C_1$) of the RC delay unit.

From the above SCE analysis, it is known that the width of the gate pulse (switch-ON duration) required at States I and II are different and are related by (5). Thus, a limitation of this implementation is that the switch-ON duration (T_G) is the same at both States I and II, set by a common tuning handle R_1 so that $T^{\mathrm{II}}_{\mathrm{SCE}} < T_G < T^{\mathrm{I}}_{\mathrm{SCE}}$. Thus, during energy extraction at State I, the switch is prematurely opened before the primary inductor current I_{L_P} reaches its maxima of $I^{\mathrm{I}}_{L_P,\max}$ [see Fig. 3(c)] leading to suboptimal energy extraction (lower than $E^{\mathrm{II}}_{\mathrm{SCE}}$) as the energy delivered to the load is proportional to the square of the peak inductor current, while at State II, the switch is ON longer than $T^{\mathrm{II}}_{\mathrm{SCE}}$, beyond which the inductor voltage V_{L_P} fails to turn negative (in polarity) due to the FWR, and I_{L_P} can no longer maintain the sine curve [see Fig. 2(d)]. The current now circulates through the new path of L_P–S–D_3–D_2 and decays from its peak value due to parasitic resistance of L_P and the switch-ON resistance of S (present in practical scenario) in the loop until the switch is opened after T_G. This again results in suboptimal energy extraction during States II and II+ (lower than $E^{\mathrm{I}}_{\mathrm{SCE}}$). Thus, T_G is tuned to a value obeying $T^{\mathrm{II}}_{\mathrm{SCE}} < T_G < T^{\mathrm{I}}_{\mathrm{SCE}}$ optimizing the total output of $E_{\mathrm{SCE}} = E^{\mathrm{I}}_{\mathrm{SCE}} + E^{\mathrm{II}}_{\mathrm{SCE}}$. This effect of pulsewidth tuning on the total energy output of the SCE circuit has been experimentally studied previously in [19].

In practical applications, the plate separation values ($x_{\max}$ and $x_{\min}$) change depending on the variations in the external mechanical input, and hence, the required $T^{\mathrm{I}}_{\mathrm{SCE}}$ and $T^{\mathrm{II}}_{\mathrm{SCE}}$ values vary. Thus, this implementation suffers from suboptimal energy extraction due to its inability to autotune the switching times to the TENG variability. Note that when restricted to a "free-standing" mode, TENG has fixed capacitance ($\beta = 1$) [6], and it holds that $T^{\mathrm{I}}_{\mathrm{SCE}} = T^{\mathrm{II}}_{\mathrm{SCE}}$ and the "fixed timing" implementation will turn out to be optimal. However, even in this case, the switch-ON period requires an initial manual tuning as per the given TENG's capacitance.

b) Optimized timing: Our previous work proposed a novel implementation for optimal energy extraction [20]. The basic idea is to create two separate tuning handles (RC delay units), which are dedicated to switching at States I and II. When the input signal to the control circuit is tapped from the rectified output, the state information is perturbed (States I and II are indistinguishable); hence, an electrically isolated auxiliary TENG (Aux-TENG) with a fraction of the main TENG's area is in-built to operate in parallel with the main TENG [see Fig. 3(e)] and provide an unperturbed input signal to the control circuit [as in Fig. 3(f)]. The control circuit operation is similar to the fixed timing case and can be understood by following the schematic waveforms of Fig. 3(g). The product $R_1 C_1$ is tuned for pulsewidth of $T^{\mathrm{I}}_{\mathrm{SCE}}$ as signal V''_{E1}, whereas the $T^{\mathrm{II}}_{\mathrm{SCE}}$ period for signal V''_{E2} is realized by tuning the $R_2 C_2$ product. These signals are disjuncted (via OR operation) to control the nMOS switch (V_G).

It is clear that while this implementation can achieve optimal energy extraction, it still does not adjust to operation variability since the timings are still "hard-wired." The requirement of Aux-TENG is another undesired feature.

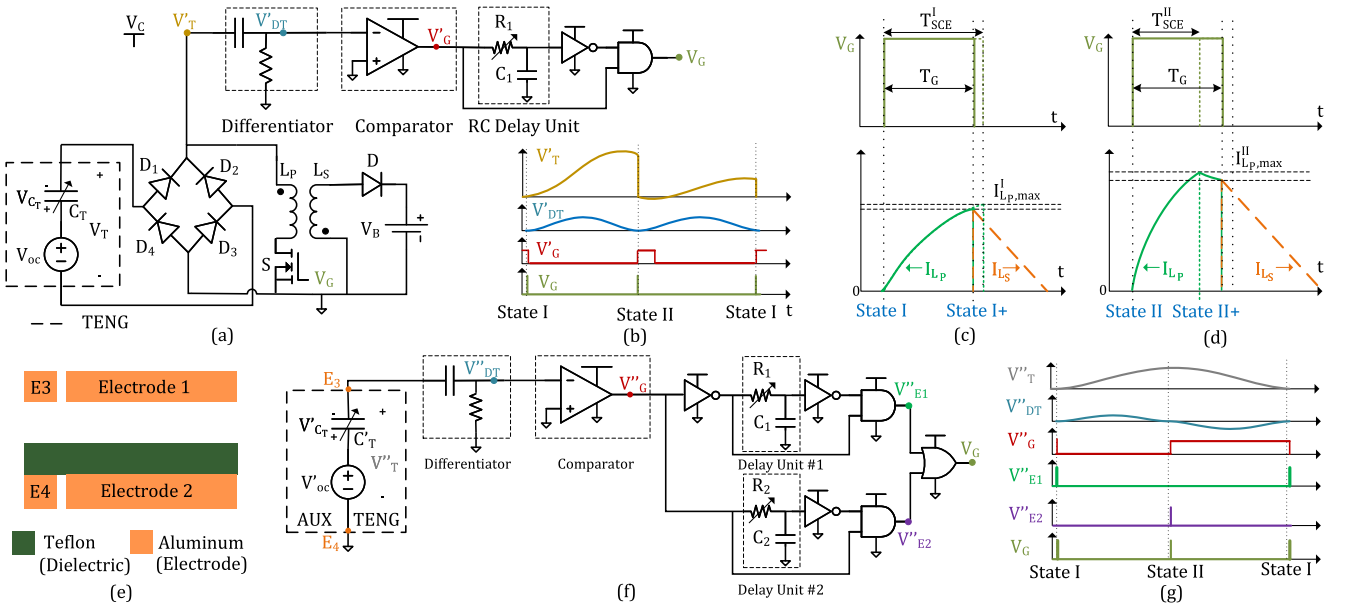

Fig. 3. Existing SCE circuit with fixed timing: (a) implementation taken from [17]–[19] and (b) its control circuit waveforms. Schematics showing the effect of suboptimal gate pulsewidth on primary inductor current, I_{LP}, during energy extraction at (c) State I and (d) State II. Existing SCE circuit with optimal timing implementation taken from [20]: (e) cross-sectional view of Aux-TENG built in parallel with the main TENG, (f) its control circuit implementation, and (g) waveforms.

c) Optimized and self-tuned timing: For an optimized and self-tuned timing, in addition to the voltage peak detector (differentiator + comparator) to start the switch-ON period, either a comparator to detect TENG's zero voltage or a current sensor in series with the primary inductor to monitor its maxima and end the switch-ON period is required. A simple-minded implementation is shown in Fig. S1 (see the Supplementary Material). However, this adds power-hungry components, such as a latch, current amplifier, and comparator. Thus, while optimality and self-tunability are realized, there are added complexity and energy cost.

Motivated by these, we propose using a circuit architecture that achieves optimal self-tuned operation with a simpler control circuit (only one active component).

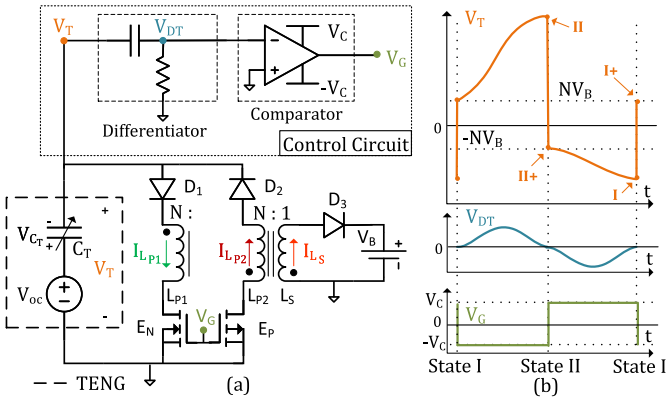

Fig. 4. (a) Proposed spSCE circuit and its control circuit. (b) Schematic waveforms of TENG voltage, $V_T(t)$, and other control circuit waveforms.

III. Proposed spSCE Circuit and Its Analysis

Fig. 4(a) shows the proposed spSCE circuit. It consists of a pair of switched inductors in parallel, L_{P1} and L_{P2}, sharing a coupled secondary inductor L_S with their turns ratio kept identical at N:1; $N = (L_{P1}/L_S)^{1/2} = (L_{P2}/L_S)^{1/2}$. L_{P1} (resp., L_{P2}) branch is serially connected to nMOS switch E_N (resp., pMOS switch E_P) and is used to extract energy at State II (resp., State I). The extracted energy is subsequently transferred to the load battery (with voltage V_B) via L_S as detailed next in Section III-A. The nMOS and pMOS gates are tied together and triggered by the control circuit output V_G. The control circuit is simply a voltage extrema detector, consisting of a CR differentiator that converts the TENG voltage V_T peaks at States I and II into zero crossings [see the V_{DT} plot in Fig. 4(b)] that toggle the output of the comparator V_G between the control circuit supply voltages: $-V_C$ and V_C, as shown in Fig. 4(b).

The self-tuned switching operation of the spSCE circuit can be understood by following the operation cycle diagram of Fig. 5(a) and the TENG voltage waveform $V_T(t)$ in Fig. 4(b) for one steady-state operation cycle. The switches E_N and E_P are normally OFF and TENG operates in open-circuit condition starting from its initial state of two plates together to reach its maximum voltage at State II [see the top left in Fig. 5(a)]. The control circuit detects the peak and changes its output to $+V_C$, enabling the nMOS E_N and forming the L_{P1}–$C_{T,\min}$ oscillator (similar to SCE), leading to rise in current through L_{P1}, while no current flows in the secondary loop due to reverse-biased diode D_3 [see the top right in Fig. 5(a)]. However, unlike the SCE circuit, the TENG voltage continues to fall beyond zero until reaching $-NV_B$, when the secondary loop diode D_3 gets forward biased (note as per the turns ratio of N:1, the voltage at the anode of diode D_3 reaches $+V_B$). This triggers current flow in the secondary inductor, while the primary inductor current drops to zero, automatically turning off the switch E_N. At this point, the open-circuit operation has resumed and continues until encountering the negative TENG voltage peak

at State I [refer Fig. 4(b) and the corresponding circuit state shown in the bottom right of Fig. 5(a)], and dual to State II above, the control circuit output toggles to $-V_C$, enabling the pMOS switch E_P to transfer built-up energy from $C_{T,\max}$ to L_{P2} [through L_{P2}–$C_{T,\max}$ oscillator, as shown in bottom left of Fig. 5(a)]. Again, dual to the State II case, E_P is automatically turned off when the TENG voltage reaches $+NV_B$ due to the forward biasing of D_3. Thus, both at States I and II, energy is extracted from TENG via self-propelled switching.

Next, we analyze the circuit by way of a smart discretization approach (as opposed to a continuous pathwise analysis) to derive the values of the TENG voltage V_T and the capacitor charge Q_{C_T} at the two discrete TENG operation extremes, States I and II, to then use them to derive the per-cycle energy output E_{spSCE}. This avoids the need to deal with the time-varying nature of the capacitance as the plates move—only charge conservation during the moving phase and the capacitance values at the two extreme positions are required for the analysis.

A. Circuit Operation and Analysis

The spSCE circuit operates with either of the switches, E_P or E_N enabled at States I ($x = 0$) and II ($x = x_{\max}$), respectively. As with the SCE circuit, we use the notations States I and I+ (resp., States II and II+) to mark the preswitching versus postswitching voltages and currents at $x = 0$ (resp., $x = x_{\max}$). Unlike the SCE circuit, spSCE shows one or more transient cycles prior to the steady-state operation as seen from the V_T waveform of Fig. 7(a) (under the "orange" curve).

We start our circuit analysis from the first cycle of operation. Starting from the resting position, the operation commences with the two TENG plates in contact, i.e., $x = 0$ and TENG voltage, $V_T = 0$. Initially, as the two plates separate, both the switches, E_N and E_P, are OFF. TENG operates in the open-circuit condition and $V_T(t) = V_{\text{oc}}(t)$ increases. The control circuit senses the rising V_T and feeds the differentiated voltage (of positive polarity) to the comparator's negative input (with positive input tied to ground) to produce the gate signal $V_G = -V_C$ [see Fig. 4(b)]. The nMOS switch E_N continues to remain OFF since the gate voltage is negative ($V_G = -V_C$). The pMOS switch E_P also remains OFF since the diode D_2 serially connected to it is reverse biased by V_T. The open-circuit state continues until the two plates are maximally apart. Here, V_T reaches the (local) peak voltage of $V_{\text{oc,max}}$ and starts to decline [see Fig. 7(a)], causing the sign of differentiated voltage to change, toggling the control circuit output from $-V_C$ to V_C, and turning on E_N, while E_P continues to remain OFF for since D_2 remains reverse-biased by V_T. The spSCE circuit simplifies to an L_{P1}–$C_{T,\min}$ oscillator, as shown in Fig. 5(c). In this configuration, the differential equation governing TENG capacitor voltage V_{C_T} can be written as

$$\frac{d^2V_{C_T}(t)}{dt^2} + \frac{V_{C_T}(t)}{L_{P1}C_{T,\min}} - \frac{V_{\text{oc,max}}}{L_{P1}C_{T,\min}} = 0; \quad t \geq 0. \tag{10}$$

With initial condition $V_{C_T}(0) = 0$ and L_{P1} taken equal to L_P (as in the SCE circuit for easy comparison), we obtain

$$V_T(t) = V_{\text{oc,max}} - V_{C_T}(t) = V_{\text{oc,max}} \cos\left(\omega_{\text{SCE}}^{\text{II}} t\right). \tag{11}$$

The oscillator resonance frequency of $\omega_{\text{SCE}}^{\text{II}}$ has been defined earlier in (4). The inductor L_{P1} voltage $V_{L_{P1}}$ equals V_T and also begins to reduce from its peak value of $V_{\text{oc,max}}$ following the cosine curve, as plotted in Fig. 6(a). Note from Fig. 4(a) that the primary inductor L_{P1} is serially connected to the TENG via a single diode, and hence, $V_{L_{P1}}$ can assume negative voltage value and continue following V_T past its zero crossing, unlike the SCE architecture [Fig. 2(a)], where the FWR restricts primary inductor to positive voltage drops only. The primary and secondary inductors have a turns ratio of N, and hence, for $t > T_{\text{SCE}}^{\text{II}}$, diode D_3, connected serially with the secondary inductor L_S, is reverse biased until the secondary voltage, $V_{L_S}(t) = (V_{L_{P1}}(t)/N) > -V_B$. As shown in Fig. 6(a), the load charging commences when the inductor voltage $V_{L_{P1}} = V_T$ reaches $-NV_B$. The secondary voltage V_{L_S} remains at $-V_B$, and thus, the primary-side voltage $V_{L_{P1}}$ remains at $-NV_B$ causing its rate of change to become zero, thereby forcing the primary side current $I_{L_{P1}}$ to be also zero. Due to the turns ratio, the secondary current spikes up to N times that of the primary current just prior to the moment it was forced zero, charging the battery while decaying linearly (since from the circuit of Fig. 4(a), $L_S(d/dt)(I_{L_S}) + V_B = 0 \Rightarrow (d/dt)(I_{L_S}) = -(V_B/L_S)$). When the primary current drops to zero, E_N is automatically switched OFF (in a self-propelled manner) and State II+ is reached, with the following values for TENG voltage and capacitor charge:

$$V_T^{\text{II+}} = -NV_B \Rightarrow Q_{C_T}^{\text{II+}} = C_{T,\min}\left(V_{\text{oc,max}} + NV_B\right). \tag{12}$$

Thus, aside from the self-propelled switch OFF, the added advantage of the proposed switching control circuit is that it automatically pre-biases the TENG to N times the load voltage ($V_T^{\text{II+}} = -NV_B$), unlike the case of SCE circuit where V_T is set to zero at State II+.

Remark 1: Note that if the turns ratio N and load voltage V_B do not satisfy $V_{\text{oc,max}} > NV_B$, after E_N is enabled at State II, the reverse biasedness of D_3 shall continue even until the TENG voltage becomes the minimum possible ($V_T(t) = V_{L_{P1}}(t) = -V_{\text{oc,max}}$), i.e., until the end of half the L_{P1}–$C_{T,\min}$ resonator cycle, and there shall be no load battery charging [see Fig. 6(b)]. Beyond this point in time, the current through the primary inductor that follows a sine curve tends to reverse its direction, but the diode D_1 blocks that, switching OFF E_N and reaching State II+. In that case, the spSCE circuit shall undergo a multiple number of transient cycles depending on the value of NV_B relative to $V_{\text{oc,max}}$ where the TENG voltage buildup occurs without charging the battery and eventually entering the steady-state operation, where the battery charging takes place. This general scenario is analyzed in the Supplementary Material, where the number of transient cycles m is derived [see (S3) in Supplementary Note S.II], which can be expressed using the ceiling function as follows:

$$m = \left\lceil \frac{1}{2}\left(1 + \frac{NV_B}{V_{\text{oc,max}}}\right)\right\rceil. \tag{13}$$

However, this situation ($m > 1$) is practically not very likely. Typical TENG's maximum open-circuit voltage to battery voltage ratio ($V_{\text{oc,max}}/V_B$) is of the order of 50 or higher, while the turns ratio N is typically no larger than 10. Hence,

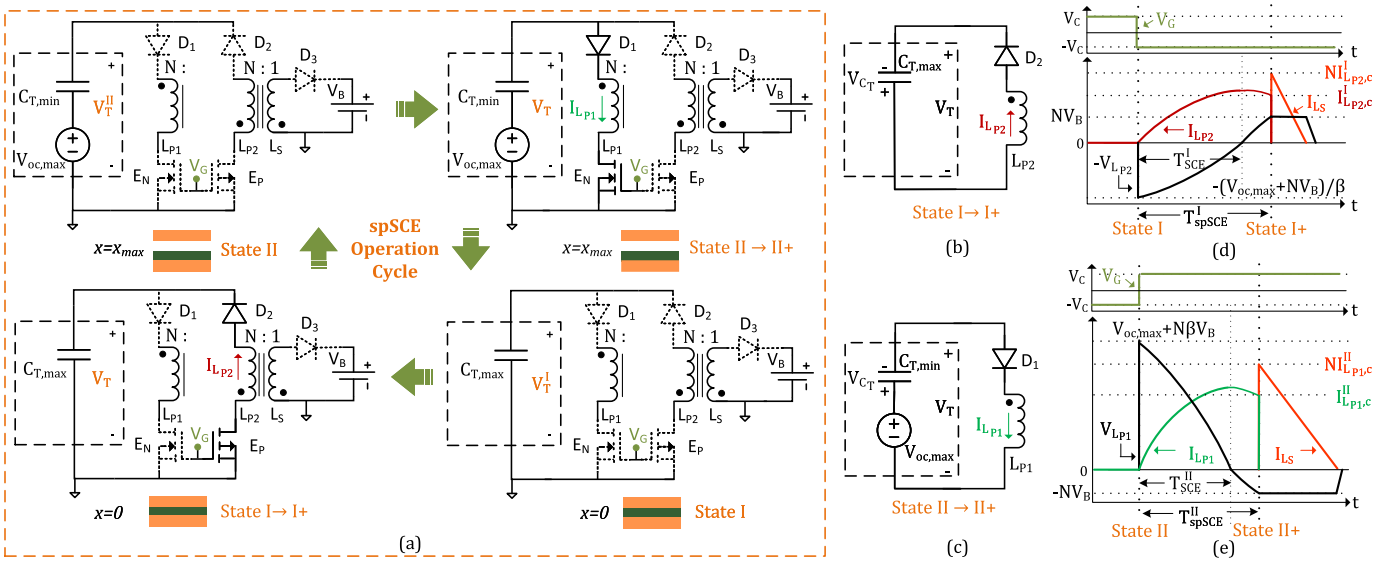

Fig. 5. spSCE circuit: (a) Operation cycle and (b) simplified circuit during energy extraction at (b) State I with E_P enabled and (c) State II with E_N enabled. Primary inductor current: $I_{L_{P2}}/I_{L_{P1}}$, voltage: $V_{L_{P2}}/V_{L_{P1}}$, and secondary inductor current: I_{L_S} during switching at (d) State I and (e) State II.

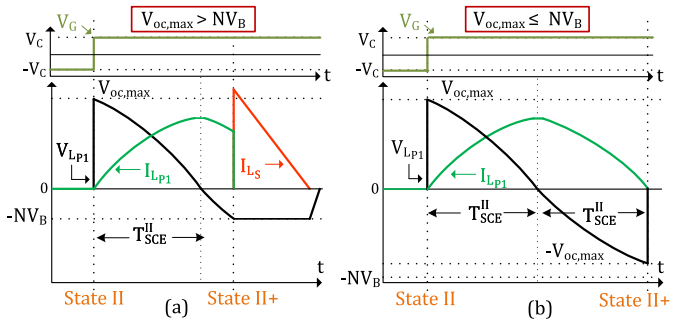

Fig. 6. Primary inductor current: $I_{L_{P1}}$, voltage: $V_{L_{P1}}$, and secondary inductor current: I_{L_S} for spSCE circuit during switching at State II of the first operation cycle in case of (a) $V_{\text{oc,max}} > NV_B$ and (b) $V_{\text{oc,max}} \leq NV_B$.

the common practical implementations will likely satisfy the condition $V_{\text{oc,max}} > NV_B$, and here, we continue to analyze this case with one transient cycle, as shown in Fig. 7(a) (under "orange" curve). Interested readers may refer to the TENG waveform of Fig. S3 (see the Supplementary Material) for $V_{\text{oc,max}} \leq NV_B$ showcasing multiple transient cycles.

As the upper plate continues to descend in the second half-cycle beyond State II+, the TENG again operates in the open-circuit condition since E_N is OFF by reverse-biased diode D_1 and pMOS E_P is OFF by gate voltage V_G remaining pegged at $+V_C$. At the end of the second half-cycle (State I), the two plates are in contact, yielding $V_{\text{oc}} = V_{\text{oc,min}} = 0$ and $C_T = C_{T,\text{max}}$ [see the bottom right in Fig. 5(a)]. In addition, since the charge is preserved, $Q^{\text{I}}_{C_T} = Q^{\text{II+}}_{C_T}$:

$$V_T^{\text{I}} \overset{(3)}{=} 0 - \frac{Q^{\text{I}}_{C_T}}{C_{T,\text{max}}} = -\frac{Q^{\text{II+}}_{C_T}}{C_{T,\text{max}}} \overset{(12)}{=} -\frac{\left(V_{\text{oc,max}} + NV_B\right)}{\beta}. \quad (14)$$

The control circuit senses this V_T minima and toggles V_G from V_C back to $-V_C$, enabling E_P this time (see the bottom left in Fig. 5), and the TENG circuit is reduced to an L_{P2}–$C_{T,\text{max}}$ oscillator [Fig. 5(b)]. Dual to State II operation described above, as schematized in Fig. 5(d), V_T follows an inverted cosine curve and rises from its minima, flips its polarity at quarter the oscillator cycle, and continues to rise until the load charging commences at $V_T = -V_{L_{P2}} = NV_B$ when E_P is automatically switched OFF and State I+ is achieved with

$$NV_B = V_T^{\text{I+}} = -\frac{Q^{\text{I+}}_{C_T}}{C_{T,\text{max}}} \Rightarrow Q^{\text{I+}}_{C_T} = -N\beta C_{T,\text{min}} V_B. \quad (15)$$

We denote the E_P's switch-ON time as $T^{\text{I}}_{\text{spSCE}}$ that satisfies $T^{I}_{\text{SCE}} < T^{\text{I}}_{\text{spSCE}} < 2T^{I}_{\text{SCE}}$ and is dependent on the voltage NV_B. Since $T^{\text{I}}_{\text{spSCE}} > T^{I}_{\text{SCE}}$, the energy extraction at State I is not optimal, and charging begins past the $I_{L_{P2}}$ peak [see the red curve of Fig. 5(d)]. However, the pre-biasing action more than compensates for it, leading to a net increase in the energy extracted at the next extraction epoch, namely, at State II, as analytically proved in Section III-B.

Remark 2: During State I to I+, with E_P enabled, the inductor voltage $V_{L_{P2}}$ following cosine curve can rise to a maximum flipped value of $-V_T^{\text{I}} = ((V_{\text{oc,max}} + NV_B)/\beta)$ by the end of half the resonator cycle ($2 \times T^{\text{I}}_{\text{SCE}}$). In case of $V_B \geq ((V_{\text{oc,max}})/(N(\beta - 1)))$, no load charging shall take place. For the sake of completeness, this case is also analyzed in the Supplementary Note S.III.

Continuing the operation analysis [see Fig. 7(a)], on reaching State II ($x = x_{\text{max}}$) with $Q^{\text{II}}_{C_T} = Q^{\text{I+}}_{C_T}$, we have

$$V_T^{\text{II}} = V_{\text{oc,max}} - \frac{Q^{\text{II}}_{C_T}}{C_{T,\text{min}}} = V_{\text{oc,max}} + N\beta V_B. \quad (16)$$

Note the increment of $N\beta V_B$ in V_T^{II} due to pre-biasing action at State I compared to its SCE counterpart. As before, a change in the state of V_G on detection of peak voltage V_T^{II} enables conduction through E_N to form the L_{P1}–$C_{T,\text{min}}$ oscillator. Referring to Fig. 5(e), past the quarter resonance cycle ($T^{\text{II}}_{\text{SCE}}$), when $V_{L_{P1}} = V_T$ reaches $-NV_B$ value (after $T^{\text{II}}_{\text{spSCE}}$), secondary loop diode D_3 starts to conduct, freezing the secondary- and primary-side voltages (to V_B and $-NV_B$, respectively) and causing a (self-propelled) zeroing of the primary inductor current $I_{L_{P1}}$ from its value of $I^{\text{II}}_{L_{P1},c}$. This further leads to rise of secondary inductor current I_{L_S} to

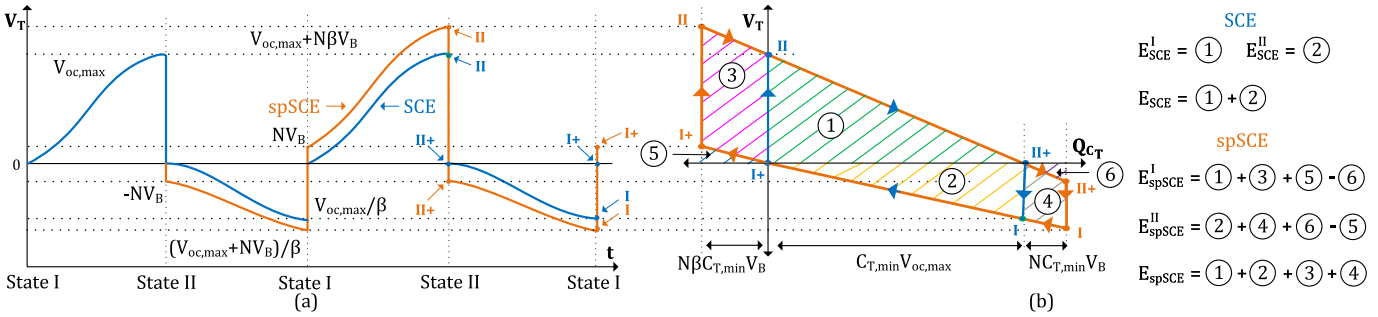

Fig. 7. (a) TENG voltage waveform plot (blue under SCE versus orange under spSCE), and (b) TENG "charge versus voltage" plot for SCE (areas 1 and 2) and spSCE (areas 1–4) circuits.

$N \times I^{\text{II}}_{L_{P1},c}$. This marks State II+, and with E_N switched OFF, $V_T^{\text{II+}}$ is pre-biased to $-NV_B$ and $Q_{C_T}^{\text{II+}}$ is the same as derived in (12), completing the analysis of one steady-state operation cycle.

B. Per-Cycle Energy Output

As with the case of the SCE circuit, per-cycle energy output will be obtained using the V_T–Q_{C_T} plot. The steady-state values of V_T and Q_{C_T} derived for the spSCE circuit at States I, I+, II, and II+ are used to obtain the plot of Fig. 7(b). The energy extracted at the end of the first half-cycle, E^{I}_{spSCE}, is equal to the net area enclosed by the extraction step, namely, State II and II+ line, and the Q_{C_T}-axis, i.e., the net area ① + ③ + ⑤ − ⑥ in Fig. 7(b) and is given by

$$E^{\text{I}}_{\text{spSCE}} = \frac{1}{2} \times C_{T,\min}\left(V_{\text{oc,max}} + N\beta V_B\right) \times \left(V_{\text{oc,max}} + N\beta V_B\right) - \frac{1}{2} \times NC_{T,\min} V_B \times NV_B. \quad (17)$$

Here, the area of the triangular region ⑥ is subtracted as V_T is negative for the corresponding part of II and II+ line turning the $V_T dQ_{C_T}$ product negative [see (6)]. Similarly, energy extracted at the end of the second half-cycle, $E^{\text{II}}_{\text{spSCE}}$, is the net area enclosed by the State I and I+ line, i.e., the net areas ② + ④ + ⑥ − ⑤ in Fig. 7(b) and can be calculated as

$$E^{\text{II}}_{\text{spSCE}} = \frac{1}{2} \times C_{T,\min}\left(V_{\text{oc,max}} + NV_B\right) \times \frac{\left(V_{\text{oc,max}} + NV_B\right)}{\beta} - \frac{1}{2} \times N\beta C_{T,\min} V_B \times NV_B. \quad (18)$$

Adding the above two energy components of the two half-cycles, it follows that the per-cycle energy output E_{spSCE} is the total area enclosed by the spSCE curve [areas ① + ② + ③ + ④ in Fig. 7(b)]:

$$\begin{aligned} E_{\text{spSCE}} &= E^{\text{I}}_{\text{spSCE}} + E^{\text{II}}_{\text{spSCE}} \\ &= \frac{1}{2} C_{T,\min}\left[\left(V_{\text{oc,max}} + N\beta V_B\right)^2 + \frac{\left(V_{\text{oc,max}} + NV_B\right)^2}{\beta} - (1+\beta)(NV_B)^2\right]. \end{aligned} \quad (19)$$

Comparing with the SCE circuit output form [see (9)], the above derived spSCE circuit's output can be rewritten as

$$E_{\text{spSCE}} = E_{\text{SCE}} + \frac{1}{2} C_{T,\min} V_B \left[2\left(\beta + \frac{1}{\beta}\right) V_{\text{oc,max}} + N^2(\beta - 1)\left(\beta - \frac{1}{\beta}\right) V_B\right]. \quad (20)$$

Since $\beta \geq 1$, it is clear from (20) that $E_{\text{spSCE}} > E_{\text{SCE}}$ and the additional harvested energy can be visualized from Fig. 7(b) as the additional area enclosed by the spSCE operation (③+④) beyond the SCE trapezoidal area (① + ②). Also, since E_{SCE} is independent of the load voltage [see (9)], it follows from (20) that E_{spSCE} is an increasing function of the load voltage V_B. In other words, the energy output and gain of spSCE over SCE continue to rise with increasing V_B. Fundamentally, the gain over SCE is due to spSCE's pre-biasing at the start of each half-cycle (by $\pm NV_B$) that increases the TENG's electrical damping, enhancing the net transduced mechanical energy [20].

Remark 3: As derived above, the spSCE circuit's output increases at higher battery load voltage, and as also stated in Remark 1 and derived in the Supplementary Note S.II, this may require a buildup of the TENG voltage to NV_B level through transient cycles. This can indeed be achieved in the ideal setting of no parasitic losses. However, in practice, there exists a limit to how far the TENG voltage can be raised before it saturates due to the parasitic resistive losses, which we briefly quantify here. In the case of $NV_B \geq V_{\text{oc,max}}$ with multiple transient cycles, referring to Fig. 6(b), during State II to II+ operation, L–$C_{T,\min}$ oscillator circuit ensures a perfect flip of voltage ($V_T^{\text{II+}} = -V_T^{\text{II}}$) in half the oscillation cycle. However, the series resistance of the primary inductor as well as the switch-ON resistance present in the oscillator loop [see Fig. S5(b) in the Supplementary Material] reduce the voltage swing to render $V_T^{\text{II+}} = -\alpha^{\text{II}} V_T^{\text{II}}$, where $0 < \alpha^{\text{II}} < 1$ is the "normalized" resonator quality factor with its value determined by the resistance, inductance, and the resonance frequency of the oscillator loop [see (S13) in the Supplementary Material]. Similarly, $0 < \alpha^{\text{I}} < 1$ determines the voltage swing of the oscillator loop during State I to I+: $V_T^{\text{I+}} = -\alpha^{\text{I}} V_T^{\text{I}}$. These imperfect swings lead to saturation of V_T over the transient buildup cycles, upper bounding its steady-state value

TABLE II

spSCE Circuit Implementations and Their Control Circuit Supply Requirements

Implementations	PMOS	NMOS	High	Low
Dual supply	Enhancement	Enhancement	V_C	$-V_C$
Single Positive supply	Depletion	Enhancement	V_C	0
Single Negative supply	Enhancement	Depletion	0	$-V_C$

(see Fig. S5(c) for visualization and the derivation of (S17) in the Supplementary Note S.IV), thereby limiting the allowable load voltage to a finite value

$$V_B = \left[\frac{\alpha^{\mathrm{II}}\left(1+\alpha^{\mathrm{I}}\right)}{\left(1-\alpha^{\mathrm{I}}\alpha^{\mathrm{II}}\right)}\right]\frac{V_{\mathrm{oc,max}}}{N}. \tag{21}$$

C. Design With Single Polarity Power Supply

For ease of explanation, the spSCE circuit operation was discussed above with commonly used enhancement-type pMOS (E_P) and nMOS (E_N) as switches. An enhancement-type nMOS requires gate voltage higher than its positive threshold voltage, while an enhancement-type pMOS requires gate voltage lower than its negative threshold voltage to switch-ON and both are normally OFF, i.e., they remain switched OFF at zero gate voltage. Hence, the control circuit (comparator) of spSCE circuit requires a dual power supply with $-V_C$ (low) and $+V_C$ (high) voltages [see Fig. 4(a) and (b)] to switch-ON pMOS and nMOS at States I and II, respectively. This dual power supply requirement can be relaxed by the innovation of introducing depletion-type pMOS or nMOS in the spSCE circuit architecture. A depletion-type pMOS (resp., nMOS) remains normally ON and is switched OFF by pulling gate voltage (V_G) to V_C (resp., $-V_C$). With enhancement-type pMOS [E_P in Fig. 4(a)] replaced by a depletion-type pMOS and E_N retained as enhancement-type nMOS, spSCE circuit operation can be achieved with gate voltage V_G toggling between 0 and V_C. Then, the control circuit shall require only a single voltage polarity power supply. Similarly, a combination of enhancement-type pMOS and depletion-type nMOS allows operation with $-V_C$ and 0 states. All these three possible spSCE circuit implementations based on the required control circuit supply voltages are listed in Table II.

IV. Experimental Implementation

A. TENG Setup and Characterization

For experimental verification of the proposed circuits, the TENG was implemented as shown in Fig. 1 with aluminum tape as the two electrode layers and Teflon tape of thickness 127 μm as the dielectric layer. The contact area between the upper moving plate (electrode 1) and the lower fixed plate (dielectric + electrode 2) is 112.5 cm^2. For TENG operation, a programmed stepper motor moves the upper plate in reciprocating fashion at $10-$ Hz frequency with an amplitude of $x_{\max} = 1.64$ mm. The overall setup picture is shown in Fig. S6 (see the Supplementary Material).

The key parameters for TENG characterization: minimum and maximum TENG capacitances ($C_{T,\min}$ and $C_{T,\max}$), and the maximum open-circuit voltage ($V_{\mathrm{oc,max}}$), for our setup, were experimentally measured and are summarized in Table III. For the TENG capacitance measurement, the phase response method described in [25] was used. The measured $C_T(t)$ is plotted in Fig. S8 (see the Supplementary Material) from which the $C_{T,\min}$ and $C_{T,\max}$ values were extracted. The maximum open-circuit voltage ($V_{\mathrm{oc,max}}$) was measured with the aid of an FWR circuit as previously carried out in [20] and [22] and described in the Supplementary Note S.VII.

TABLE III

Measured TENG Parameters

Maximum open circuit voltage: $V_{oc,max}$	282.88 V
Minimum TENG capacitance: $C_{T,min}$	76.35 pF
Maximum TENG capacitance: $C_{T,max}$	241.12 pF
TENG capacitance ratio: β	3.16

B. Circuit Implementations

The proposed spSCE circuit along with the SCE circuit was implemented over PCB using off-the-shelf components for energy output measurement and comparison.

1) SCE Circuit: The SCE circuit with fixed as well as optimal switch-ON period were implemented, as shown in Fig. 3(a) and (f), respectively. For the fixed timing case, the capacitor C_1 was fixed at 1 pF, while the resistance R_1 was tuned to 750 kΩ, corresponding to a switching pulsewidth of $\sim$5.8 μs, to offer maximized energy output of the fixed timing architecture. For the optimal timing implementation, an Aux-TENG with a contact area of 22.5 cm^2 (1/5th area of main TENG) was fabricated to provide an input signal to the control circuit (see Figs. 3(e) and S6). The switching pulsewidth for State I ($T^{\mathrm{I}}_{\mathrm{SCE}}$) was tuned to $\sim$6.8 μs using $R_1 = 820$ kΩ ($C_1 = 1$ pF), while that for State II ($T^{\mathrm{II}}_{\mathrm{SCE}}$) was tuned to $\sim$1.8 μs using $R_2 = 300$ kΩ ($C_2 = 1$ pF) [see Fig. 3(f)]. The control circuit's supply voltage, V_C, and the measured per-cycle energy consumption, E_{control}, for both the implementations are provided in Table IV. The PCB implementation of the fixed-timing and the optimal-timing SCE circuits is shown in Fig. S7 (see the Supplementary Material).

2) spSCE Circuit: The spSCE circuit of Fig. 4(a) is implemented with enhancement-type pMOS and nMOS. A depletion-type nMOS is used for single negative supply implementation. The PCB implementation of the spSCE circuits with coupled inductors' turns ratio $N = 1$ with Murata 1026C (1:1:1) and $N = 2$ with Pulse PH9400 (2:2:1) is shown in Fig. S7 (see the Supplementary Material). The spSCE output and control circuit consumption are listed in Table IV.

V. Results and Discussion

For our experimental spSCE and TENG with its parameters listed in Table III, the measured TENG voltage V_T, load current I_{L_S}, and the control voltage V_G waveforms in steady state at battery voltage $V_B = 10$ V under the turns ratio $N = 2$ and $N = 1$ are shown in Fig. 8(a) and (b), respectively. As predicted from our derivation, due to the pre-biasing, the maximum TENG voltage in both the half-cycles, i.e., at States I and II, is higher (in magnitude) for $N = 2$ than

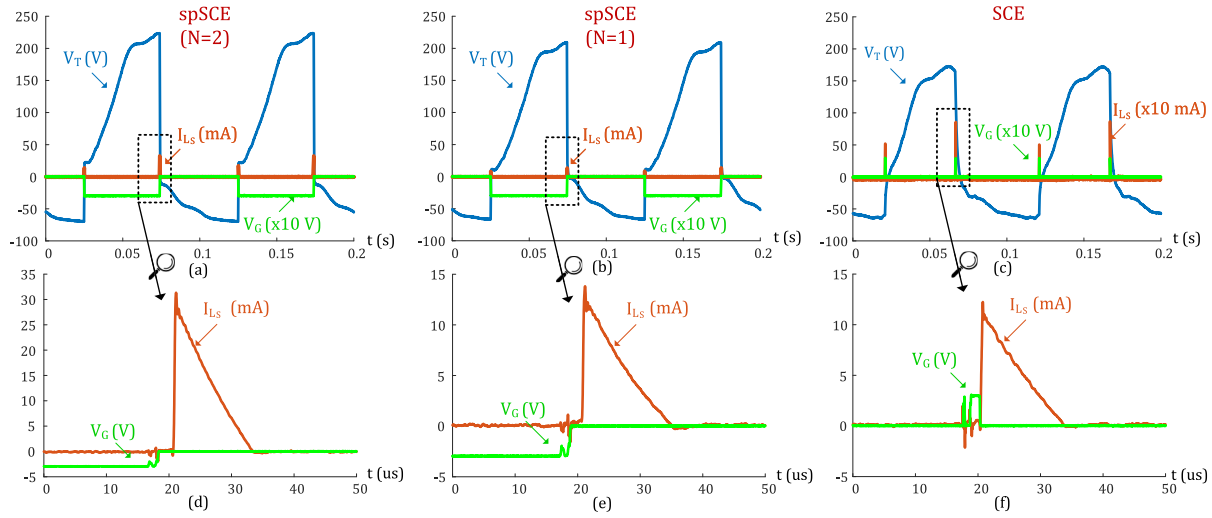

Fig. 8. Measured TENG voltage: V_T, load current: I_{L_S}, and control voltage: V_G waveforms at 10-V battery load for (a) spSCE with turns ratio $N = 1$, (b) spSCE with turns ratio $N = 2$, and (c) SCE (optimal timing) circuits. Zoomed-in view of I_{L_S} and V_G at State II for (d) spSCE ($N = 1$), (e) spSCE ($N = 2$), and (f) SCE (optimal timing) circuits.

TABLE IV
NET ENERGY OUTPUT FOR CIRCUIT IMPLEMENTATIONS AT $V_B = 10$ V

SCE Circuit Implementations	E_{SCE} (uJ)	Supply (V) Low	High	$E_{control}$ (uJ)	$E_{SCE,net}$ (uJ)
Fixed Timing	0.883	0	3	0.219	0.664
Optimal Timing	1.061	0	3	0.256	0.805
spSCE Circuit Implementations	**E_{spSCE} (uJ)**	**Supply (V) Low**	**High**	**$E_{control}$ (uJ)**	**$E_{spSCE,net}$ (uJ)**
Dual Supply (N=1)	1.471	-3	3	0.262	1.209
Single Supply (N=1)	1.379	-3	0	0.098	1.281
Single Supply (N=2)	1.839	-3	0	0.098	1.741

N: Turns ratio of the coupled inductors

for $N = 1$, which in turn is higher than its SCE counterpart [Fig. 8(c)]. Fig. 8(d) and (e) shows the zoomed-in view of load current, I_{L_S}, and control voltage, V_G at State II for the $N = 2$ and $N = 1$ implementations, respectively. The change of V_G from -3 to 0 V enables the depletion-type nMOS, and the rise of secondary loop current I_{L_S} after the switch-ON period is observed, which subsequently linearly decays, charging the load battery. Similarly, for the SCE circuit, Fig. 8(f) shows the rise of the load current I_{L_S} triggered by the fall of the gate signal V_G at State II. Similar plots are observed for State I.

A. Performance Comparison

1) Energy Output: The measured per-cycle energy outputs using the fixed-timing and the optimal-timing SCE circuits at $V_B = 10$ V battery load are listed in Table IV. It is calculated as the product of load voltage and integration of the measured current (i.e., the net accumulated charge) flowing through the load battery over one cycle. Per-cycle energy consumed by their respective control circuits, E_{control}, is nearly constant across the load voltage range and is deducted from E_{SCE} to obtain their net energy output, $E_{\text{SCE,net}}$. In our experiments, optimal-timing SCE implementation delivers 20.2% (178 nJ) higher energy compared to the fixed-timing implementation (see Table IV). Thus, from here on, we use the optimal-timing SCE implementation with higher energy output for comparison with the spSCE circuit implementations.

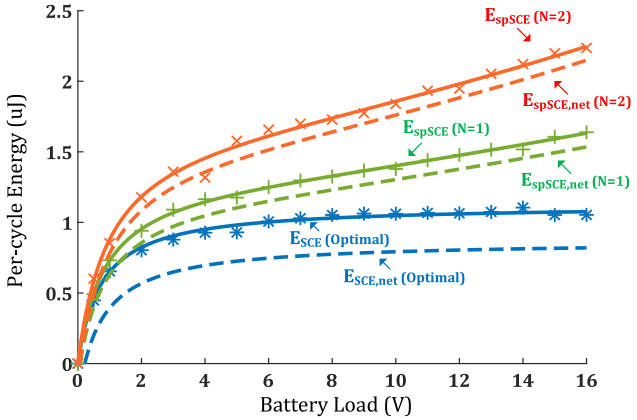

Fig. 9. Comparison of measured per-cycle gross spSCE circuit energy output: E_{spSCE} with that of SCE: E_{SCE} against the load voltage: V_B. $E_{\text{spSCE,net}}$ and $E_{\text{SCE,net}}$ are the net energy output post deduction of respective control circuit consumption.

For the case of $N = 1$, among the two spSCE circuit implementations (dual versus single supply) listed in Table IV, due to lower E_{control}, the net per-cycle energy output, $E_{\text{spSCE,net}}$, of the single supply implementation has a gain of 6% (72 nJ). This validates the proposed innovation of employing a depletion-type MOSFET to enable single supply implementation, demonstrating that it not only eases the supply voltage polarity requirement but also significantly reduces the energy consumption. Hence, the preferred single supply implementation was further used in the spSCE circuit with $N = 2$.

Next, we compare the measured per-cycle energy output of the single supply spSCE circuit with $N = 1$ and 2 and the optimal-timing SCE circuit, over a load battery range of 0–16 V in Fig. 9. The net energy output of these implementations obtained by deducting their respective control circuit energy consumption is also coplotted in Fig. 9 for visual confirmation of the minimal energy loss in the control circuit. The observed increasing trend of E_{spSCE} with increasing V_B validates the theoretical development of Section III.

TABLE V
EXPERIMENTAL NET POWER DENSITY OF SCE AND pSCE CIRCUITS AT 10-V BATTERY LOAD

Circuit	PCB Area (cm^2)	Power Density (uW/cm^2)	PCB+TENG Area (cm^2)	Power Density (uW/cm^2)
SCE (Fixed)	5.955	1.115	118.46	0.056
SCE (Optimal)	8.300	0.970	143.3[a]	0.056
spSCE (N=1)	5.023	2.550	117.52	0.109
spSCE (N=2)	5.530	3.149	118.03	0.148

[a] includes auxiliary TENG area

Also, a higher pre-biasing due to $N = 2$ consistently fetches a higher gain over $N = 1$, and both these spSCE cases are consistently superior over the SCE. The energy gains of 34.2% (0.402 μJ) at $V_B = 5$ V and 36.8% (0.592 μJ) at $V_B = 15$ V over the spSCE circuit with $N = 1$ were observed. The gains were even higher with respect to SCE: 69.7% (0.648 μJ) at $V_B = 5$ V and 108.9% (1.146 μJ) at $V_B = 15$ V. Due to the spSCE's innovative control circuit, which uses a single active component (namely, the comparator), its E_{control} is less than half of that for the SCE circuit (see Table IV), rendering even higher net energy gains: 119.7% (0.806 μJ) at $V_B = 5$ V and 163.7% (1.304 μJ) at $V_B = 15$ V.

2) Power Density: The net power density figures of the two SCE (fixed versus optimal timing) and the two spSCE ($N = 1$ versus $N = 2$) implementations computed from our validation experiments at 10-Hz operational frequency and 10-V load are listed in Table V. The proposed spSCE circuit achieves more than a twofold improvement in power density over the SCE circuit. Also, it should be noted that the reported values are for our initial PCB implementation; the power density can be significantly improved by reducing the circuit area through further optimization of design and selection of components.

3) Efficiency: A measure of energy conversion efficiency is the performance against the "CMEO" [6], which sets the upper limit on the energy that can be harvested without any active feedback (pre-biasing) of the already harvested energy into the TENG transducer. This CMEO limit is given by $E_{\text{CMEO}} = (1/2)(1+(1/\beta))C_{T,\min}V_{\text{oc,max}}^2$ and is attained by the optimized timing SCE architecture under ideal setting [see (9)]. Using the CMEO as a reference, the conversion efficiency of an EEC is defined as $\eta = (E_{\text{cycle}}/E_{\text{CMEO}}) \times 100\%$ as has been used in previous works, such as [9] and [18]. While the ideal setting (no parasitic losses) SCE efficiency is 100%, its measured value is only 26.38%. In comparison, the spSCE with $N = 2$ has a measured efficiency of 54.66% for a 15-V load, while it is even higher at 161.26% under the ideal setting. The spSCE achieves such high improvements due to its in-built active pre-biasing feature, which is designed to increase with the increase in load voltage or by simply using a higher turns ratio N (as derived in Section III-B). The proposed spSCE can further be compared with other EECs in the literature by referring to the efficiency survey table provided in our previous work [20].

B. Impact of Nonidealities

The nonidealities that affect the overall performance include diode voltage drops, leakage currents, diode/switch/inductor resistances, and so on. While the ideal SCE output is supposed to be constant across load voltages, it is not so in practice due to nonidealities as seen by the concave shape of the E_{SCE} curve at lower load voltages in Fig. 9, which is primarily caused by the parasitic nonzero diode drop, V_D [across the diode connected in series with the secondary inductor marked as diode "D" in Fig. 2(a)]. The derivation of E_{SCE} considering V_D [see (S22) in the Supplementary Note S.VIII] introduces a multiplication factor $(V_B/(V_B + V_D))$ to the ideal SCE circuit's energy output. With a typical V_D of $\sim$0.7 V, we observe the concave curve for E_{SCE} at low V_B and flat response for $V_B \gg V_D$ in Fig. 9. Similar behavior is observed for the spSCE circuit, too, due to the diode voltage drop across D_3 during the energy extraction.

Both SCE and spSCE circuits operate generally in open-circuit conditions other than the brief periods at States I and II. The leakage currents during the off periods through the nonideal switches lead to lower TENG voltage amplitudes at States I and II, reducing the extracted energy. In case of the SCE circuit, for example, the TENG voltage at State II is expected to be equal to measured $V_{\text{oc,max}} = 282.88$ V, but the leakage reduces the measured peak to 179.61 V [see Fig. 8(c)]. Besides the mentioned diode drops and leakage currents nonidealities, ON-resistance of the MOSFET switches, and the limited quality factors of the inductors due to their parasitic resistances reduce the output compared to the theoretically expected value. Specifically, as derived in (21), the limited inductor quality factor places an upper bound on the maximum attainable TENG voltage/pre-biasing beyond which no added energy gain can be expected.

VI. CONCLUSION

This work proposed a novel EEC, a self-propelled pre-biased synchronous charge extraction for TENG. The proposed circuit realizes efficient energy extraction via an external inductor, switched synchronously with the TENG operational extremes (TENG plates fully separated versus fully contracted). The desirable self-propelled feature refers to the automated tuning of the switching start and end epochs as per any given TENG's operating conditions, as against the existing SCE circuit implementations that require a manually tuned control circuit and hence are not adaptive to the vibrations they respond to. Furthermore, it is analytically derived that the in-built pre-biasing feature of the spSCE circuit leads to an increase in the net per-cycle transduced mechanical energy, boosting the energy output beyond the SCE's limit of CMEO. The turns ratio N of the used coupled inductors serves to boost the effective battery voltage by a factor N raising the pre-biasing level by that same factor. It is formally derived that the spSCE circuit outperforms the SCE circuit at any load voltage, and its gain continues to rise with the rising effective load voltage.

The theoretically expected gain in energy output was validated by the experimental implementation of the spSCE as well as the SCE circuit for comparison. The self-propelled switching control circuit of spSCE is found to consume 161.2% smaller per-cycle energy compared to the one currently used for SCE. The low energy consumption of spSCE's control circuit is attributed to its simple single active

component design and the innovative use of depletion-type MOSFET (against typically used enhancement-type MOSFET) for switching in the spSCE circuit. The proposed circuit's higher energy output, yet lower control circuit energy consumption when compared to the SCE circuit, led to a measured net gain of 119.7% at $V_B = 5$ V that rose to 163.7% at $V_B = 15$ V. We hope that the presented spSCE EEC with simpler implementation and boosted energy output shall pave the way toward its wide-scale adoption in motion energy-harvesting applications.

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