A non-isolated Common-Ground High Step-Up Soft Switching DC-DC Converter with Single Active Switch

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***Abstract*— This paper presents a new non-isolated high gain (HG) dc-dc topology. Using a magnetically coupled inductor (MCI), the proposed topology can reach a higher voltage gain than those of other topologies with a moderate duty cycle. The voltage gain will be expanded further by enhancing duty cycle of the active power switch or the turn ratio (N). The resonance passive clamping circuits are presented to recycle the energy of leakage inductance and mitigating voltage spikes on the primary power MOSFET efficaciously. Then, the output diode's reverse-recovery problem is lightened by the resonance between leakage inductance and resonance capacitor. Accordingly, the efficiency of the presented HG converter can be improved. The active power switch turns ON and OFF in the zero current switching (ZCS) and zero voltage switching (ZVS) modes, respectively. The numerical investigation and MATLAB/Simulink simulations are depicted in detail. Likewise, an experimental setup is developed using a 100 W solar panel that supplies the suggested dc-dc converter, validating the introduced analysis and simulations.**

***Index Terms*— High gain, dc-dc converter, common-ground, MPPT, low voltage stress, high efficiency.**

I. INTRODUCTION

DC microgrid innovation is spreading because of the penetration of distributed generating sources. One issue with DC generators is the low voltage output, requiring high gain and highly efficient DC to DC topologies instead of cascade connection of DC modules [1]. High gain DC-DC topologies are utilized in numerous applications such as renewable energy sources (e.g., PV and wind systems), battery backup systems for uninterrupted power supplies (UPS), high severity discharge lamp ballasts for automobile headlamps, several clinical types of equipment (e.g., X-ray systems), copy machines and electric tractions [2]-[4].

In the recent past, boost converters were utilized to increase the voltage level. Nonetheless, the voltage stress on most of these converters' switches was equivalent to the output voltage Since voltage stress causes the choice of a higher-rated switch, the conduction losses also increase. On the one hand, in conventional boost converters, using a large duty cycle is not a beneficial solution to increment the voltage gain because it increases the conduction losses in switches and higher voltage spikes. On the other hand, the diode conducts for 5-10 % of the whole time, suffering intense reverse recovery issues [7].

In many studies, isolated DC-DC converters with high switching frequencies have been suggested to reduce losses and dimensions to achieve high voltage gains. One of the major problems with this type of converter is the saturation of the transformer core. A converter realized in [8] using a unique Y-source (YS) impedance network and a two-switch push-pull topology with a voltage-doubling scheme. In this isolated converter, two switches connected to the transformer primary side's common ground show high voltage stress. Half-bridge LLC DC-DC topology is favored in electric vehicles (EV) to use as a charger due to its low losses and soft-switching performance. A small common-mode noise half-bridge LLC DC-DC topology using an asymmetrical center-tapped rectifier is proposed in [14].

Recently, various non-isolated DC-DC topologies with a step-up voltage gain were proposed. Most of the introduced non-insulated high gain topologies are based on a switched-capacitor [9], switched inductors [10], two/three-winding MCI [11], cascaded method [12], voltage multiplier cells [13], or a related combined design. A high gain converter with a single power switch, two hybrid voltage multiplier cells, and a three-winding MCI are suggested in [11]. This converter can attain step-up voltage gain in proper duty cycles and small turn ratios. Nevertheless, the three-winding MCI causes more power losses and makes the converter more complex.

This paper presents a new high voltage gain DC-DC topology consisting of one MCI, two switched capacitors, one active switch and two passive clamping circuits. This proposed topology has the advantages of reducing switching losses, improving drawbacks of the diodes reverse recovery during the turn off along with reducing switching losses of the output diodes by employing resonance circuits that combines capacitors with the leakage inductance. Because of the MCI leakage inductance, the converter's single switch turns ON under the ZCS and uses another resonance circuit switch to turn OFF in a situation like as zero voltage switching (ZVS) condition. This resonance circuit decrease the spike of main switch and recycle it to the capacitance of the input source. An experimental setup was implemented to confirm the introduced comparative analysis. The rest of the paper is formed as follows. The presented topology and its operating principles are depicted in Section II. Steady-state characteristics and the closed loop control of the proposed topology are analyzed in Section III. Key design parameters are described in Section IV. A comparative study is given in Section V. Experimental results and simulations are presented in Section VI. A conclusion is given in Section VII.

II. Proposed Converter: Principles of Operation

The proposed high step-up DC-DC topology is depicted in Fig. 1. This circuit consists of a power switch S_1, a single input inductance L_{in}, a MCI, six diodes D_1, D_2, D_3, D_4, D_5, D_O, a single output capacitor C_O, two resonance capacitors C_{r1}, C_{r2}, and three other capacitors C_1, C_2, C_3. The MCI in this topology can be modeled as an equivalent leakage inductance L_{lk}, a magnetizing inductance L_m and a single ideal transformer with a turn ratio Ns/Np and V_{in} is symbol of PV panel with input capacitor.

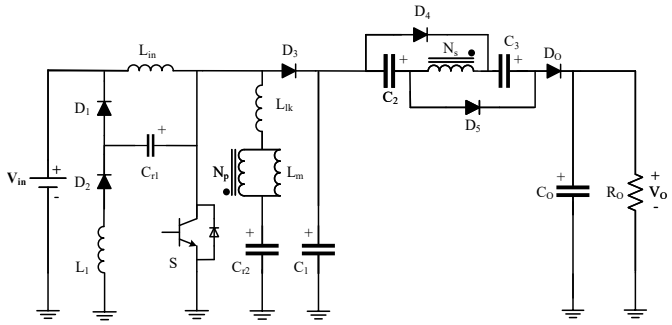

Fig.1. Proposed High Step-up DC-DC topology

Fig.2 depicts the current-flow of all modes of operation for the converter. Operation of the proposed converter in continuous conduction mode (CCM) is divided into seven modes per switching cycle.

A. MODE 1 [0 to t1]:

During this period, the power MOSFET is turned ON. Due to the constant current direction in the MCI windings, capacitors C_2 and C_3 continue to be charged. The inductor current I_{L1} passes through diode D_2, capacitor C_{r1} and the switch S, resonating with capacitor C_{r1} to discharges it. Presence of inductor L_1 forces the current of diode D_2 grows smoothly. Capacitor C_{r2} also resonates with leakage inductance L_{lk}, lowering its voltage. Mathematical description in this mode are as follows:

$$V_{Lin}^{D} = V_{in} \tag{1}$$

$$I_{Lin} = I_{Lin}(t_0) + \frac{V_{in}}{L_{in}}(t - t_0) \tag{2}$$

$$V_{Lm}^{D} = V_{cr2} \tag{3}$$

$$I_{Lm} = I_{Lm}(t_0) + \frac{V_{cr2}}{L_m}(t - t_0) \tag{4}$$

$$I_S = I_{in} + I_{lm} + I_{np} + I_{L1} \tag{5}$$

$$V_{L1}^{D} = V_{cr1} \tag{6}$$

$$I_{L1} = I_{L1}(t_0) + \frac{V_{cr1}}{L_1}(t - t_0) \tag{7}$$

$$I_{L1} = \frac{(\frac{V_{in}}{D'} - V_{in})}{Z_{r1}} \sin\big(\omega_{r1}(t - t_0)\big) = \frac{DV_{in}}{Z_{r1}D'} \sin(\omega_{r1}(t - t_0)) \tag{8}$$

$$V_{cr1} = \frac{DV_{in}}{D'} \cos\big(\omega_{r1}(t - t_0)\big) \tag{9}$$

$$\omega_{r1} = \frac{1}{\sqrt{L_1 C_{r1}}} \text{ , } T_{r1} = 2\pi\sqrt{L_1 C_{r1}} \tag{10}$$

$$Z_{r1} = \sqrt{\frac{L_1}{C_{r1}}} \tag{11}$$

B. MODE 2 [t1 to t2]:

During this period, the direction of current in the MCI is changed, which causes the output voltage V_O increases by charging capacitor C_O. The output capacitor voltage is obtained by summing the voltages of capacitors C_1, C_2, and C_3. This interval continues until the output diode D_O is turned OFF. The following equation describes the output voltage during the second interval:

$$V_O = V_{C1} + V_{C2} + V_{C3} + NV_{Lm}^{D} \tag{12}$$

C. MODE 3 [t2 to t3]:

This mode begins when the output diode turns OFF. The output diode current is slowly reduced to turn OFF. The diode is turned OFF when nearly crossing zero current without switching loss, such that the reverse recovery of the diode is almost diminished. At the end of this interval, the MOSFET is turned OFF.

D. MODE 4 [t3 to t4]:

This interval starts when the MOSFET turns OFF and diode D_1 turns ON. Owing to the leakage inductance in the copuled Inductor, V_{DS} of the power MOSFET increases, but due to the use of passsive snubber in the converter, these voltage spikes are retrieved to the input by diode D_1.

Initially, the voltage of capacitor C_{r1} is increased by a leakage inductance during a resonance process. It turns on diode D_1, and the remaining energy of the leakage inductor returns to the input voltage source.

Another advantage of using this snubber is the increase of capacitance at the MOSFET's Drain. The increase in capacitance causes the switch voltage to rise slowly at the switching instant, and the switch turns OFF at nearly zero voltage condition. This interval continues until diodes D_4 and D_5 are ON, and the following equation is obtained:

$$V_{\text{Lin}}^{D'} = -V_{cr1} \tag{13}$$

E. MODE 5 [t4 to t5]:

This interval starts when both diodes D_4 and D_5 turn ON. By the current flow in the MCI's primary winding side, switching capacitors are charged by the MCI's secondary winding. The current in these diodes increases slowly, and the diodes turn ON take place smoothly. This interval continues until diode D_3 turns ON.

F. MODE 6 [t5 to t6]:

When diode D_1 turns OFF, diode D_3 turns ON; henec, the switch voltage will be clamped to the capacitor voltage C_1. So, its voltage is limited to the capacitor voltage C_1. Diodes D_4 and D_5 also charge the switched capacitors, and the current flows in the MCI winding. This interval finishes when diode D_3 turns OFF. The equations in this mode are derived as follows:

$$V_{Lin}^{D'} = V_{C1} - V_{in} \tag{14}$$

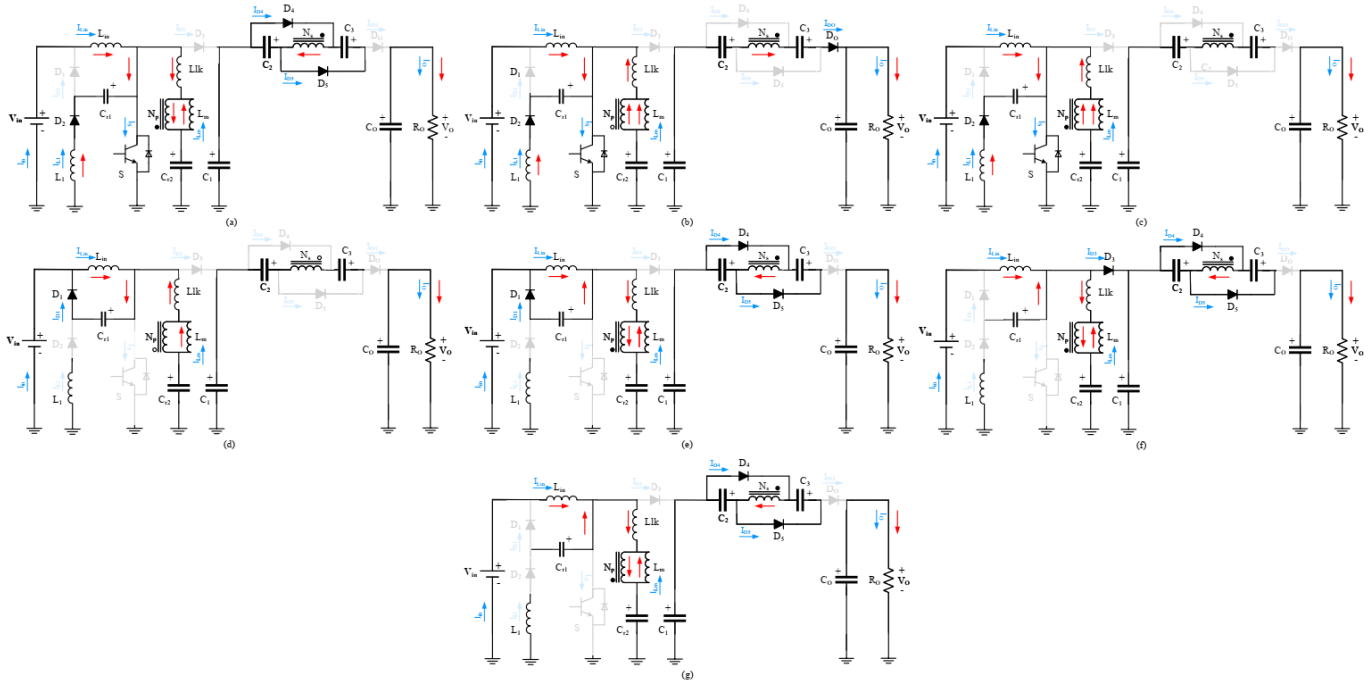

Fig. 2. Operating modes and current paths of the proposed DC-DC topology; (a) first mode, (b) second mode, (c) third mode, (d) fourth mode, (e) fifth mode, (f) sixth mode and (g) the seventh mode.

$$I_{Lin} = I_{Lin}(t_4) + \frac{V_{C1}-V_{in}}{L_{in}}(t - t_0) \quad (15)$$

$$V_{Lm}^{D'} = V_{cr2} - V_{C1} \quad (16)$$

$$I_{Lm} = I_{Lm}(t_4) + \frac{V_{cr2}-V_{C1}}{L_m}(t - t_0) \quad (17)$$

$$-NV_{Lm}^{D'} = V_{C2} = V_{C3} \quad (18)$$

MODE 7 [t6 to t7]:

This interval starts when diodes D_1 and D_3 turn OFF and continues until the MOSFET is tuened ON. Fig.3 illustrates several common waveforms of the proposed topology in CCM operation simulated for a single switching cycle.

III. Steady-State Analysis and Closed-Loop Control of the Proposed Topology

A. Voltage gain calculation

Applying the volt-second balance to V_{Lin} (see (1) and (14)), the following equation is obtained:

$$\int_0^{DT_S} V_{Lin}^{D} dt + \int_{DT_S}^{T_S} V_{Lin}^{D'} dt = 0 \rightarrow V_{C1} = \frac{V_{in}}{D'} \quad (19)$$

Similarly, by applying the same principle to L_m (see (3) and (16)):

$$\int_0^{DT_S} V_{Lm}^{D} dt + \int_{DT_S}^{T_S} V_{Lm}^{D'} dt = 0 \rightarrow V_{cr2} = V_{in} \quad (20)$$

From equations (16), (19), and (20), we get:

$$V_{Lm}^{D'} = -\frac{D}{D'} V_{in} \quad (21)$$

By substituting (21) into (18):

$$V_{C2} = V_{C3} = \frac{ND}{D'} V_{in} \quad (22)$$

The CCM gain of the proposed topology can be found by substituting (3), (19), (20), and (22) into (12):

$$G_m = \frac{V_O}{V_{in}} = \frac{1+2ND+ND'}{D'} \quad (23)$$

Fig.4 shows voltage gain G_m versus duty cycle D of the proposed topology for various turn ratios (N). It can be seen from Fig. 4 that, even the high voltage gains can be reached effectively in low duty cycle ranges. Meanwhile, it is shown that the proposed HG topology can achieve step-up voltage gain without working at the high MCI's turn ratios.

B. Calculation of the rest of the converter ratings

So far, all capacitor voltages were obtained except for the capacitor C_{r1}. Applying the volt-second balance to V_{Lin} (see (1) and (13)), this capacitor voltage is derived as follows:

$$\int_0^{DT_S} V_{\mathrm{Lin}}^{D} dt + \int_{DT_S}^{T_S} V_{Lin}^{D'} dt = 0 \rightarrow V_{cr1} = \frac{D}{D'} V_{in} \quad (24)$$

C. Voltage stress and current of the active switch

As previously indicated, the MOSFET and diodes voltage stress is obtained from the following equations:

$$V_{D1} = V_{in} + \frac{D'}{D} V_{in} = \frac{V_{in}}{D} \quad (25)$$

$$V_{D2} = V_{in} \quad (26)$$

$$V_{D3} = V_S = \frac{V_{in}}{D'} \quad (27)$$

$$V_{D4} = V_{D5} = V_{DO} = \frac{N}{D'} V_{in} \quad (28)$$

To calculate conducting current of the switch, assume L_{in} and L_m are large enough to ignore the current ripple. By applying the charge balance rule to C_2 and C_3, these capacitor currents are equal to the output current. According to (23), ignoring the converter losses results in the following relationships:

$$I_{in} \approx I_{in(avg)} = G_m I_O \quad (29)$$

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$$I_{lm} \approx I_{lm(avg)} = NI_O \quad (30)$$

The currents of the converter diodes are as follows:

$$I_{D1(peak)} \approx (G_m + N)I_O + \frac{DV_{in}}{D'Z_{r1}} \quad (31)$$

$$I_{D2(peak)} \approx \frac{DV_{in}}{D'Z_{r1}} \quad (32)$$

$$I_{D3(peak)} \approx (M + N)I_O \quad (33)$$

$$I_{D4(peak)} = I_{D5(peak)} \approx \frac{(M+N)I_O}{2N} \quad (34)$$

$$I_{Do(peak)} \approx \frac{\pi T_s I_O}{T_{r2}} \approx \frac{\pi I_O}{2D} \quad (35)$$

Also, the switch current is approximately equal to:

$$I_S \approx I_{in} + I_{lm} + \frac{DV_{in}}{D'Z_{r1}}\sin(\omega_{r1}t) + \frac{\pi T_s I_O}{T_{r2}}\sin(\omega_{r2}t) \quad (36)$$

$$\omega_{r2} = \frac{1}{\sqrt{L_{lk}C_{r2}}} \text{ , } T_{r2} = 2\pi\sqrt{L_{lk}C_{r2}}$$

Thus, the MOSFET maximum current and the RMS current are:

$$I_{S(peak)} \approx (M + N)I_o + \frac{DV_{in}}{D'Z_{r1}} + \frac{N\pi T_s I_O}{T_{r2}} \quad (37)$$

$$I_{S(RMS)} \approx \sqrt{\frac{1}{T_s}\int_0^{\frac{T_{r2}}{2}}(I_{in(avg)} + I_{Lm(avg)} + \frac{DV_{in}}{D'Z_{r1}}\sin(\omega_{r1}t) + \frac{N\pi T_s I_O}{T_{r2}}\sin(\omega_{r2}t))^2 dt}$$

$$= \sqrt{\left(\frac{N^2\pi^2 T_S}{4DT_R} + \left(\frac{1+N}{1-D}\right)^2\frac{2T_{r2}}{T_s} + 2N\left(\frac{1+2N}{1-D}\right)\right){I_O}^2 + (\frac{DV_{in}}{D'Z_{r1}})^2} \quad (38)$$

D. Soft Switching Losses

References [11] and [23] used a single switch for their converter in series with the coupled inductor in soft switching condition (only in ZCS condition); thus, the leakage inductance of the coupled inductor opposes the current changes through L_{lk}, which in turn causes the switch starts from zero when turning on, i.e. zero current switching (ZCS) (the switch voltage is already zero). Fig. 12 (h) shows this fact by experimental result. Furthermore, regarding the moment of switch turn off, our suggested converter uses a resonance circuit to apply a situation like zero voltage switching (ZVS) condition for the switch turn off; however, this is not a complete ZVS, but there is much lower dissipation compared to hard switching turn off condition. Moreover, currents of diodes reach zero before their corresponding mode of operation is finished; hence, they do not suffer from reverse recovery problem. Thus, their considerable power losses are just accounted for conducting voltage drop of diodes.

E. Maximum Power Point Tracking (MPPT) algorithm

The proposed model in [15] has been used to manage the MPPT of the input PV cells (see Figs. 5 and 10 (a)). This technique can give a superior outcome than the conventional $0.8V_{oc}$ model, particularly in the case of partial shading on solar cells. It is demonstrated numerically and graphically in [15] that the primitive idea stated in [26] could reach the maximum power point far from that of $0.8V_{oc}$. For this reason, the perturbation and observation method based on the proposed model in [15] is utilized in our suggested topology, where the effectiveness of the MPPT can be improved by roughly 2%.

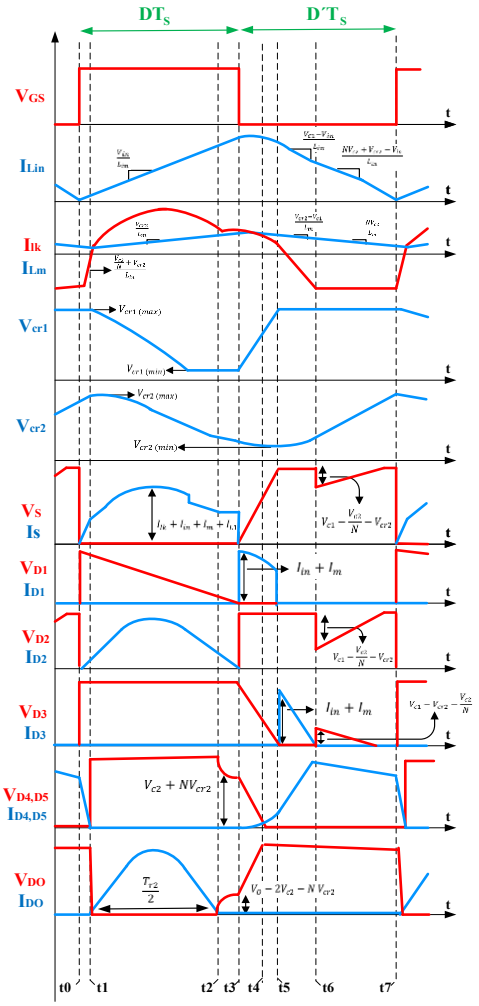

Fig. 3. Common waveforms concering different modes of operation

To show the performance effectiveness of the proposed HG topology in the closed-loop mode, the control scheme of Fig. 5 is utilized. The effect of the PI controller in the proposed scheme is to reduce the output voltage ripple. In this control scheme, $G_v(z)$ presents a discrete-time PI voltage controller.

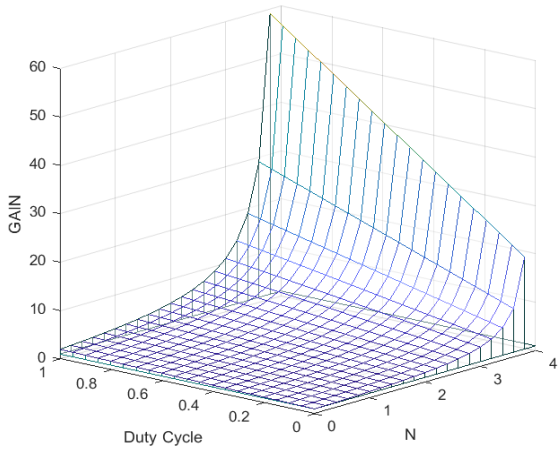

Fig. 4. Voltage gain of the topology vs. duty cycle under different turn ratios.

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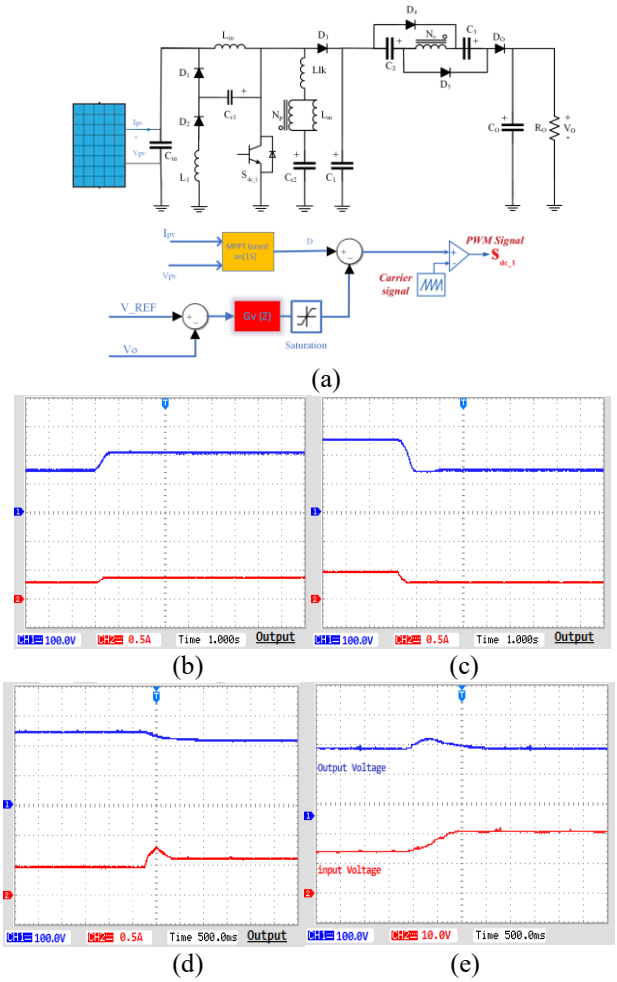

Fig. 5. (a) General construction of the proposed HG converter with MPPT technique and output voltage regulation, (b) output voltage and current when increasing irradiance (time division : 1 Sec./div.), (c) output voltage and current when decreasing irradiance (time division : 1 Sec./div.)and (d) Output voltage and current in over load condition (time division : 500ms/div) (e) Output and input voltage when input voltage is increased (time division : 500ms/div)

To illustrate the overall dynamic response (not power or voltage regulation) of the converter, the following tests are arranged. Figs. 5 (b) and (c) show the dynamic performance of the converter. Here it is shown two implemented tests under MPPT conditions. First, the irradiance level is increased by removing a shadow plane, while the load remains unchanged. As can be seen from Fig. 5 (b), both the voltage and current of output load is increased (voltage from 155V to 208V and current from 0.26A to 0.35A). Second, the irradiance level is decreased by inserting a shadow plane, while still the load remains unchanged. As can be seen from Fig. 5 (c), both voltage and current of the load is decreased (voltage from 219V to 153V and current from 0.45A to 0.26A).

Third, the output load power is increased from the nominal power of the solar cell to check the stability of the output voltage in this case. As can be seen from Fig. 5 (d), when the output power exceeds the maximum power of the panel, the steady state of output voltage decreases while the load current increases slightly; the converter continues performing stable operation. For the last dynamic response analysis, authors used a power supply as the input source in which there is no MPPT control or PV panel; the aim is to regulate desired level of output voltage. As can be seen from Fig. 5 €, the input voltage is changed from 15 V to 20 V and the output voltage remains constant after a short time.

IV. Key Parameter Design

A. Input filter design (L_{in})

Assuming 15% input current ripple, the size of the input inductor is obtained from the following equation:

$$L_{in} = \frac{V_{in}D}{\Delta I_{in} f_s} \rightarrow L_{in} \geq \frac{V_{in}D}{0.15 I_{in} f_s} \tag{39}$$

Fig. 6 is shows the boundary Region between DCM and CCM for Lin = 100 μH; the suggested design works for all duty cycles in the CCM as long as the load resistance is smaller than 1868Ω.

B. Designing capacitors

The following equations are used to calculate the size of capacitors by assuming 1% voltage ripple.

$$C_1 = \frac{P_O}{V_O \Delta V_{c1} f_s} \rightarrow C_1 \geq \frac{P_O D'}{V_O 0.01 V_{in} f_s} \tag{40}$$

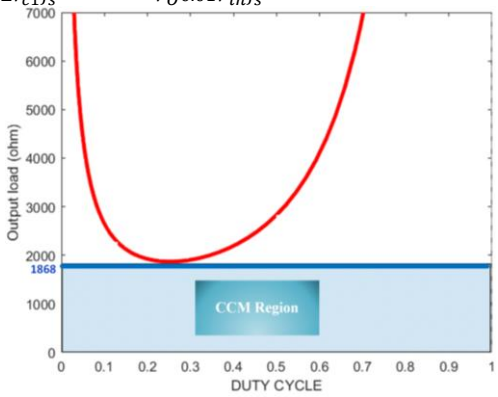

Fig. 6. The boundary Region between DCM and CCM when $L_{in} = 100\mu$H.

$$C_2 = C_3 = \frac{P_O}{V_O \Delta V_{c2} f_s} \rightarrow C_2 = C_3 \geq \frac{P_O D'}{V_O 0.01 N D V_{in} f_s} \tag{41}$$

$$C_O \geq \frac{P_O}{V_O 0.01 V_O f_s} \tag{42}$$

C. Coupled inductor magnetizing inductance design(L_m)

By assuming 50% current ripple, the amount of the magnetic inductance is obtained from the following equation:

$$L_m = \frac{V_{in}D}{\Delta I_{Lm} f_s} \rightarrow L_m \geq \frac{V_{in}D}{0.5 N I_O f_s} \tag{43}$$

To decrease the magnetic field (B_m) and some common relation for Flyback inductor design the ETD 49/25/16 selected as for core of inductor. According to next equation the number of rounds of primary is obtained:

$$N = \sqrt{\frac{L_m l_g}{\mu_0 A_c K_f}} \tag{44}$$

Where l_g is air gap, A_c is core cross-sectional area, μ is equal $4\pi \times 10^{-7}$ and K_f is 1.5.

D. Design of resonance components

The resonance capacitor C_{r1} plays a fundamental role in turning OFF the switch, where the soft switching condtion takes

TABLE I :DETAILED COMPARISON OF THE CHARACTERISTICS OF THE PROPOSED TOPOLOGY WITH THOSE OF OTHER AVAILABLE DC-DC CONVERTERS

Parameters	Proposed	[18] 2016	[22] 2017	[24] 2018	[16] 2018	[11] 2018	[17] 2019	[21] 2019	[27] 2020
N_{sw}	1	1	2	6	1	1	2	1	1
Nominal Gain	12	10	7.9	8.3	10	16	10	8.3	7.15
N_d	6	3	4	0	3	5	2	2	3
N_{cap}	6	3	3	3	4	5	4	3	4
N_{ind}	2+ 1CI(2W)	1CI(2W)	2+1CI(2W)	2+1CI(2W)	1+1CI(2W)	1CI(3W)	1+1CI(2W)	1+1CI(2W)	1+1CI(2W)
Soft Switching Design	✓	×	×	✓	×	×	✓	×	×
Common-Ground	✓	✓	✓	✓	✓	×	✓	✓	✓
Voltage gain (Vo/Vin)	$\frac{1+ND+N}{1-D}$	$\frac{1+N}{1-D}$	$\frac{2+N}{1-D}$	$\frac{1+2N}{1-D}$	$\frac{2+N}{1-D}$	$\frac{2N+3}{1-D}$	$\frac{2N-1}{(N-1)(1-D)}$	$\frac{ND+N-1}{(1-D)(N-1)}$	$\frac{2N-1}{(N-1)(1-D)}$
Voltage stress of main switches	$\frac{V_O}{1+ND+N}$	$\frac{V_O}{1+N}$	$\frac{Vo}{2+N}$	$\frac{2NVo}{1+2N}$	$\frac{Vo}{2+N}$	$\frac{Vo}{2N+3}$	$\frac{Vo}{1+ND+D}$	$\frac{(N-1)Vo}{2N-1}$	$\frac{(N-1)Vo}{2N-1}$
Voltage stress of output diode(s)	$\frac{NV_O}{1+ND+N}$	$\frac{NV_O}{1+N}$	Vo	×	$\frac{(N+1)Vo}{N+2}$	$\frac{(2N+1)Vo}{2N+3}$	$\frac{(N+1)Vo}{1+ND+D}$	Vo	$\frac{NVo}{2N-1}$

*CI – coupled inductor; W–winding ; d–diode; sw–switch; ind–inductor; cap–capacitor.

place by growing the switch voltage from zero up to its circuit rating depending on C_{r1}, the higher the capacitance C_{r1}, the slower will rise switch voltage (t_3-t_5). Hence, the turn OFF switching losses are dramatically reduced. However, according to (5), the large C_{r1} potentially provides considerale discharge capacity for resonance current to the switch. As a result, the excessive increase of this current causes significant losses on the switch. Meanwhile, this can be overcome by increasing inductance L_1, if the resonance period T_{r1} is shorter than or equal to the switching period T_s.

According to [23], to calculate the amount of resonance capacitor C_{r2} and the MCI leakage inductance L_{lk}, these components are designed to operate in below-resonance mode to reduce the output diode switching losses and improve its reverse recovery problems. Thus, the following equation is obtained:

$$\pi\sqrt{L_{lk}C_{r2}} \leq \mathrm{D}T_s \rightarrow C_{r2} \leq \frac{D^2}{\pi^2 L_{lk} f_s^2} \tag{45}$$

E. Efficiency Estimation

Voltage and current stresses of the elements were assessed in the previous sections by choosing suitable duty cycles and turn ratio to lower these stresses. In this part, the dissipation mechanism for the provided topology is assessed to validate the appropriate converter operation. The proposed HG topology will operate under the details given in Table II.

For the active power MOSFET S, the dissipation is divided into switching and conduction losses. Due to the soft switching operation, when the MOSFET turns ON (starting current from zero smoothly to its rating value) along with turn OFF (starting voltage from zero smoothly to its rating value), the switching losses of the MOSFET is quite negligible. The conduction loss can be calculated as:

$$P_{sconduction} = R_{DS(ON)}\, I_{switch(RMS)}{}^2. \tag{46}$$

Where $R_{DS(on)}$ is the switch on-resistance during the conduction mode given by the datasheet and $I_{switch(RMS)}$ is the RMS current of the switch given by (34). It is noticeable that the experimental prototype gives conduction losses equal to 0.43 W according to (46) (see section VI).

Diodes conduction dissipation can be surmised as follows:

$$P_{diode} = V_{Forward}\, I_{D(RMS)} \tag{47}$$

Where $V_{Forward}$ is the diode threshold voltage obtained from the datasheet attributes and $I_{D(RMS)}$ is the RMS current. Also, the experimental prototype gives diode conduction losses equal to 2.05 W according to (47) . Also, the equivalent series resistor (ESR) of the capacitors, expressed in Table II, gives the total capacitors' losses as below:

$$P_{Capacitors} = \mathrm{ESR}.\, I_{C(RMS)}{}^2 \tag{48}$$

Where $I_{C(RMS)}$ is the RMS current of the capacitor. The practical ESR losses are worked out using (48) as 0.36 W (see section VI). Further, the ferrite core of the MCI and iron powder of input inductor in this converter imposes hystheresis and eddy current losses. According to [25], the total magnetic and copper losses can be calculated as:

$$\begin{cases} P_{Lin}^{Copper} + P_{MCI}^{Copper} = R_{Lin}\, I_{L(RMS)}^2 + R_{MCI}\, I_{MCI(RMS)}^2 \\ P_{Lin}^{Core} + P_{MCI}^{Core} = (\alpha B^x f_{sw} y) A_c l_c + \frac{1}{2} f_{sw} L_k I_{Lmax}^2 \end{cases} \tag{49}$$

where α, x, y are constant parameters were chosen from the core curve fitting, B is the AC magnetic flux density for the magnetic component core, l_c is the medium path length (MPL) of the core and A_c is the transversal area of this core. The total losses shown by (46)-(49) is illusterated as a pie chart in Fig. 8 for the implemented converter, where V_{in} is 18V and the output load is 100 W.

V. COMPARATIVE STUDY

In this section, a detailed comparative study is provided for various topologies, where the converters use the MCI under the same conditions for a fair comparison. Figure 7 compares voltage gain of various topologies for D = 0.5, showing the proposed topology provides higher voltage gains compared to those of [16]-[18] under turn ratios bigger than 2.5. Table I clearly depicts that the provided topology's voltage conversion

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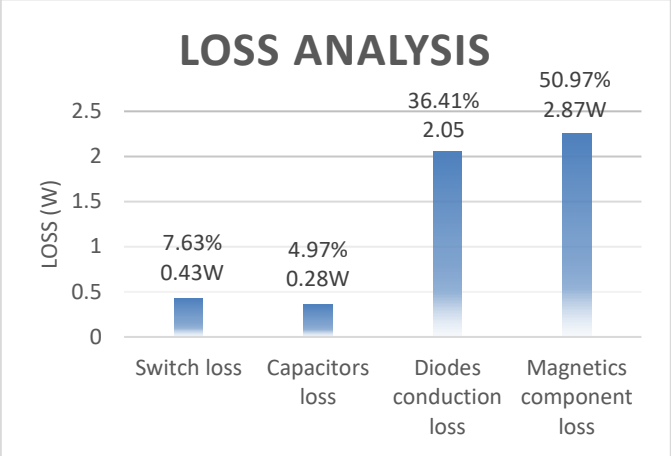


Fig. 8. Power losses of different elements (for 100 kHz switching frequency) within the presented topology shown by a bar-chart.

ratio is expanded by increasing the turns ratio (in the numerators). In contrast, the converter's gain in [16] is nonlinearly decreased by increasing the turns ratio (in the denominator).

Fig. 10 depicts the voltage gain comparison in several high gain converters. As indicated in Fig. 10, our proposal provides voltage gains higher than those of other converters for all duty cycles. According to Fig. 10 voltage gain of the suggested converter is higher than other converters except the converter of [24] and it should be considered that the [24] has six main active switches which can increase the total price and complexity of the converter.

The normalized voltage stress (Vstress/Vos) of the active power switch and output diode (see Table I) as shown in Fig. 11 for turns ratio $N = 3.3$; voltage stresses of the suggested HG topology is lower than those of other proposals, while the increase in duty ratio lowers the voltage stress within a limited range. A comparison of the HG topologies is presented in Table I, describing the analytic comparison in terms of voltage stress of switches/output diodes, the number of inductors, capacitors and switches along with common-ground, soft switching capability and voltage gain. It can be seen from Table I that the suggested HG converter provides high voltage with low voltage stress of active power MOSFET and output diode.

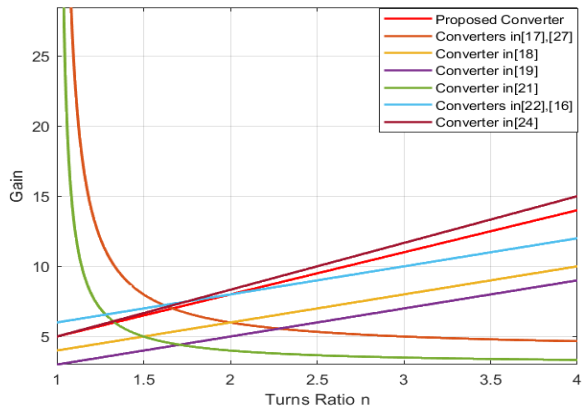


Fig. 9. Voltage gain comparison among different converters in terms of fixed duty cycle (D=0.5)

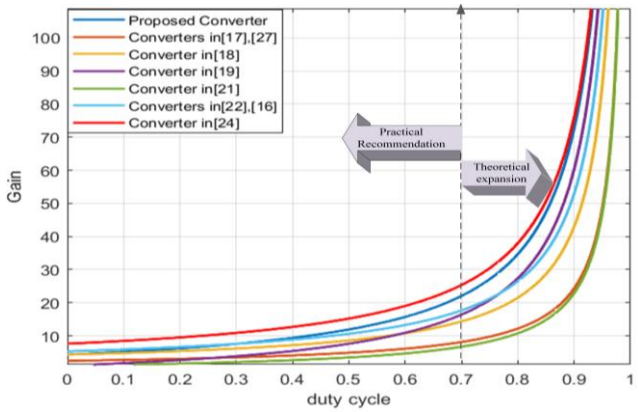


Fig. 10. Voltage gain comparison among different topologies in terms of a fixed turns ratio (N =3.3)

VI. Experiments and Discussions

In order to investigate the high quality of the suggested HG converter, a 100W, (17 (V) – 20 (V))-input 240V-output prototype is built as shown in Figs. 12 (a)–(b). The C2000 digital signal processors and microcontrollers TMS320F28335 have been utilized to generate the switching pulses. The switching frequency is 100 kHz, and the duty cycle of the MOSFET is roughly 0.51 under nominal condition. Table II lists the parameters of the practical setup, where the overall experimental test setup photo is shown by Fig. 12 (a) and the proposed HG converter prototype in Fig. 12 (b).

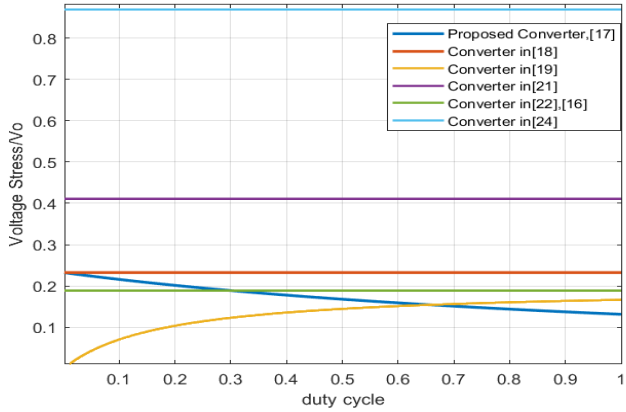
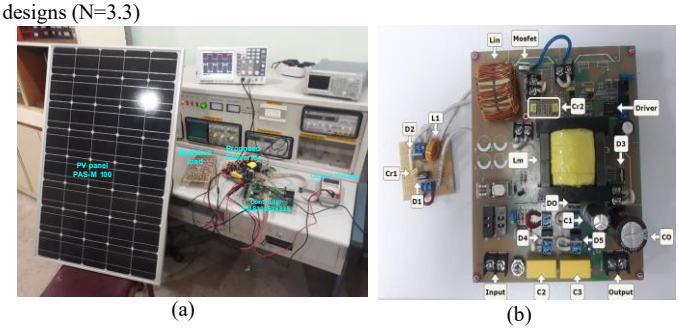
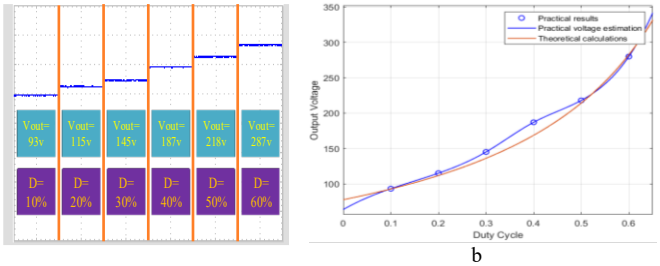


Fig. 11. Comparing normalized voltage stress on active switch for various designs (N=3.3)



(a) (b)

Fig. 12. Experimental hardware, (a) experimental test setup, and (b) implemented HG converter prototype.



a b

Fig. 13. Output voltage when the input is fixed, (a) experimental different duty cycles at six different operating conditions, and (b) comparing practical operating conditions with those of theoretical analysis given by (23).

A. Voltage gain

Fig. 13 (a) depicts practical output voltage in different duty cycles while the input voltage is approximately constant 18V under a fixed output load for six different duty cycles. Figure 13 (b) compares these experimental gains with those of simulated gains (see (23)). This figure validates the accuracy of the theoretical analysis presented in section II.

TABLE II
PARAMETERS OF THE EXPERIMENTAL SETUP

Parameter	Description/ Value	Parameter	Value
Switch	IRFB4110 MOSFET, 4.5 mΩ on-resistance	$\mathbf{V_{in}}$	20 V
$\mathbf{D_1, D_2, D_3, D_4, D_5, D_O}$	MBR2045CTG , $V_F = 0.5$ V V30202C Schottky diode, $V_F = 0.54$ V	$\mathbf{V_{out}}$	240 V
Magnetically Coupled Inductor (MCI)	Turn ratio: 3.3 (N_1:N_2=20:66) Core: ETD 49/25/16 ferrite core Magnetizing inductance: 100μH With PSPS winding Leakage inductance: 1/5 μH	$\mathbf{P_{out}}$	100 W
$\mathbf{L_{in}}$ **L1**	100 μH, 23 turns wrapped on double T131-52 iron powder core 100 μH, 40 turns wrapped on T68-26 iron powder core	**Duty cycle**	0.50
$\mathbf{C_1}$	22 μF, 100 V, ESR=100 mΩ, NIPPON CHEMI-CON	$\mathbf{V_{S(peak)}}$ $\mathbf{V_{D1(peak)}}$ $\mathbf{V_{D2(peak)}}$	43.4 V 43.2 V 20.1 V
$\mathbf{C_2, C_3}$	8.2 μF, 63 V AC (MKT)	$\mathbf{V_{D3(peak)}}$ $\mathbf{V_{D4(peak)}}$	43.2 V 135.6 V
$\mathbf{C_O}$	180 μF, 250 V, ESR=70 mΩ, NIPPON CHEMI-CON	$\mathbf{V_{D5(peak)}}$ $\mathbf{V_{DO(peak)}}$	135.3 V 135.5 V
$\mathbf{C_{r1}}$ $\mathbf{C_{r2}}$	47 nF (MKT) 1.68 μF (MKT)		
Switching Frequency	100 kHz	**Nominal Gain**	12

B. Soft operation of diodes

The experimental waveforms of voltages and currents of the diodes (D_1, D_3, D_4) are demonstrated in Figs. 14 (a)-(c). As can be seen from these Figures, these diodes operate in soft operating mode, where the usual reverse recovery problem is avoided significantly. The biggest voltage stress on diodes D_1, D_3 and D_4 is around 39.3 V, 38.3 V and 123.6 V, respectively, which are in accordance with (25)-(28). Moreover, the current and voltage across the output diode D_O are demonstrated in Fig. 14 (d), showing the diode current D_O increases softly during the turn on and decays gently toward zero during the turn off. In other words, this output diode has nearly negligible switching losses,in particular, resolving the reverse-recovery issue.

C. Capacitors and inductor

Figures 14 (e)-(f) demonstrate the voltage waveforms of the resonance capacitors C_{r1} and C_{r2}, respectively. The maximum voltage values of the resonance capacitors C_{r1} and C_{r2} are 20.3 V and 27.1 V, in accordance with (20). The voltage across and the current through primary side of the MCI are shown in Fig 14 (g). The maximum current of the coupled Inductor L_{lk} is 11.24 A. The experimental results confirms the theoreetical analysis given by (44) for the proposed converter.

D. Soft operation of switch

The voltage and current waveforms of the switch are shown in Fig. 14 (h). The highest stress on the active MOSFET S_1 is 42.13 V. It can be seen that the active power MOSFET turns ON and OFF very softly due to the presence of capacitor C_{r1} (see the loop containing D_1, C_{r1} and MOSFET during turn off and the loop L_1, D_2, C_{r1} and MOSFET during turn on). Furthermore, the highest voltage stress on the MOSFET is approximately 5.3 times lower than the output voltage in this situation and there is no ringing in experimental result of the MOSFET.

E. Shunted capacitor with PV cell

Figs. 14 (i) and 14 (j) show the voltage and current of input and output of the converter, respectively. A capacitor was used as the DC link at the input of the converter in order to absorb possible reversing current toward the input PV cell.

F. Efficiency:

Fig. 15 compares the efficiency of the proposed topology with those of other high gain suggestions based on two-winding CIs available in Table 1. As can be seen from Fig. 15 the efficiency of suggested topology is 94.67% at 100W output power (100kHz prototype) and 95.44% for 100 kHz simulations. The higher would be the output power, the higher will be the efficiency of 100 kHz design. Also, both black and brown curves show higher efficiencies at higher output powers in comparison with those of the other converters.

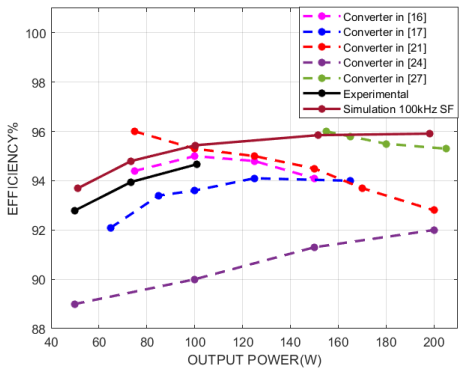


Fig. 15. Efficiency comparison between proposed converter and other high gain topologies (SF: Switching Frequency).

G. Cost Comparison:

In this section, in order to compare the proposed converter with converters in the Table I, a cost comparison has been done. Table III shows the costs of different parts of the proposed converter with those of other converters; references such as mouser electronics and Digi-Key Electronics have been used to collect these costs. Considering Table III, total cost of the converter design in [18] is cheaper than the proposed converter;

this is because soft switching is not applied in [18] and the switch stress is allowed to be higher (lower active switch life expectancy). It can also be seen the low total cost of the proposed converter is because of the use of low-size elements such as C_{r1} and L_1.

TABLE III. Comparing costs of the converters listed in Table I.

Converters	Switches	diodes	Capacitors	Inductors (Cores)	Total
Suggested Converter	$4.29	$14.24	$3.22	$3.6	$25.35
[11]	$6.44	$35.18	$10.7	$4.2	$56.52
[16]	$6.04	$7.86	$7.2	$3.6	$24.7
[17]	$8.51	$6.17	$5.7	$9.6	$29.98
[18]	$7.88	$5.5	$5.416	$2.8	$21.596
[21]	$8.14	$5.42	$11.1	$7.6	$32.26
[22]	$10.48	$7.76	$4.4	$12.4	$35.04
[24]	$57.18	$0	$5.76	$5.3	$68.24
[27]	$4.42	$4.38	$16.04	$4.6	$29.44

I. CONCLUSION

This article proposes a new single-switch high gain MCI boost topology. The suggested topology is analyzed, showing the following specifications:

1. The turn ratio of the MCI contributes to accomplish high voltage gain by charging capacitors C_2 and C_3.
2. The energy of leakage inductance can be recovered using the resonance circuit and leakage inductor.

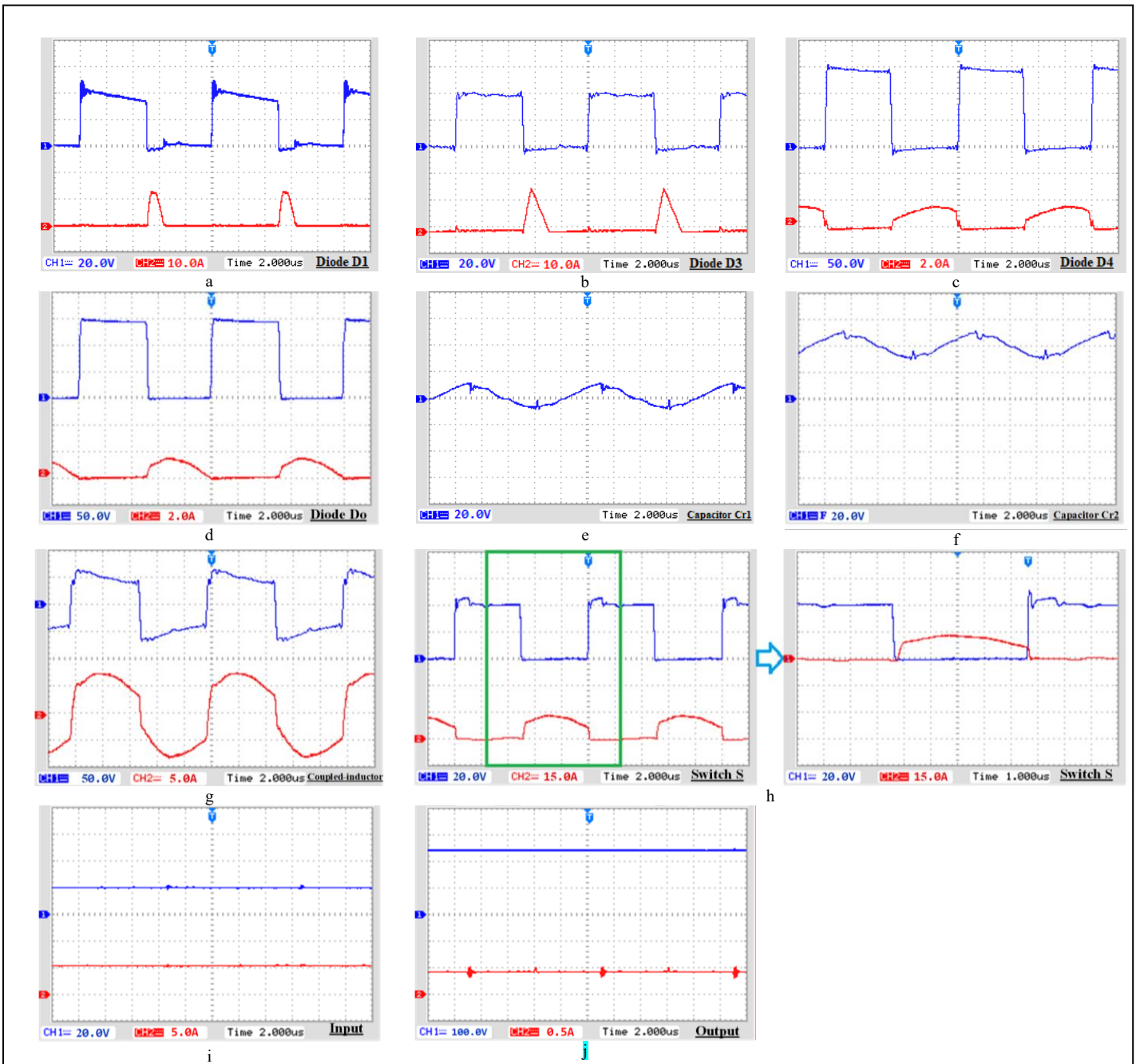


Fig. 14. Current and Voltage stresses on)a) diode D_1, (b) diode D_3, (c) diode D_4, (d) diode D_o; (e) capacitor voltage (C_{r1}), (f) capacitor voltage (C_{r2}), (g) coupled-inductor voltage and current, (h) conducting current and breaking voltage on switch S, (i) voltage and current of input side, and (j) voltage and current of output side; time division: 2μs/div.

3. Reverse recovery of diodes is resolved, while it is required a switch with low voltage stress. Hence, selecting one low-voltage-rating MOSFET lowers conduction losses of the converter due to smaller on-resistance, resulting in higher total efficiency. Moreover, a low side MOSFET driver can be used.
4. Unlike the conventional MCI-based converters, the voltage spikes on MOSFET due to the leakage inductance are totally vanished for the suggested topology.
5. Breaking voltage of the output diode is much smaller than the output voltage; this allows choosing a less expensive diode.
6. Switching losses of the diodes, especially output diodes, are negligible; this soft design for the diodes and MOSFET enables high efficiency for the converter.
7. Due to the soft switching operation and lack of voltage ringing for power switch, the converter's EMI noise is low.

The suggested single-switch two-winding topology offers the high gain of 12 at a moderate duty cycle of 0.5 (still can be increased further), which is an advantage for this proposal compared to other available designs.

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